CS4334/5/6/7/8/9

8-Pin, 24-Bit, 96 kHz Stereo D/A Converter

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 24-Bit Conversion
- 96 dB Dynamic Range
- -88 dB THD+N
- Low Clock Jitter Sensitivity
- Single +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Popguard™ Technology
- Functionally Compatible with CS4330/31/33

Description

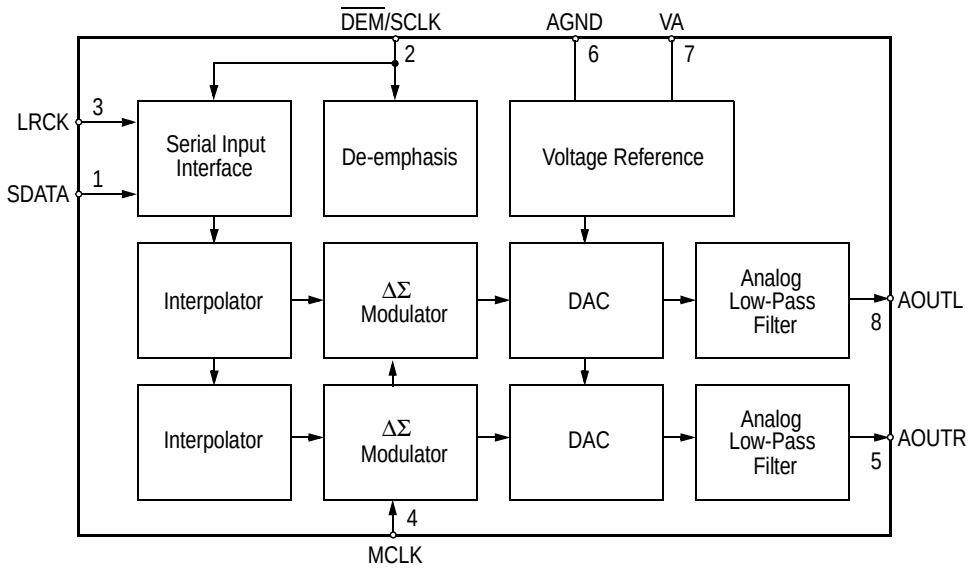
The CS4334 family members are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. The CS4334/5/6/7/8/9 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support circuitry. These features are ideal for set-top boxes, DVD players, SVCD players, and A/V receivers.

ORDERING INFORMATION

See page 23



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; Logic "1" = VA = 5 V; Logic "0" = AGND; Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 40 kHz, unless otherwise specified. Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1))

Parameter			Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Dynamic Performance for CS4334/5/6/7/8/9-KS										
Specified Temperature Range			T_A	-10	-	70	-10	-	70	°C
Dynamic Range		(Note 1)								
	18 to 24-Bit	unweighted		88	93	-	-	90	-	dB
		A-Weighted		91	96	-	91	96	-	dB
	16-Bit	unweighted		86	91	-	-	88	-	dB
		A-Weighted		89	94	-	89	94	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N							
	18 to 24-Bit	0 dB		-	-88	-83	-	-88	-83	dB
		-20 dB		-	-73	-68	-	-70	-65	dB
		-60 dB		-	-33	-28	-	-30	-25	dB
	16-Bit	0 dB		-	-86	-81	-	-86	-81	dB
		-20 dB		-	-71	-66	-	-68	-63	dB
		-60 dB		-	-31	-26	-	-28	-23	dB
Interchannel Isolation		(1 kHz)		-	94	-	-	95	-	dB
Dynamic Performance for CS4334/5/6/7/8/9-BS										
Specified Temperature Range			T_A	-40	-	85	-40	-	85	°C
Dynamic Range		(Note 1)								
	18 to 24-Bit	unweighted		85	93	-	-	90	-	dB
		A-Weighted		88	96	-	88	96	-	dB
	16-Bit	unweighted		83	91	-	-	88	-	dB
		A-Weighted		86	94	-	86	94	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N							
	18 to 24-Bit	0 dB		-	-88	-82	-	-88	-82	dB
		-20 dB		-	-73	-65	-	-70	-62	dB
		-60 dB		-	-33	-25	-	-30	-22	dB
	16-Bit	0 dB		-	-86	-70	-	-86	-80	dB
		-20 dB		-	-71	-63	-	-68	-60	dB
		-60 dB		-	-31	-23	-	-28	-20	dB
Interchannel Isolation		(1 kHz)		-	94	-	-	95	-	dB

Notes: 1. One-half LSB of triangular PDF dither added to data.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Combined Digital and On-chip Analog Filter Response (Note 2)								
Passband (Note 3)								
to -0.05 dB corner		0	-	.4780	-	-	-	Fs
to -0.1 dB corner		-	-	-	0	-	.4650	Fs
to -3 dB corner		0	-	.4996	0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz		-.01	-	+.08	-.05	-	+.2	dB
Passband Ripple		-	-	±.08	-	-	±.2	dB
StopBand		.5465	-	-	.5770	-	-	Fs
StopBand Attenuation (Note 4)		50	-	-	55	-	-	dB
Group Delay	tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation 0 - 40 kHz		-	±0.36/Fs	-	-	±1.39/Fs	-	s
0 - 20 kHz					-	±0.23/Fs	-	s
De-emphasis Error Fs = 32 kHz		-	-	+1.5/+0				dB
Fs = 44.1 kHz		-	-	+.05/-.25		(Note 5)		dB
Fs = 48 kHz		-	-	-.2/-.4				dB

Parameters	Symbol	Min	Typ	Max	Units
dc Accuracy					
Interchannel Gain Mismatch		-	0.1	0.4	dB
Gain Error		-	±5	-	%
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		3.25	3.5	3.75	Vpp
Quiescent Voltage	V_Q	-	2.2	-	VDC
Max AC-Load Resistance (Note 6)	R_L	-	3	-	kΩ
Max Load Capacitance (Note 6)	C_L	-	100	-	pF

Notes:
2. Filter response is not tested but is guaranteed by design.
3. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 17-24) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
4. For Base-Rate Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For High-Rate Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
5. De-emphasis is not available in High-Rate Mode.
6. Refer to Figure 2.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	normal operation	I_A	-	15	19	mA
	power-down state	I_A	-	40	-	µA
Power Dissipation	(Note 7)					
	normal operation		-	75	104	mW
	power-down		-	0.2	-	mW
Package Thermal Resistance		θ_{JA}	-	110	-	°C/Watt
Power Supply Rejection Ratio	(1 kHz)	PSRR	-	79	-	dB

Notes: 7. Refer to Figure 3. Max Power Dissipation is measured at VA=5.5V.

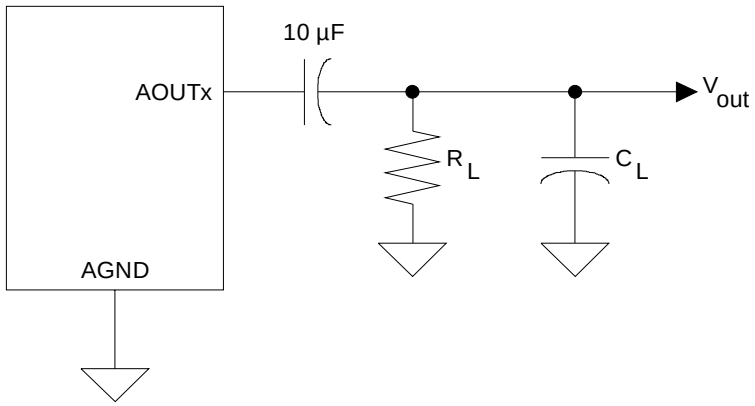


Figure 1. Output Test Load

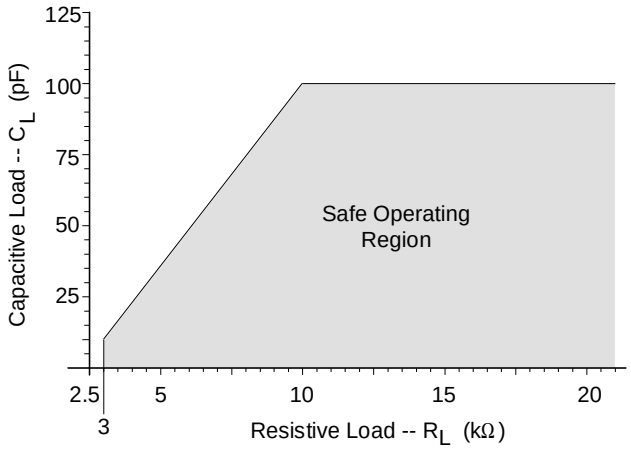


Figure 2. Maximum Loading

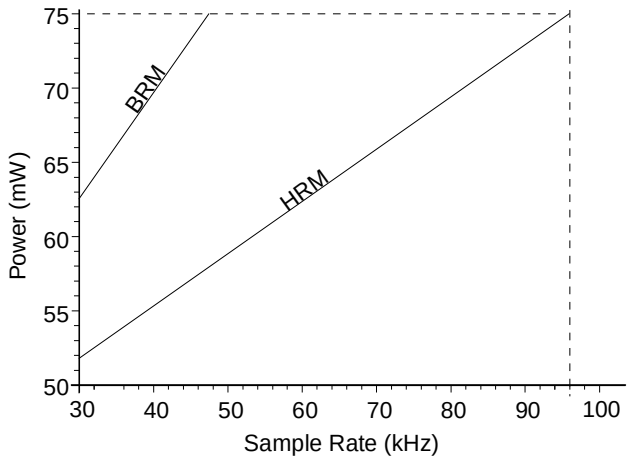


Figure 3. Power vs. Sample Rate

DIGITAL CHARACTERISTICS (T_A = 25°C; VA = 4.75V - 5.5V)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
Input Leakage Current (Note 8)	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

Notes: 8. I_{in} for CS433X LRCK is ±20µA max.

ABSOLUTE MAXIMUM RATINGS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VA	4.75	5.0	5.5	V

SWITCHING CHARACTERISTICS (T_A = -40 to 85°C; VA = 4.75V - 5.5V; Inputs: Logic 0 = 0V, Logic 1 = VA, CL = 20pF)

Parameters	Symbol	Min	Typ	Max	Units
Input Sample Rate	Fs	2	-	100	kHz
MCLK Pulse Width High MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width Low MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 256 or 128		31	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 256 or 128		31	-	1000	ns
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		40	50	60	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Period MCLK / LRCK = 512, 256 or 384	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period MCLK / LRCK = 128 or 192	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 9)		-	50	-	%
SCLK Period (Note 10)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 9. In Internal SCLK Mode, the Duty Cycle must be 50% +/– 1/2 MCLK Period.

10. The SCLK / LRCK ratio may be either 32, 48, or 64. This ratio depends on part type and MCLK/LRCK ratio. (See figures 10-15)

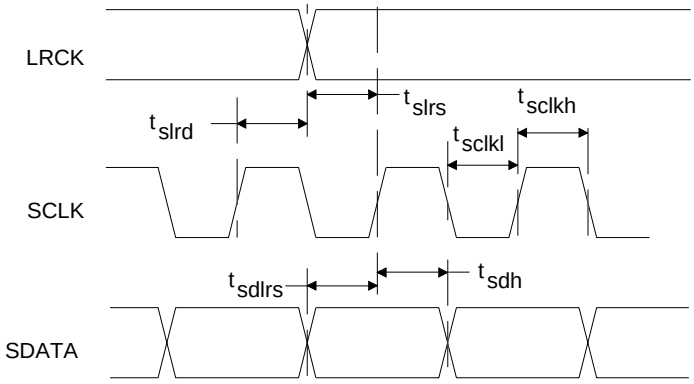


Figure 4. External Serial Mode Input Timing

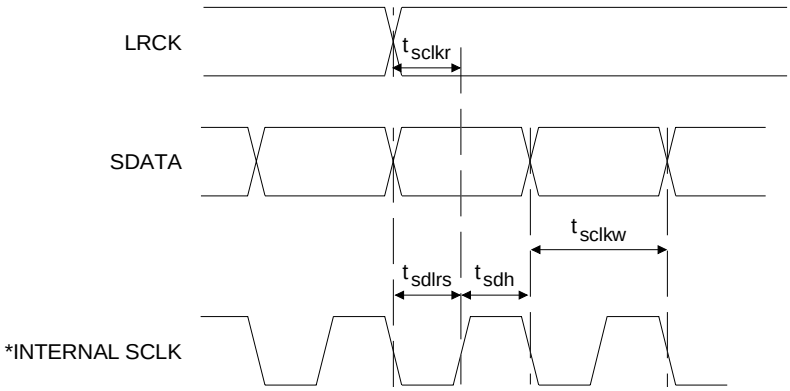


Figure 5. Internal Serial Mode Input Timing

* The SCLK pulses shown are internal to the CS4334/5/6/7/8/9.

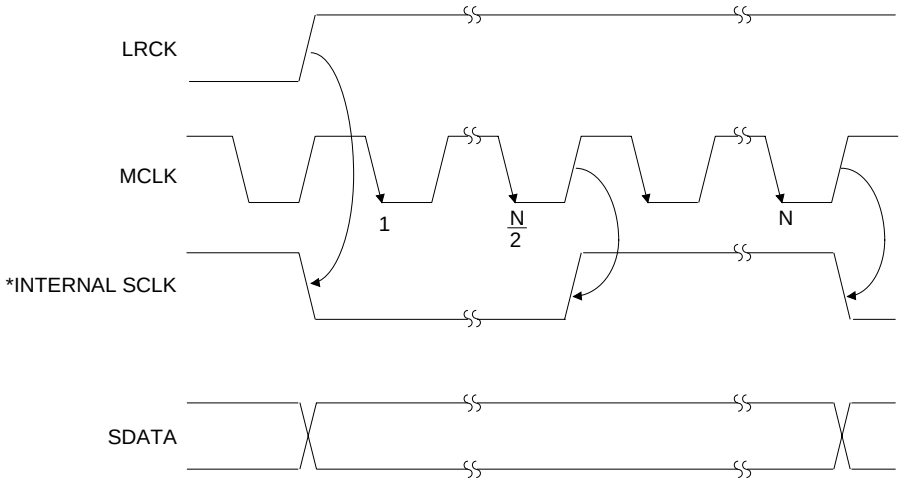


Figure 6. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4334/5/6/7/8/9.

N equals MCLK divided by SCLK

2. TYPICAL CONNECTION DIAGRAM

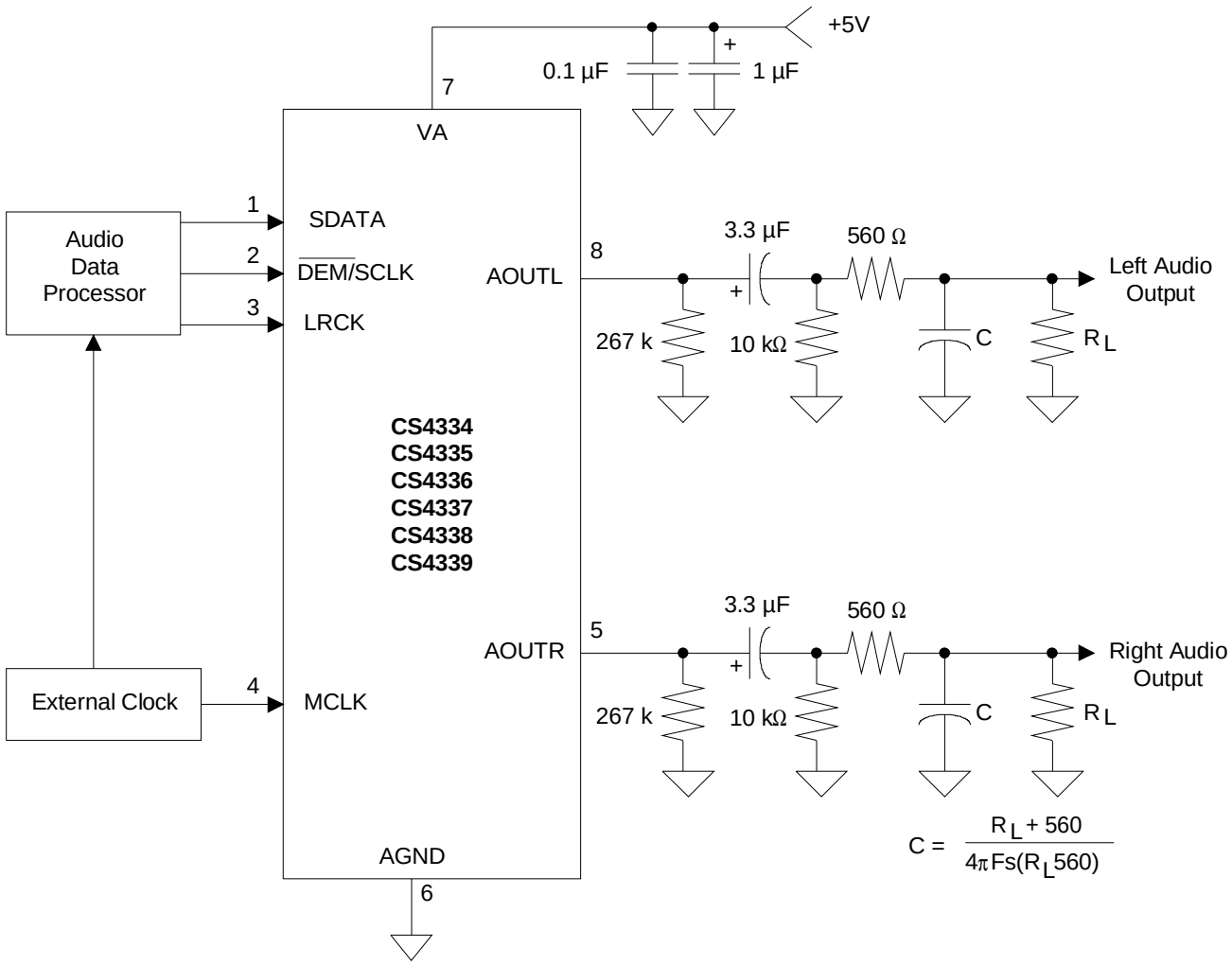


Figure 7. Recommended Connection Diagram

3. GENERAL DESCRIPTION

The CS4334 family of devices offers a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and analog filtering, as shown in Figure 8. This architecture provides a high tolerance to clock jitter.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of resistive laser trimmed digital-to-analog converter architectures by using an inherently linear 1-bit digital-to-analog converter. The advantages of a 1-bit digital-to-analog converter include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

The CS4334 family of devices supports two modes of operation. The devices operate in Base Rate Mode (BRM) when MCLK/LRCK is 256, 384 or 512 and in High Rate Mode (HRM) when MCLK/LRCK is 128 or 192. High Rate Mode allows input sample rates up to 100 kHz.

3.1 Digital Interpolation Filter

The digital interpolation filter increases the sample rate, Fs, by a factor of 4 and is followed by a 32× digital sample-and-hold (16× in HRM). This filter eliminates images of the baseband audio signal which exist at multiples of the input sample rate. The resulting frequency spectrum has images of the input signal at multiples of 4 Fs. These images are easily removed by the on-chip analog low-pass filter and a simple external analog filter (see Figure 7).

3.2 Delta-Sigma Modulator

The interpolation filter is followed by a fourth order delta-sigma modulator which converts the interpolation filter output into 1-bit data at a rate of 128 Fs in BRM (or 64 Fs in HRM).

3.3 Switched-Capacitor DAC

The delta-sigma modulator is followed by a digital-to-analog converter which translates the 1-bit data into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit data. This technique greatly reduces the sensitivity to clock jitter and provides low-pass filtering of the output.

3.4 Analog Low-Pass Filter

The final signal stage consists of a continuous-time low-pass filter which serves to smooth the output and attenuate out-of-band noise.

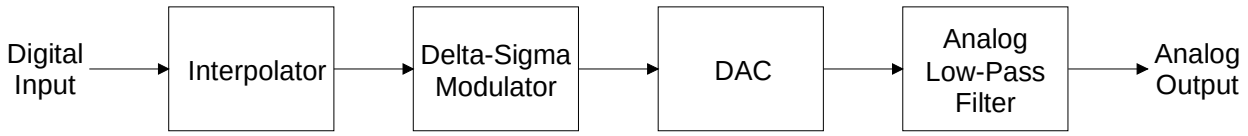


Figure 8. System Block Diagram

4. SYSTEM DESIGN

The CS4334 family accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in BRM and 96, 88.2 and 64 kHz in HRM. Audio data is input via the serial data input pin (SDATA). The Left/Right Clock (LRCK) defines the channel and delineation of data, and the Serial Clock (SCLK) clocks audio data into the input data buffer. The CS4334/5/6/7/8/9 differ in serial data formats as shown in Figures 10-15.

4.1 Master Clock

MCLK must be either 256x, 384x or 512x the desired input sample rate in BRM and either 128x or 192x the desired input sample rate in HRM. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are set to generate the proper clocks. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

LRCK (kHz)	MCLK (MHz)				
	HRM		BRM		
	128x	192x	256x	384x	512x
32	4.0960	6.1440	8.1920	12.2880	16.3840
44.1	5.6448	8.4672	11.2896	16.9344	22.5792
48	6.1440	9.2160	12.2880	18.4320	24.5760
64	8.1920	12.2880	-	-	-
88.2	11.2896	16.9344	-	-	-
96	12.2880	18.4320	-	-	-

Table 1. Common Clock Frequencies

4.2 Serial Clock

The serial clock controls the shifting of data into the input data buffers. The CS4334 family supports both external and internal serial clock generation modes. Refer to Figures 10-15 for data formats.

4.2.1 External Serial Clock Mode

The CS4334 family will enter the External Serial

Clock Mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4334 family will switch to Internal Serial Clock Mode if no low to high transitions are detected on the DEM/SCLK pin for 2 consecutive frames of LRCK. Refer to Figure 16.

4.2.2 Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures 10 - 16 for details.

While the Internal Serial Clock Mode is provided to allow access to the de-emphasis filter, the Internal Serial Clock Mode also eliminates possible clock interference from an external SCLK.

4.3 De-Emphasis

The CS4334 family includes on-chip digital de-emphasis. Figure 9 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the DEM/SCLK pin is low (high) for 5 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode.

4.4 Initialization and Power-Down

The Initialization and Power-Down sequence flow chart is shown in Figure 16. The CS4334 family enters the Power-Down State upon initial power-up.

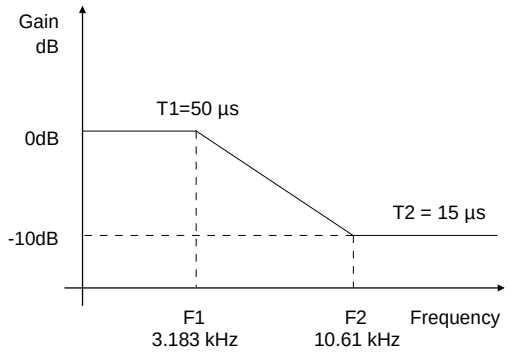


Figure 9. De-Emphasis Curve (Fs = 44.1kHz)

The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, one-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down mode until MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, V_Q.

4.5 Output Transient Control

The CS4334 family uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. After a short delay of approximately 1000 sample periods, each output begins to ramp towards its quiescent voltage, V_Q. Approximately 10,000 sample cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to V_Q, effectively blocking the quiescent DC voltage.

To prevent transients at power-down, the device must first enter its power-down state. This is accomplished by removing MCLK or LRCK. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. A soft-start current sink is substituted in place of AOUTL and AOUTR which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

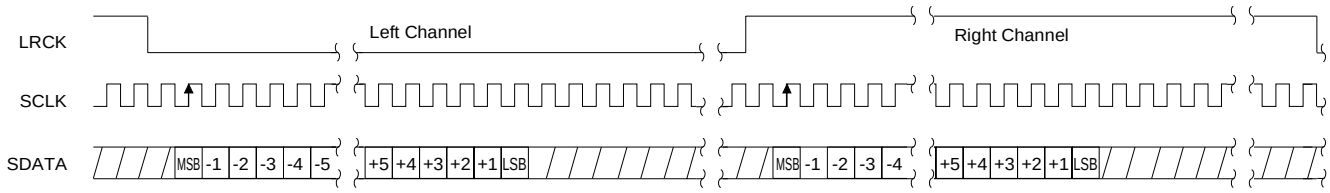
To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning off the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the time that the device must remain in the power-down state will be approximately 0.4 seconds.

4.6 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4334 family requires careful attention to power supply and grounding arrangements to optimize performance. Figure 7 shows the recommended power arrangement with VA connected to a clean +5V supply. For best performance, decoupling capacitors should be located as close to the device package as possible with the smallest capacitor closest.

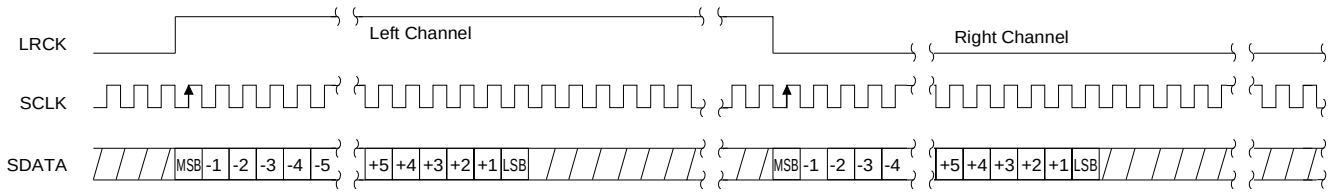
4.7 Analog Output and Filtering

The analog filter present in the CS4334 family is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 17 - 24.



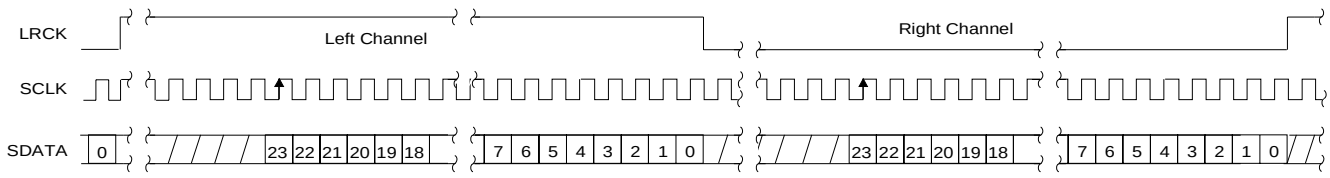
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	I^2S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 10. CS4334 Data Format (I^2S)



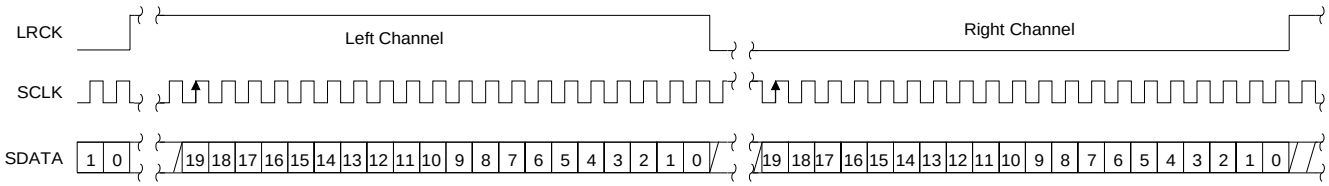
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Left Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 11. CS4335 Data Format



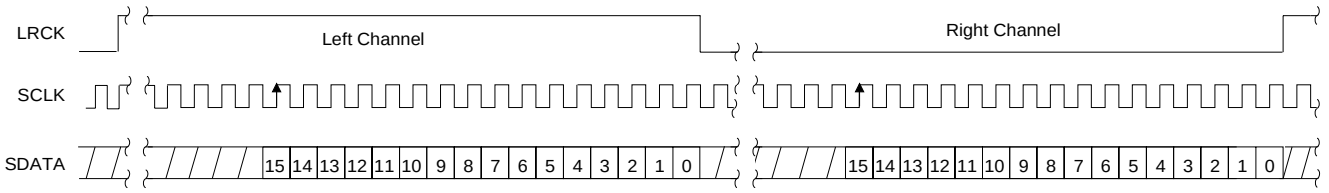
Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 12. CS4336 Data Format



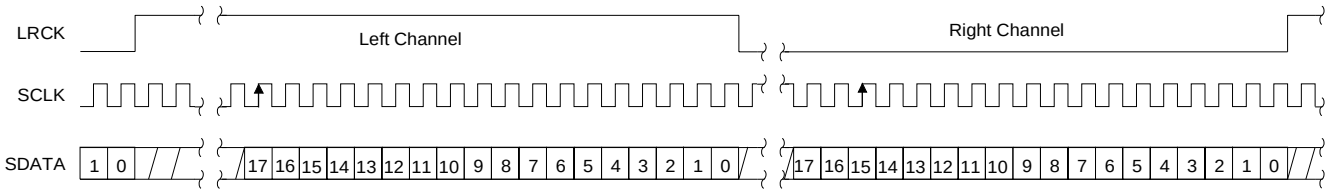
Internal SCLK Mode	External SCLK Mode
Right Justified, 20-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 20-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 40 Cycles per LRCK Period

Figure 13. CS4337 Data Format



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 14. CS4338 Data Format



Internal SCLK Mode	External SCLK Mode
Right Justified, 18-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 18-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 36 Cycles per LRCK Period

Figure 15. CS4339 Data Format

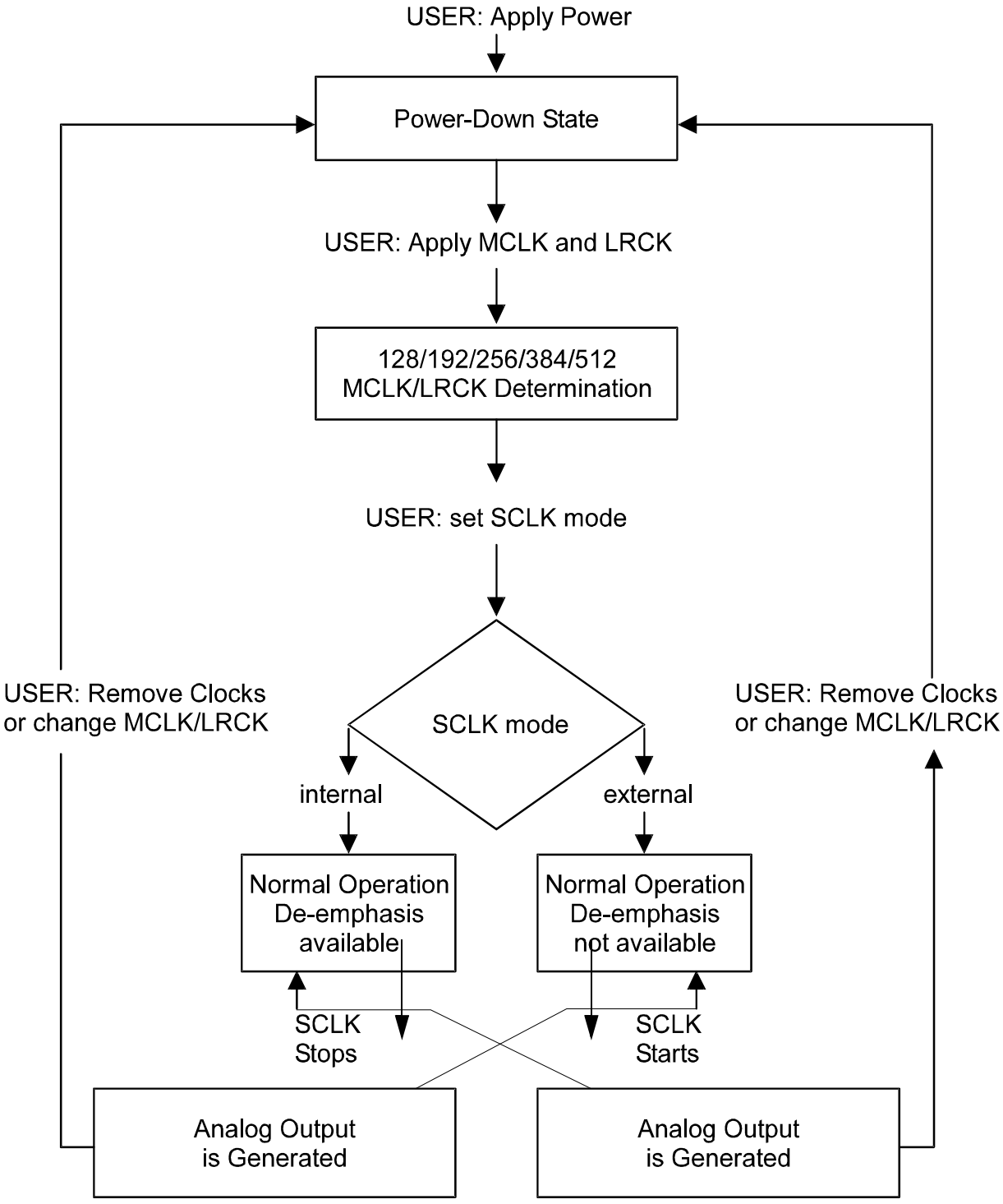


Figure 16. CS4334/5/6/7/8/9 Initialization and Power-Down Sequence

4.8 Overall Base-Rate Frequency Response

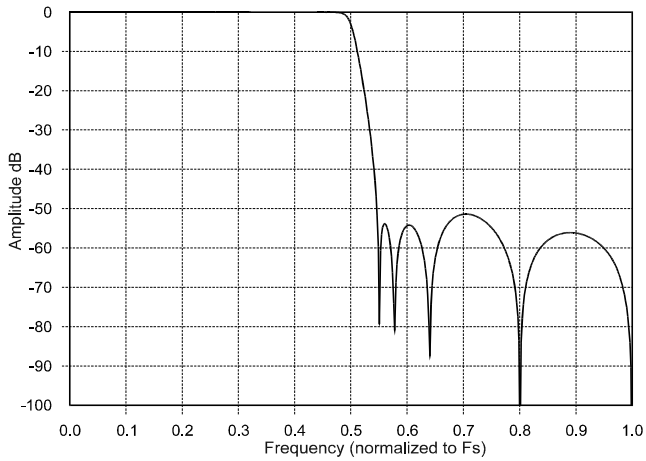


Figure 17. Stopband Rejection

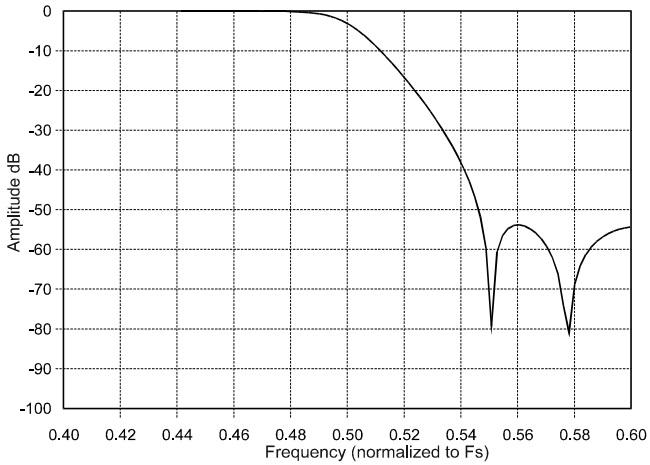


Figure 18. Transition Band

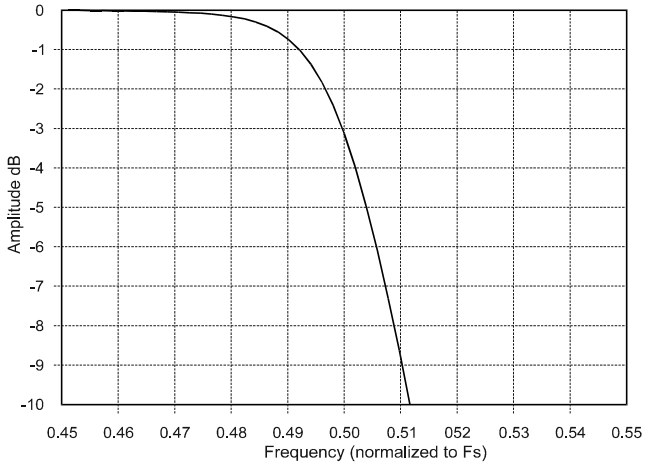


Figure 19. Transition Band

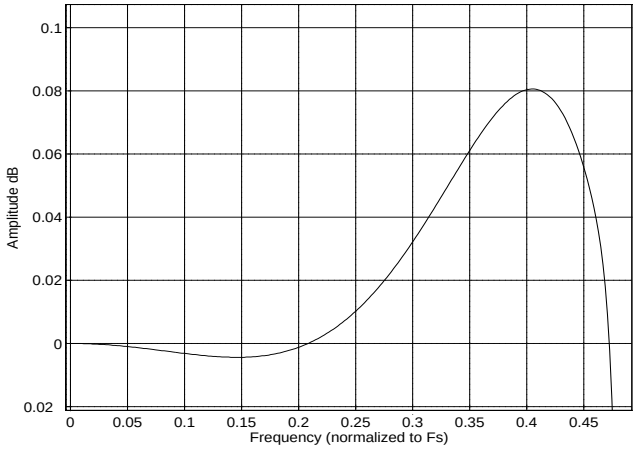


Figure 20. Passband Ripple

4.9 Overall High-Rate Frequency Response

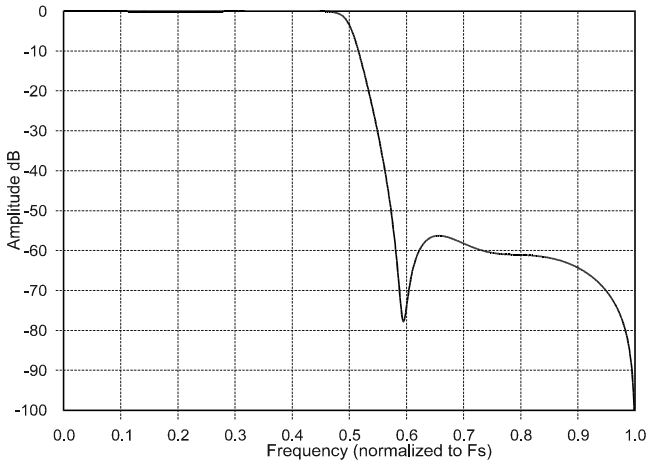


Figure 21. Stopband Rejection

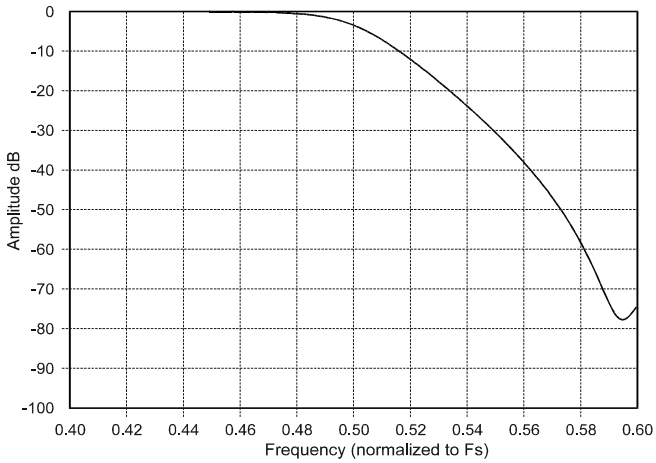


Figure 22. Transition Band

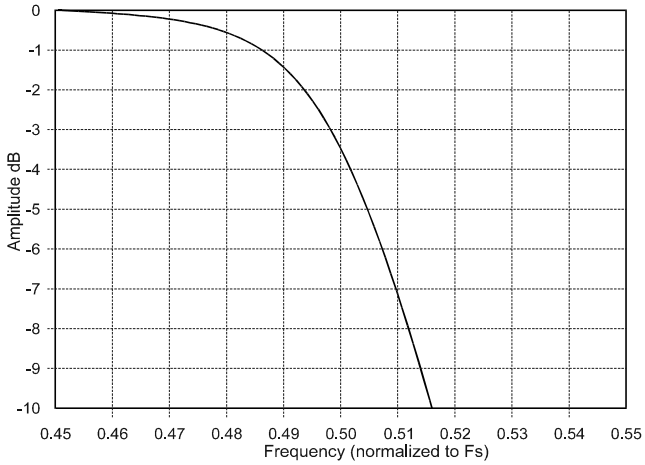


Figure 23. Transition Band

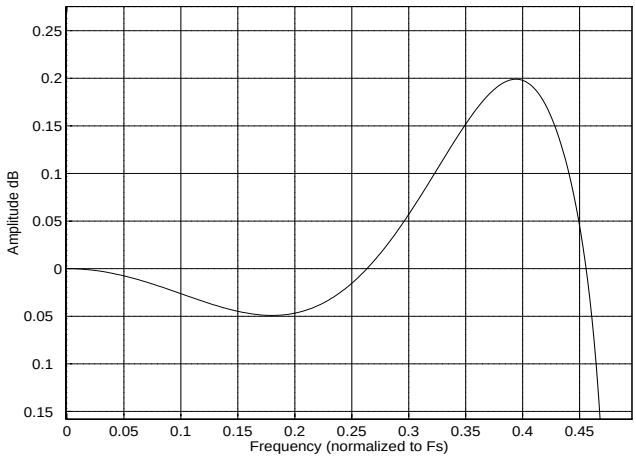
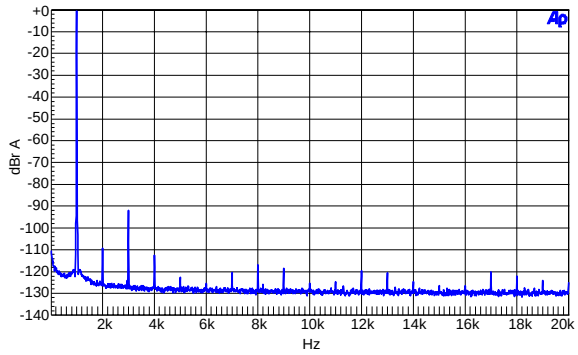


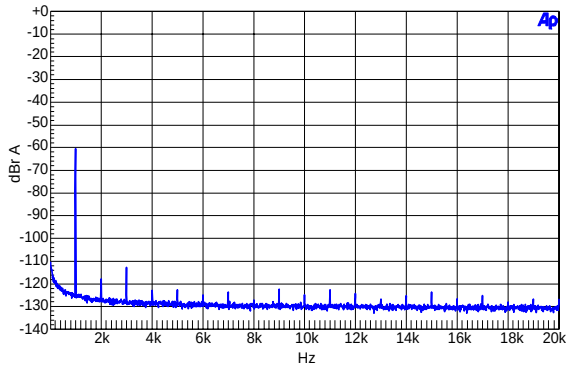
Figure 24. Passband Ripple

4.10 Base Rate Mode Performance Plots



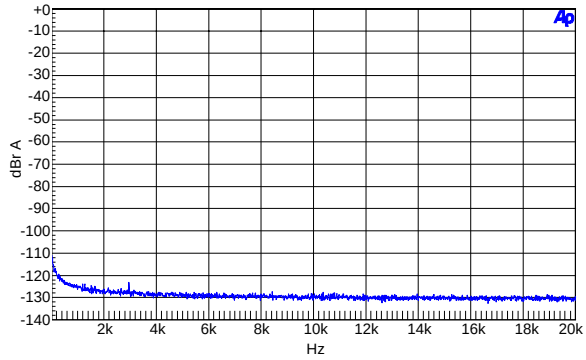
(16k FFT of a 1 kHz input signal)

Figure 25. 0 dBFS FFT (BRM)



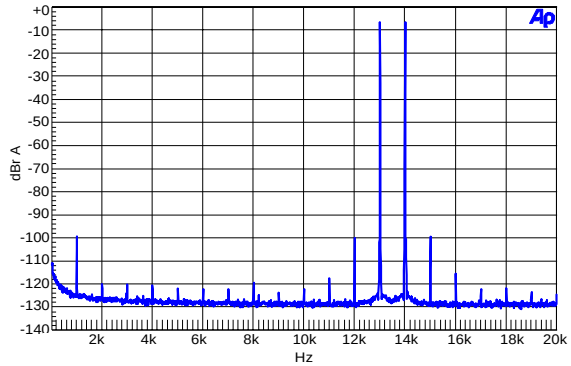
(16k FFT of a 1 kHz input signal)

Figure 26. -60 dBFS FFT (BRM)



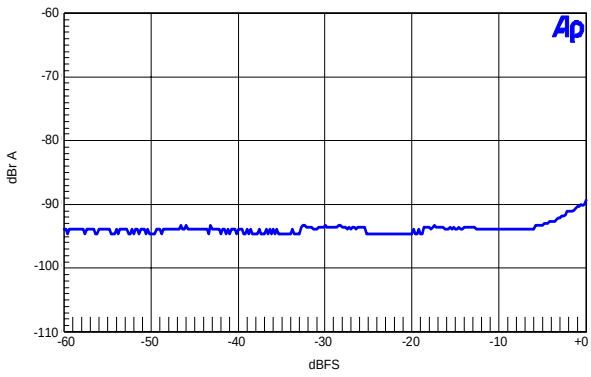
(16k FFT with no input signal)

Figure 27. Idle Channel Noise FFT (BRM)



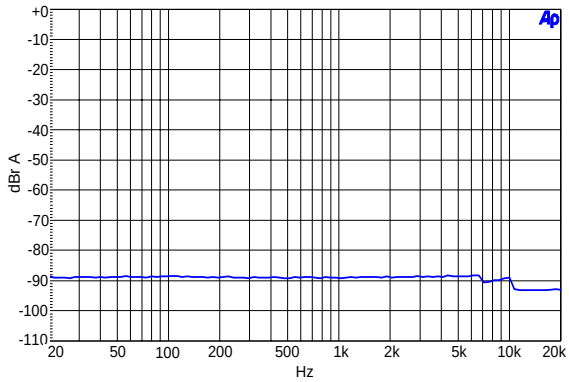
(16k FFT of intermodulation distortion using 13 kHz and 14 kHz input signals)

Figure 28. Twin Tone IMD FFT (BRM)



(THD+N plots measured using a 1kHz 24-bit dithered input signal)

Figure 29. THD+N vs. Amplitude (BRM)

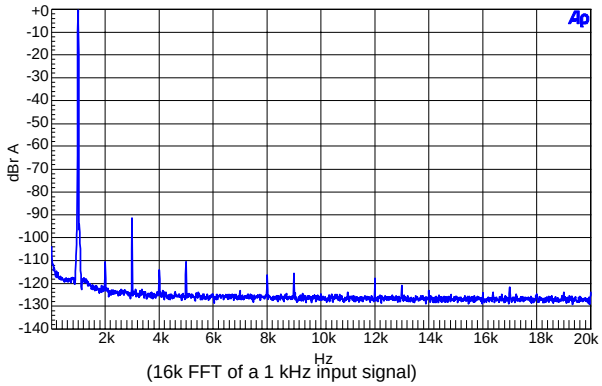


(THD+N plots measured using a 1kHz 24-bit dithered input signal)

Figure 30. THD+N vs. Frequency (BRM)

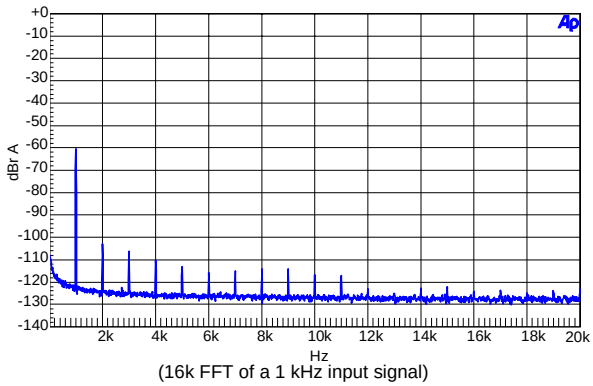
All measurements were taken from the CDB4334 evaluation board using the Audio Precision Dual Domain System Two Cascade.

4.11 High Rate Mode Performance Plots



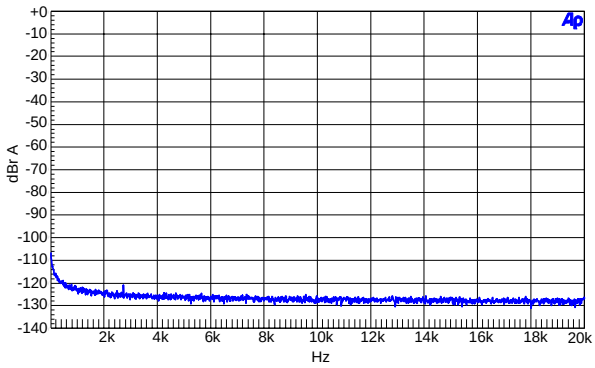
(16k FFT of a 1 kHz input signal)

Figure 31. 0 dBFS FFT (HRM)



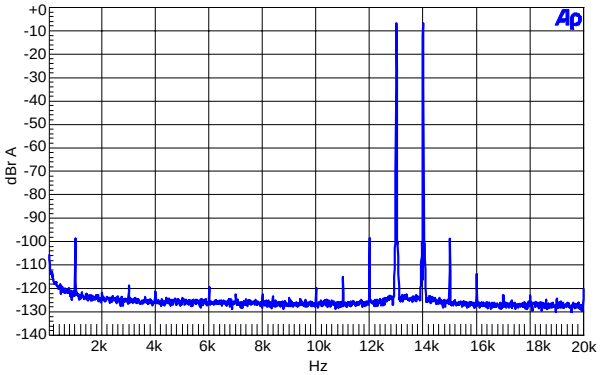
(16k FFT of a 1 kHz input signal)

Figure 32. -60 dBFS FFT (HRM)



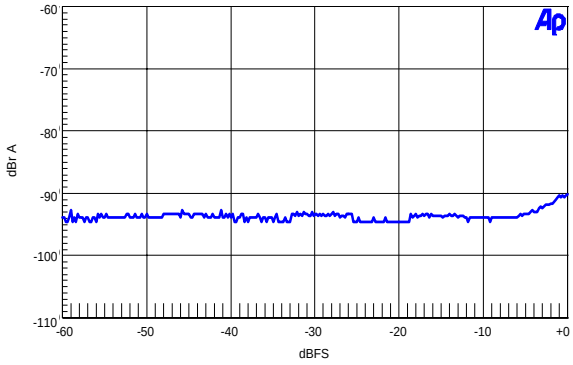
(16k FFT with no input signal)

Figure 33. Idle Channel Noise FFT (HRM)



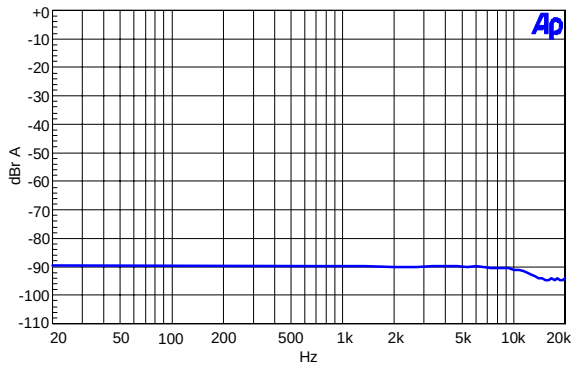
(16k FFT of intermodulation distortion using 13 kHz and 14 kHz input signals)

Figure 34. Twin Tone IMD FFT (HRM)



(THD+N plots measured using a 1kHz 24-bit dithered input signal)

Figure 35. THD+N vs. Amplitude (HRM)

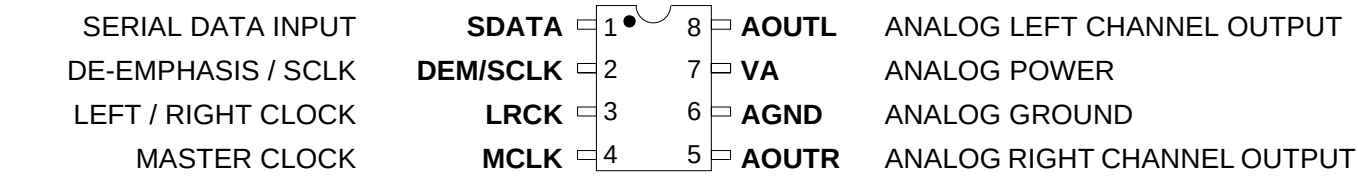


(THD+N plots measured using a 1kHz 24-bit dithered input signal)

Figure 36. THD+N vs. Frequency (HRM)

All measurements were taken from the CDB4334 evaluation board using the Audio Precision Dual Domain System Two Cascade.

5. PIN DESCRIPTIONS



No.	Pin Name	I/O	Pin Function and Description
1	SDATA	I	***Serial Audio Data Input*** - two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4334/5/6/7/8/9 via internal or external SCLK, and the channel is determined by LRCK.
2	DEM/SCLK	I	***De-Emphasis/External Serial Clock Input*** - used for de-emphasis filter control or external serial clock input.
3	LRCK	I	***Left/Right Clock*** - determines which channel is currently being input on the Audio Serial Data Input pin, SDATA.
4	MCLK	I	***Master Clock*** - frequency must be 256x, 384x, or 512x the input sample rate in BRM and either 128x or 192x the input sample rate in HRM.
5	AOUTR	O	***Analog Right Channel Output*** - typically 3.5 Vp-p for a full-scale input signal.
6	AGND	I	***Analog Ground*** - analog ground reference is 0V.
7	VA	I	***Analog Power*** - analog power supply is nominally +5V.
8	AOUTL	O	***Analog Left Channel Output*** - typically 3.5 Vp-p for a full-scale input signal.

6. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)- The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

7. REFERENCES

1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) CDB4334/5/6/7/8/9 Evaluation Board Datasheet

8. ORDERING INFORMATION:

Model	Temperature	Package	Serial Interface
CS4334-KS	-10 to +70 °C	8-pin Plastic SOIC	16 to 24-bit, I2S
CS4335-KS	-10 to +70 °C	8-pin Plastic SOIC	16 to 24-bit, left justified
CS4336-KS	-10 to +70 °C	8-pin Plastic SOIC	24-bit, right justified
CS4337-KS	-10 to +70 °C	8-pin Plastic SOIC	20-bit, right justified
CS4338-KS	-10 to +70 °C	8-pin Plastic SOIC	16-bit, right justified
CS4339-KS	-10 to +70 °C	8-pin Plastic SOIC	18-bit, right justified, 32 F_S Internal SCLK mode
CS4334-BS	-40 to +85 °C	8-pin Plastic SOIC	16 to 24-bit, I2S
CS4335-BS	-40 to +85 °C	8-pin Plastic SOIC	16 to 24-bit, left justified
CS4336-BS	-40 to +85 °C	8-pin Plastic SOIC	24-bit, right justified
CS4337-BS	-40 to +85 °C	8-pin Plastic SOIC	20-bit, right justified
CS4338-BS	-40 to +85 °C	8-pin Plastic SOIC	16-bit, right justified
CS4339-BS	-40 to +85 °C	8-pin Plastic SOIC	18-bit, right justified, 32 F_S Internal SCLK mode

9. FUNCTIONAL COMPATIBILITY

CS4330-KS ⇒ CS4339-KS

CS4331-KS ⇒ CS4334-KS

CS4333-KS ⇒ CS4338-KS

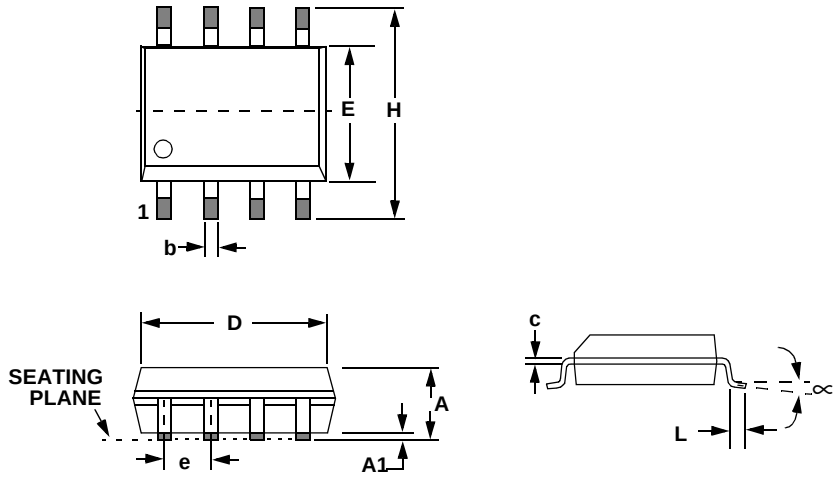
CS4330-BS ⇒ CS4339-BS

CS4331-BS ⇒ CS4334-BS

CS4333-BS ⇒ CS4338-BS

10. PACKAGE DIMENSIONS

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

• Notes •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