Building an IP Surveillance Camera System with a Low-Cost FPGA

WP-01133-1.0 White Paper

Current market trends in video surveillance present a number of challenges to be addressed, including the move from analog to digital cameras, conversion to high-definition (HD) video, adoption of Wide Dynamic Range (WDR) sensors, and Internet Protocol (IP) connectivity for control and data streams. This white paper describes the IP Surveillance Camera Reference Design and shows how the entire system is built using a low-cost Altera® Cyclone® III FPGA.

Introduction

In the video surveillance marketplace, the need for higher quality video, higher resolution, and more flexibility and features is driving the change from analog to digital cameras. By definition, high-definition (HD) video must be digital, so the adoption of HD standards is symbiotic with the move to digital sensors. The higher frame rates and resolution supported by HD video standards require newer compression techniques, such as H.264, which in turn require greater processing power in the camera.

The need to extract maximum image content in a wide range of lighting conditions (high and low light, high contrast) has led to digital cameras adopting a new class of WDR sensors, which require dynamic range compression within the camera, again in the digital domain. A further benefit of the digital data path in the camera is the possibility of performing "analytics" processing within the camera.

IP Surveillance Camera Reference Design

Figure 1 shows the top-level block diagram and hardware of the IP Surveillance Camera Reference Design, which targets the new generation of HD (>1 MP) WDR sensors. The IP Surveillance Camera Reference Design combines hardware and software intellectual property from Altera and a number of partners.

Figure 1. Block Diagram of IP Surveillance Camera Reference Design

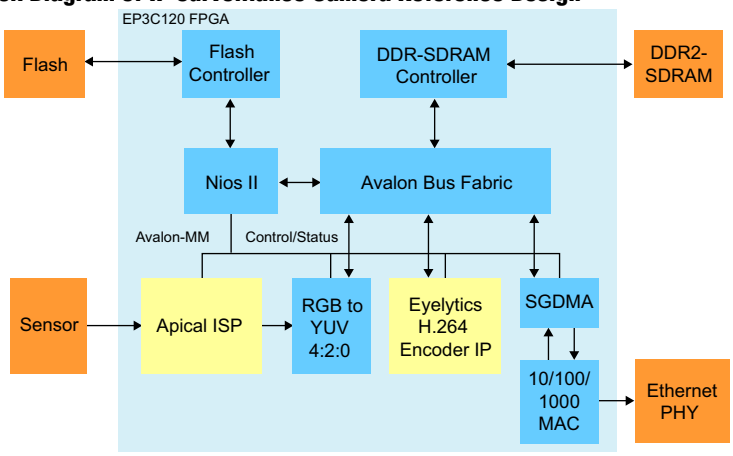
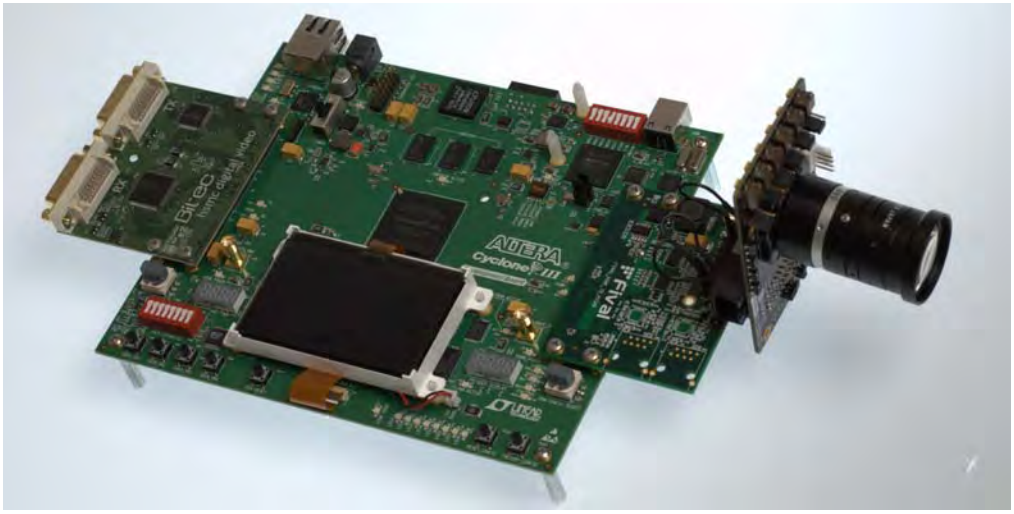


Figure 2 shows the hardware platform for the reference design, based around the Cyclone III EP3C120 development board. Pixel data from Aptina's WDR sensor is fed into the Image Sensor Pipeline (ISP) from Apical. The output data is YUV4:2:0 format and written to a frame buffer in the external DDR2 SDRAM using components from Altera's Video and Image Processing (VIP) suite. Video data then is encoded in H.264 format using a core from EyeLytics, and supporting (in this application) baseline/main profile level 3 for streaming via Ethernet to be viewed on a remote host. A Scatter-Gather Direct Memory Access (SGDMA) controller supports Altera's Triple-Speed Ethernet (TSE) MegaCore® function for streaming the encoded video to a remote client over Ethernet.

Figure 2. IP Surveillance Camera Reference Design Hardware



Wide Dynamic Range Sensor

The Aptina MT9M033 is a 0.33" 720p60 WDR CMOS sensor targeted for use in the surveillance camera market. The sensor and lens assembly are mounted on a "headboard," which is then connected via an I/O transposer board to the Cyclone III EP3C120 development board.

Image Sensor Pipeline

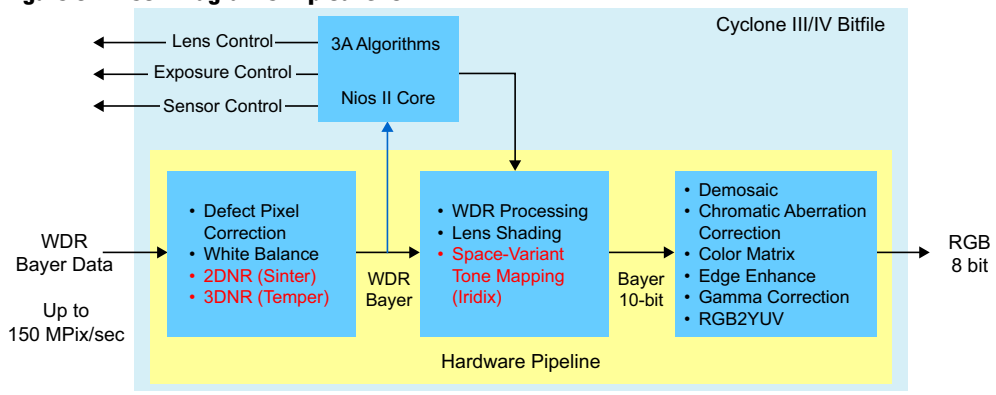
CMOS WDR sensors have no on-chip image pipeline processing and output the image data in RAW/Bayer format at up to 20 bits per pixel. The large amount of raw data coming from the sensor can be computed as:

20 bits/pixel x (1280 x 720) pixels/frame x 60 frames/s = >1 Gbit/s

This large amount of data makes it difficult to connect the new generation of WDR sensors to the ASSPs commonly used in surveillance solutions. Therefore, FPGAs are the ideal choice for efficient processing of this data. Apical's ISP (Figure 3) includes the following functions:

- Hot pixel removal and noise reduction (spatial and temporal IP cores are available)
- Advanced per pixel tone mapping using Apical's award-winning and patented Iridix IP core
- Advanced demosaic and color correction

Figure 3. Block Diagram of Apical's ISP



Compared to the unprocessed image in Figure 4 (top), the image in Figure 4 (bottom) shows how the Iridix core allows the maximum detail to be extracted from a high-contrast scene. In particular, the dark areas are revealed without corresponding overexposure in the bright areas.

Figure 4. Effect of Apical's ISP on High-Contrast Scenes

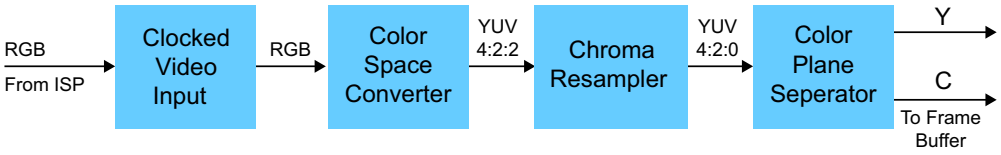
The output of the ISP is available as an option from the reference design through a Bitec DVI output board connected to the second HSMC connector on the Cyclone EP3C120 development board (shown on the left of the hardware shown in Figure 2).

Video and Image Processing Suite

The Altera® VIP Suite is a collection of MegaCore functions that designers can use to facilitate the development of custom video- and image-processing designs. The VIP Suite features MegaCore functions that range from simple building block functions, such as color space conversion, to sophisticated video scaling functions that can implement programmable polyphase scaling. These functions are suitable for use in a wide variety of image-processing and display applications, such as video surveillance, broadcast, video conferencing, and medical and military imaging.

In the IP Surveillance Camera Reference Design, a number of VIP cores are used for color space conversion and chroma resampling to convert the RGB encoded video from the ISP to the YUV 4:2:0 encoded input requirement of the H.264 encoder. The cores used, shown in Figure 5, are interconnected with Avalon® Streaming (Avalon-ST) interfaces overlaid with the Avalon-ST video protocol. The Y and C video components are written to a frame buffer in the external DDR2 memory using Avalon Memory-Mapped (Avalon-MM) interfaces.

Figure 5. Conversion and Resampling of Processed Sensor Image

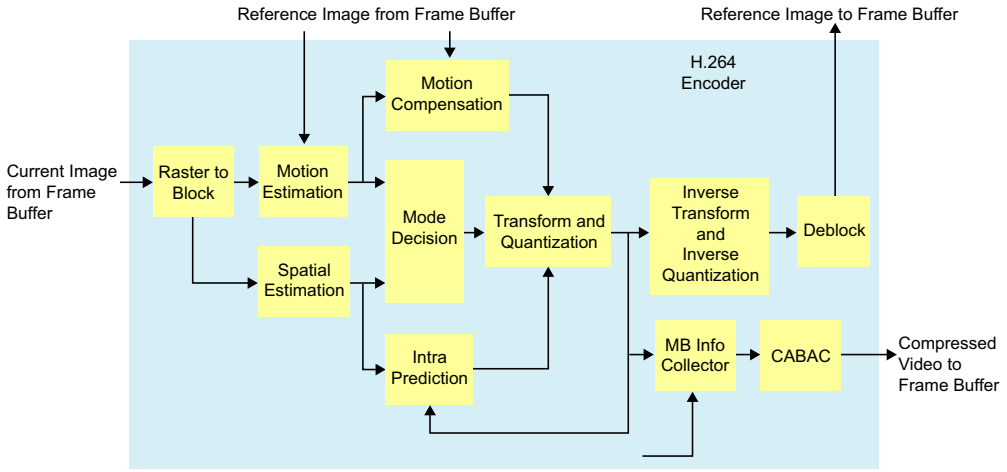


The sensor frame rate of 720p60 is converted to 720p30 before H.264 encoding by skipping alternate frames of video, in the frame buffer writer, by not writing them to the frame buffer.

Video Compression

The H.264 Encoder (Figure 6) used in this design is an IP core available from EyeLytics that has been optimized for surveillance applications. This core contains many surveillance features, including multichannel support, constant quality rate control, intra-/intermodes, QPEL, context-adaptive binary arithmetic coding (CABAC)/context-adaptive variable-length coding (CAVLC), and a low gate count. The core supports both main and baseline profiles.

Figure 6. H.264 Encoder Architecture



Triple-Speed Ethernet MAC

Altera's TSE MegaCore function combines the features of a 10-/100-/1000-Mbps Ethernet media access controller (MAC) and a 1000BASE-X physical coding sublayer (PCS) with an optional physical medium attachment (PMA). The Cyclone III EP3C120 development board includes a 10/100/1000 base-T, auto-negotiating Ethernet PHY with reduced-Gigabit media-independent interface (RGMII) connection to the TSE function.

Avalon Bus Fabric and DDR2 Frame Buffer Memory

A single bank of external DDR2 SDRAM with a 32-bit data bus running at 150 MHz and controlled by Altera's DDR and DDR2 SDRAM High-Performance II Controller MegaCore Functions is used for application code and data storage, input and output frame buffers, and intermediate frame buffers for the H.264 encoder. To meet timing and performance targets, the Avalon-MM bus fabric is 128 bits wide running at 75 MHz. Avalon arbitration shares are applied to each Avalon-MM bus master connection to the DDR2 memory controller to guarantee efficient and uninterrupted access for bursts of data to and from the H.264 encoder.

☞ A number of standard Avalon components, such as clock crossing bridges, timers and parallel I/Os, are used to complete the system. For the sake of simplification, these are not shown in Figure 6.

Tool Flow

The IP Surveillance Camera Reference Design is implemented as a complete system on a chip (SOC) using Altera's SOPC Builder tool. Using SOPC Builder, the designer specifies the system components in a GUI, and SOPC Builder generates the interconnect logic automatically. SOPC Builder generates HDL files that define all components of the system, and a top-level HDL file then connects all the components together. The IP Surveillance Camera Reference Design is generated in Verilog HDL, but SOPC Builder can generate both Verilog HDL or VHDL.

The ISP and the H.264 encoder are available as SOPC Builder components with Avalon-MM interfaces, allowing them to be easily integrated into a system with standard peripherals available from Altera, as well as third-party IP and the designer's own components.

SOPC Builder is included in Altera's Quartus® II development software, which provides a complete, multiplatform design environment that easily adapts to specific design needs. Quartus II software includes solutions for all phases of FPGA and CPLD design:

- Design entry
- Synthesis
- Place and route
- Timing analysis
- Simulation
- Programming and configuration

Software development is performed using Altera's Nios® II Embedded Design Suite. A board support package (BSP) is generated including all the necessary device drivers, based on the components that were included in the SOPC Builder design.

Software Applications

A Nios II embedded processor is used for programming the various registers within the different modules as well as for running the RTP stack to stream the compressed video. Working with the Ethernet MAC module to control the ISP, the embedded processor runs the uC/OS-II real time kernel from Micrium, NicheStack and RTP stack from InterNiche Technologies, and a video-streaming application and a web-server application from Altera's reference deisgn . The processor also handles auto exposure and auto white balance control of the ISP.

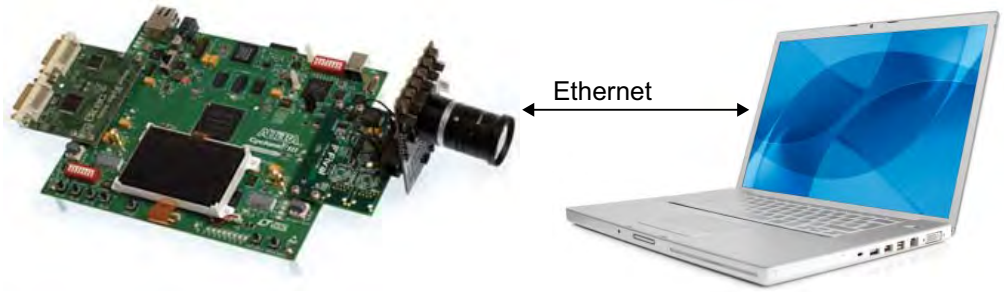
The video-streaming application responds to interrupts from the H.264 encoder and reloads various buffer pointers. Reloading allows it to prepare for the next video frame to be encoded and for the just encoded frame to be passed to the RTP stack for onward transmission via Ethernet.

The web-server application allows simple control of the ISP to switch the sensor between normal and WDR mode and to enable and disable Iridix. This control allows the benefits of the ISP to be shown in real time. The web-server application also allows configuration of the encoder, including bitrate, quality, and selecting between CABAC and CAVLC.

Host Software

A host PC running VLC media player (or similar) is used to view the streamed video output of the IP Surveillance Camera Reference Design. As shown in Figure 7, the only required connection between the host and the EP3C120 development kit is an Ethernet cable.

Figure 7. Host Connection to IP Surveillance Camera Reference Design Kit



Performance

Performance metrics of the IP Surveillance Camera Reference Design comprise speed, latency, power consumption, and resource utilization numbers.

Speed

When implemented on a Cyclone III EP3C120I7 development board, the reference design runs with a DDR clock frequency of 150 MHz, sufficient to compress frames of 720p30 video using a H.264 baseline or main profile. The Avalon-MM bus fabric runs at 75 MHz, and the H.264 encoder core runs at 150 MHz. The DDR2 memory controller, Avalon-MM bus fabric, and H.264 core are connected through synchronous half rate bridges to minimize latency between the clock domains.

The Nios II processor and TSE are clocked at 125 MHz. The Nios II processor is implemented as the Nios II/F (fast) version with an 8-Kbyte instruction cache, 8-Kbyte data cache, and floating point support.

Latency

The latency from the sensor input to the ISP to the output of the H.264 encoder is less than two frames, and comes about from the double buffering of the image data. A new input frame is always being written to memory while the previous frame is being encoded.

Power Consumption

The total power consumption of the reference design including all of the ancilliary blocks and I/O is 2.7 W. Table 1 shows the power consumption for each of the major blocks used in the reference design. The remaining 700mW are consumed by the Avalon bus fabric, color space conversion, and I/Os ancillary to the reference design.

Table 1. Power Consumption in Blocks

Block	Power Consumption (mW)
H.264	944
ISP	578
DDR2	311
Nios II CPU	88
TSE MAC	83

Resource Utilization

When implemented in a Cyclone EP3C120, the resource utilization for the complete reference design is:

- 107K logic elements (LEs) (90% device utilization)
- 410 M9K embedded memories (95% device utilization)
- 140 embedded multiplier 9-bit elements (24% device utilization)

Table 2 lists specific block resource utilizations.

Table 2. Specific Resource Utilization

Block	LE Usage	M9K Usage
Apical ISP	41K	127
EyeLytics H.264 core	35K	225
Remaining system (e.g., Nios II core, DDR2 Controller, TSE, etc.)	31K	58

Table 3 lists I/O usage.

Table 3. I/O Usage

Interface	I/O
ISP	20 for parallel sensor interface with 12-bit data
DDR2 SDRAM High-Performance II	64 with 32-bit datapath
TSE	16
Flash	46with 16-bit datapath
Clocks and reset	3
Additional	Other I/Os are used for switches, LEDs, etc., which are ancillary to the IP Surveillance Camera Reference Design

Flexibility

An FPGA-based architecture is completely flexible and customizable, while at the same time offering the peace of mind that comes from using a standard, well-understood silicon platform. This flexibility allows the system architecture to be enhanced and modified to suit different system requirements. Increasing camera resolution or adding custom video processing or a video analytics engine is easy because the design is implemented with standard HDL. Furthermore, it is possible to deploy upgrades remotely over the Ethernet. For example, a new FPGA programming file can be sent to the Nios II embedded processor, which then writes the file to flash memory, thus reconfiguring the system or changing the sensor or ISP settings.

Integrating the complete IP Surveillance Camera Reference Design onto a single FPGA results in a reduction of chip count and saving of PCB real estate. The reduction in I/O connections by not requiring communication with external devices reduces dynamic power consumption, thus easing any thermal management issues. Multiple camera personalities can be supported with a single system design, using different FPGA images for each personality (e.g., resolution, frame rate, compression options). Vertical migration allows devices of different logic density to be used within the same package footprint.

Since the design can be targeted to any Altera FPGA, adopting an open design allows the designer to target the newest FPGA, thus receiving the higher performance and lower cost/power ratios as newer FPGA families are introduced.

Conclusion

The challenges facing the designers of state- of-the-art IP surveillance systems are addressed by Altera with its Cyclone III and Cyclone IV family of low-cost FPGAs. With the IP Surveillance Camera Reference Design, Altera and its partners provide a complete solution, from image capture to IP encapsulation, using a range of MegaCore functions integrated with Altera's SOPC Builder tool to provide a scalable solution and rapid time to market.

Further Information

- Video Surveillance:
  www.altera.com/surveillance
- Video: "Easily Support WDR CMOS Image Sensor Processing with Low-Cost FPGAs":
  www.altera.com/education/webcasts/videos/videos-image-processing-fpgas.html
- Request a demonstration or evaluation of the IP Surveillance Camera Reference Design:
  mailto:videosurveillance@altera.com
- Video and Image Processing (VIP) Suite MegaCore Functions:
  www.altera.com/products/ip/dsp/image_video_processing/m-alt-vipsuite.html
- Triple Speed Ethernet (TSE) IP Core Resource Center:
  www.altera.com/support/ip/interface-protocols/ips-inp-tse.html
- DDR and DDR2 SDRAM High-Performance II Controller MegaCore Functions:
  www.altera.com/products/ip/iup/memory/m-alt-hpddr2.html
- Nios II Embedded Design Suite:
  www.altera.com/support/ip/processors/nios2/tools/ni2-development_tools.html
- EyeLytics Inc:
  www.eyelytics.com
- Apical Limited
  www.apical-imaging.com
- Aptina Imaging:
  www.aptina.com
- Bitec:
  www.bitec.ltd.uk
- Micrium:
  www.micrium.com
- InterNiche Technologies:
  www.iniche.com
- VLC Media Player:
  www.videolan.org/vlc

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Document Revision History

Table 4 shows the revision history for this document.

Table 4. Document Revision History

Date	Version	Changes
June 2010	1.0	Initial release.