AL440B Data Sheets

Version 1.0

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Amendments

11-28-01 AL440B version 1.0 release data sheets.

AL440B 4MBits FIFO Field Memory

Contents:

1.0 Description

The AL440B 4Mbits (512k x 8-bit) FIFO memory provides completely independent 8bit input and output ports that can operate at a maximum speed of 80 MHz. The built-in address and pointer control circuits provide a very easy-to-use memory interface that greatly reduces design time and effort. Manufactured using state-of-the-art embedded high density memory cell array, the AL440B uses high performance process technologies with extended controller functions (write mask, read skip.. etc.), allowing easy operation of non-linearity and regional read/write FIFO for PIP, Digital TV, security system and video camera applications. The status flags can be used to indicate Fullness/Emptiness of the FIFO and also allow multiple cascading AL440Bs to expand the storage depth or provide a longer delay, which cannot be achieved with only a single device. Expanding AL440B data bus width is also possible by using multiple AL440B chips in parallel. To get better design flexibility, the polarities of the AL440B control signals are selectable. The read and write control signals, such as Read/Write Enable, Input/Output Enable.., can be either active low or high by pulling /PLRTY signal to high or low respectively. In AL440B, Window data write/read and data mirroring functions can offer better control assistance in the application design. The built-in registers set can be easily programmed via serial bus (I2C like control bus) to perform various useful functions such as multi-freeze, P-in-P in the digital TV, VCR, and video camera application.

Available as a 44-pin TSOP (II), the small footprint allows product designers to keep real estate to a minimum.

2.0 Features

- 4Mbits (512k x 8 bits) organization FIFO
- Independent 8bit read/write port operations (different read/write data rates acceptable)
- Maximum Read/write cycle time: 80Mhz and 40Mhz (2 speed grades)
- Input Enable (write mask) / Output Enable (data skipping) control
- Window read/write with Mirroring capable
- Selectable control signal polarity
- Input Ready / Output Ready flags
- Direct cascade connection
- Self refresh
- 3.3V ± 10% power supply
- Standard 44-pin TSOP (II) package

3.0 Applications

- Multimedia systems
- Video capture or editing systems for NTSC/PAL or SVGA resolution
- Security systems
- Scan rate converters
- PIP (Picture-In-Picture) video display
- TBC (Time Base Correction)
- Frame synchronizer
- Digital video camera
- Hard disk cache memory
- Buffer for communication systems

* 80MHz High-Speed version

- DTV/HDTV video stream buffer

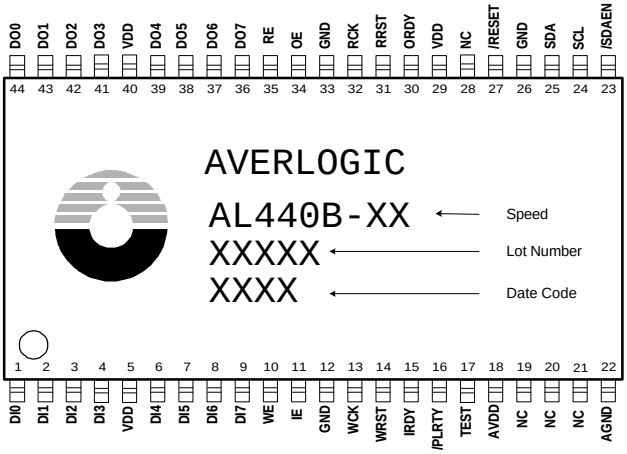
4.0 Ordering Information

The AL440B has two speed grades, AL440B-24 and AL440B-12, which can operate at frequencies of 40MHz and 80MHz respectively. Both speed grades are powered by 3.3V and are available in a 44-pin standard TSOP-II package.

Part number	Package	Power Supply	Status
AL440B-24 (40MHz)	44-pin plastic TSOP(II)	+3.3V±10%	Sample Dec., 2001
AL440B-12 (80MHz)	44-pin plastic TSOP(II)	+3.3V±10%	Sample Dec.., 2001

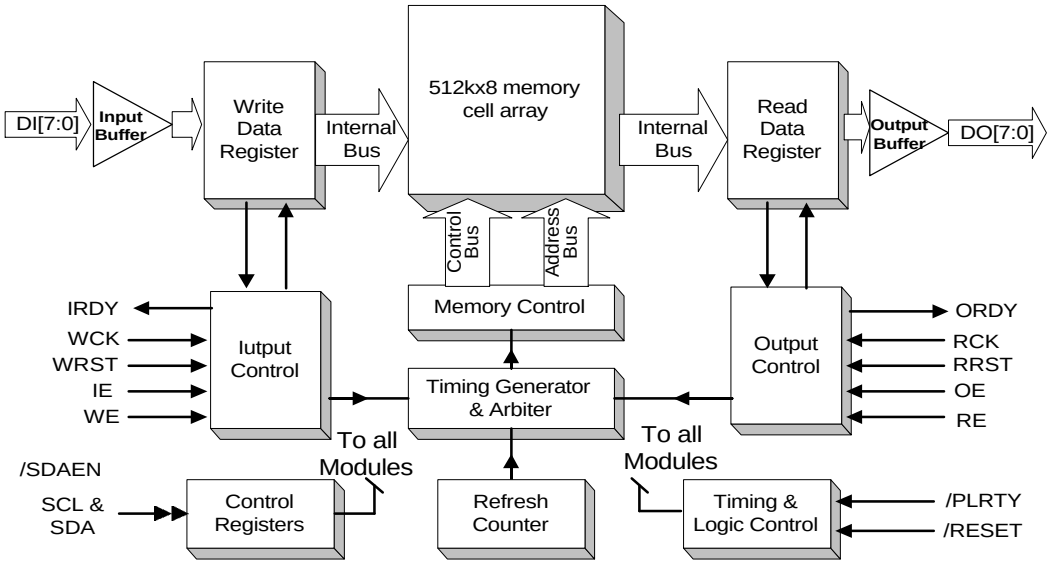
5.0 Pin-out Diagram

The AL440B pin-out diagram is following.



AL440B-12/24 TSOP (II) pinout diagram (Top view)

6.0 Block Diagram



AL440B Block Diagram

The internal structure of the AL440B consists of an Input/Output buffers, Write Data Registers, Read Data Registers and main 512k x8 memory cell array and the state-of-the-art logic design that takes care of addressing and controlling the read/write data.

7.0 Pin Definition and Description

The pin definitions and descriptions are as follows:

Write Bus Signals

Pin name	Pin number	I/O type	Description
DI[7:0]	9,8,7,6,4,3,2, 1	I	The DI pins input 8bits of data. Data input is synchronized with the WCK clock. Data is acquired at the rising edge of WCK clock.
WE	10	I	WE is an input signal that controls the 8bit input data write and write pointer operation.
IE	11	I	IE is an input signal that controls the enabling/ disabling of the 8bit data input pins. The internal write address pointer is always incremented at rising edge of WCK by enabling WE regardless of the IE level.
WCK	13	I	WCK is the write clock input pin. The write data input is synchronized with this clock.
WRST	14	I	The WRST is a reset input signal that resets the write address pointer to 0.
IRDY	15	O	IRDY is a status output flag that reports the FIFO space availability.

*Note: For the polarity definition of all write control signals (WE, IE, WRST and IRDY), please refer to /PLRTY pin definition and “Memory Operation” section for details.

Read Bus Signals

Pin name	Pin number	I/O type	Description
DO[7:0]	36,37,38,39, 41,42,43,44	O	The DO pins output 8bit of data. Data output is synchronized with the RCK clock. Data is output at the rising edge of the RCK clock.
RE	35	I	RE is an input signal that controls the 8bit output data read and read pointer operation.
OE	34	I	OE is an input signal that controls the enabling/ disabling of the 8bit data output pins. The internal read address pointer is always incremented at rising edge of RCK by enabling RE regardless of the OE level.
RCK	32	I	RCK is the read clock input pin. The read data

			output is synchronized with this clock.
RRST	31	I	The RRST is a reset input signal that resets the read address pointer to 0.
ORDY	30	O	ORDY is a status output flag that reports the FIFO data availability.

*Note: For the polarity definition of all read control signals (RE, OE, RRST and ORDY), please refer to /PLRTY pin definition and "Memory Operation" section for details.

Serial Port Bus Signals

Pin name	Pin number	I/O type	Description
SDA	25	I/O	SDA carries the serial bus read/write data bits. The SDA data bit is valid when the SCL is high after start up sequence.
SCL	24	I	SCL supplies the serial bus clock signal to FIFO. The serial data bit is valid when the SCL is high after start up sequence.
/SDAEN	23	I	/SDAEN controls the enabling/disabling of serial bus interface. When /SDAEN is high, the serial interface is disabled and SDA pin is high impedance. When /SDAEN is low, the serial interface is enabled and data can be written to or read from the FIFO registers.

Power/Ground Signals

Pin name	Pin number	I/O type	Description
V_{DD}	5, 29, 40	-	3.3V ± 10%.
GND	12, 26, 33	-	Ground.
AV_{DD}	18	-	Dedicated power pin for the internal oscillator. 3.3V ± 10%.
AGND	22	-	Dedicated ground pin for the internal oscillator.

Miscellaneous Signals

Pin name	Pin number	I/O type	Description
/RESET	27	I	The global reset pin /RESET will automatically initialize chip logic. For the recommended circuit for the global reset signal, please refer to the Application Notes.

/PLRTY	16	I	Select active polarity of the control signals including WE, RE, WRST, RRST, IE, OE, IRDY and ORDY totally 8 signals /PLRTY = V_{DD}, active low. /PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VDD or GND. If /PLRTY level is changed during memory operation, memory data is not guaranteed.
TEST	17	I	For testing purpose only. No connect or connect to Ground.
NC	19,20,21,28	-	No connect or connect to Ground

8.0 Register Definition

There are some built-in registers in the AL440B that allows performing some optional functions such as window read/write access. These registers can be programmed via serial bus (SDA, SCL and /SDAEN). The serial bus interface protocol is illustrated in "Serial Bus Interface" chapter. The serial bus control software code or tool is available at Averlogic Technologies, Inc. upon request.

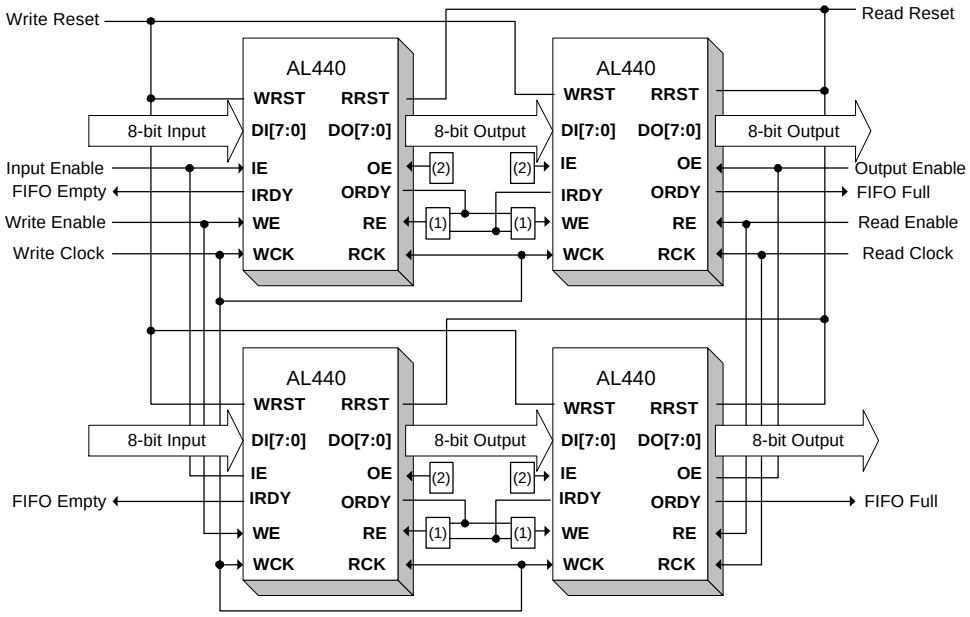
8.1 Register Set

Address	Register	R/W	Description
00h	COMPANYID	R	Company ID (46h)
02h	WSTART_L	R/W	Window write starting address (Low byte)
03h	WSTART_H	R/W	Window write starting address (High byte)
04h	WXSIZE_L	R/W	Window write horizontal size (Low byte)
05h	WXSIZE_H	R/W	Window write horizontal size (High byte)
06h	WSTRIDE_L	R/W	Window write strike size (Low byte) 2's complement (for Y-mirror)
07h	WSTRIDE_H	R/W	Window write strike size (High byte) 2's complement (for Y-mirror)
08h	WYSIZE_L	R/W	Window write vertical size (Low byte)
09h	WYSIZE_H	R/W	Window write vertical size (High byte)
0Ah	WWCTRL	R/W	Window write control register [7]: enable window write function [6]: X mirror [5]: freeze
0Bh	RSTART_L	R/W	Window read starting address (Low byte)
0Ch	RSTART_H	R/W	Window read starting address (High byte)
0Dh	RXSIZE_L	R/W	Window read horizontal size (Low byte)
0Eh	RXSIZE_H	R/W	Window read horizontal size (High byte)
0Fh	RSTRIDE_L	R/W	Window read strike size (Low byte)
10h	RSTRIDE_H	R/W	Window read strike size (High byte)
11h	RYSIZE_L	R/W	Window read vertical size (Low byte)

12h	RYSIZE_H	R/W	Window read vertical size (High byte)
13h	RWCTRL	R/W	Window read control register [7]: enable window read function

9.0 Multiple Devices Bus Expansion and Cascading

The AL440B FIFO memory can be applied to very wide range of media applications. A parallel connect or cascade of multiple AL440B FIFOs provides FIFO bus width or memory depth expansion for some applications; eg. accommodating HDTV resolution.. etc.



(1) Logic Block: "OR" Gate if /PLTY = HIGH, "AND" Gate if /PLTY = HIGH
(2) Always Enabled : Tie to LOW if /PLTY = HIGH, Tie to High if /PLTY = LOW

AL440B Expanding & Cascading

10.0 Serial Bus Interface

The serial bus interface consists of the SCL (serial clock), SDA (serial data) and /SDAEN (serial interface enable) signals. There are pull up circuit internally for both SCL and SDA pins. When /SDAEN is high, the serial bus interface is disabled and both SCL and SDA pins are pulled high. When /SDAEN is low, the serial bus interface is enabled and data can be written into or read from the AL440B register set. For both read and write, each byte is transferred MSB first and LSB last, and the SDA data bit is valid when the SCL is pulled high. The serial bus control sample C code is available in Averlogic Technologies, Inc. upon request.

The read/write command format is as follows:

Write: <S> <Write SA> <A> <Register Index> <A> <Data> <A> <P>

Read: <S> <Write SA> <A> <Register Index> <A> <S> <Read SA> <A> <Data> <NA> <P>

Following are the details:

<**S**>:
Start signal

SCL	SDA
High	High
High	Low

The Start signal is HIGH to LOW transition on the SDA line when SCL is HIGH.

<**WRITE SA**>:
Write Slave Address: 0h

<**READ SA**>:
Read Slave Address: 1h

<**REGISTER INDEX**>:
Value of the AL440B register index.

<**A**>:
Acknowledge stage
The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) for the AL440B (slave) to pull down the SDA line during the acknowledge clock pulse.

<**NA**>:
Not Acknowledged stage
The acknowledge-related clock pulse is generated by the host (master). The host releases the SDA line (HIGH) during the acknowledge clock pulse, but the AL440B does not pull it down during this stage.

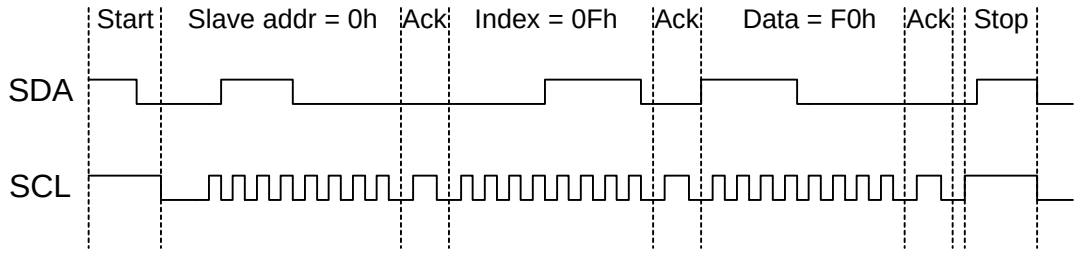
<**DATA**>:
Data byte write to or read from the register index.
In read operation, the host must release the SDA line (high) before the first clock pulse is transmitted to the AL440B.

<**P**>:
Stop signal

SCL	SDA
High	Low
High	High

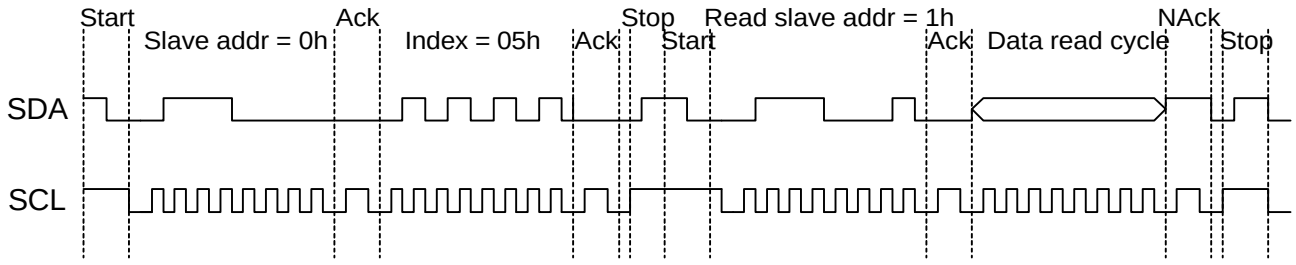
The Stop signal is LOW to HIGH transition on the SDA line when SCL is HIGH.

Suppose data F0h is to be written to register 0Fh using write slave address 0h, the timing is as follows:



AL440B Serial bus Write timing

Suppose data is to be read from register 05h using read slave address 1h, the timing is as follows:



AL440B Serial bus read timing

11.0 Memory Operation

11.1 Power-On-Reset & Initialization

During the system power on, a 200µs negative pulse on the /RESET pin is required and will automatically initialize chip logic. Apply a valid reset pulse to WRST and RRST after power-on-reset to reset read/write address pointer to zero.

11.2 WRST, RRST Reset Operation

The reset signal can be given at any time regardless of the WE, RE and OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again.

11.3 Control Signals Polarity Select

The AL440B provides the option for operating polarity on controlling signals. With this feature the application design can benefit by matching up the operation polarity between AL440B and an existing interfacing devices without additional glue logic. The operating polarity of control signals WE, RE, WRST, RRST, IE, OE, IRDY and ORDY are controlled by /PLRTY signal. When /PLRTY is pulled high all 8 signals will be active low. When /PLRTY is pulled low all 8 signals will be active high.

11.4 FIFO Write Operation

In the FIFO write operation, 8 bits of write data are input in synchronization with the WCK clock. The FIFO write operation is determined by WRST, WE, IE and WCK signals and the combination of these signals could produce different write result. The /PLRTY signal determines the activated polarity of these control signals. The following tables describe the WRITE functions under different operating polarities.

/PLRTY = VDD

WRST	WE	IE	WCK	Function
L	-	-	↑	Write reset. The write pointer is reset to zero.
H	L	L	↑	Normal Write operation.
H	L	H	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
H	H	-	↑	Write operation stopped. Write address pointer is also stopped.

/PLRTY = GND

WRST	WE	IE	WCK	Function
H	-	-	↑	Write reset. The write pointer is reset to zero.
L	H	H	↑	Normal Write operation.
L	H	L	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
L	L	-	↑	Write operation stopped. Write address pointer is also stopped.

11.5 FIFO Read Operation

In the FIFO read operation, 8 bits of read data are available in synchronization with the RCK clock. The access time is stipulated from the rising edge of the RCK clock. The FIFO read operation is determined by RRST, RE, OE and RCK signals, so the combination of these signals could produce varying read results. The /PLRTY signal could decide the activated polarity of these control signals. The following tables describe the READ functions under different operating polarities.

/PLRTY = VDD

RRST	RE	OE	RCK	Function
L	L	L	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
L	L	H	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
L	H	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.

L	H	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
H	L	L	↑	Normal Read operation.
H	L	H	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
H	H	L	↑	Read address pointer is stopped. Output data is held.
H	H	H	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

/PLRTY = GND

RRST	RE	OE	RCK	Function
H	H	H	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
H	H	L	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
H	L	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.
H	L	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
L	H	H	↑	Normal Read operation.
L	H	L	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
L	L	H	↑	Read address pointer is stopped. Output data is held.
L	L	L	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

When the new data is read, the read address should be between 192 and 524,287 cycles after the write address pointer, otherwise the output for new data is not guarantee.

11.6 IRDY, ORDY Flags

The IRDY, ORDY flags indicate the status of FIFO. The IRDY signal reports whether or not there is space available for writing new data to the FIFO. An ORDY signal reports whether or not there is valid new data available at output. The IRDY and ORDY signals only report the status of the address pointer; they will not stop or affect the read/write operations. The following tables describe the IRDY/ORDY functions under different operating polarities.

/PLRTY = VDD

Signal	State	Function
IRDY	H	No more free space is available for new input data
	L	Memory space is available for new input data.
ORDY	H	No new data is available in FIFO memory.

	L	New data are available in the FIFO memory.

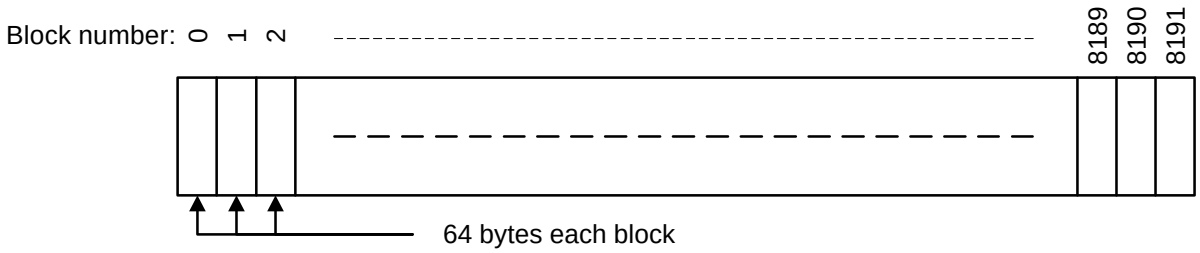
/PLRTY = GND

Signal	State	Function
IRDY	H	Memory space is available for new input data.
	L	No more free space is available for new input data
ORDY	H	New data are available in the FIFO memory.
	L	No new data is available in FIFO memory.

11.7 Window Write Register Programming

Window data read/write is supported in the AL440B to benefit the designing effort for applications such as PIP display. The window mode is enabled by driving low on /SDAEN signal. A serial bus can program built-in registers to set up coordinates of the window and the settings take effect following by next read/write reset pulse. Window mirroring can cooperate with the window mode data access to flip window data in x or y direction. When window-mirroring function is turned on, write data can be stored in reverse sequence.

The serial communication interface consists of 3 signals, they are SCL (serial clock), SDA (serial data) and /SDAEN (window mode enable). The serial communication interface is enabled by driving low on /SDAEN signal. The detail operation timing of the serial bus is illustrated in chapter 10. In Window read/write mode, read and/or write may begin at the start address of any of the 8192 blocks. Each block is 64 bytes in length. (8192 blocks x 64 byte = 512 kbytes)



Memory size: 8192 blocks x 64 bytes = 512 kbytes

AL440B Window mode block address

The Window Write related registers are listed as follows:
WSTART_L and WSTART_H define the widow data write starting address.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	WSTART_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
03h	WSTART_H	0	0	0	[12]	[11]	[10]	[9]	[8]

WSTART (Write Start address) <= WSTART_H[4:0] & WSTART_L ;
WSTART range is from 0 to 8191 (block).

WXSIZE_L and WXSIZE_H define the window data write horizontal size.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	WXSIZE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
05h	WXSIZE_H	0	0	0	0	0	0	[9]	[8]

WXSIZE (Write X Size) <= WXSIZE_H[2:0] & WXSIZE_L ;

WXSIZE range is from 0 to 1023 (block).

WXSTRIDE_L and WXSTRIDE_H define the window data write horizontal width.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	WSTRIDE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
07h	WSTRIDE_H	0	0	0	[12]	[11]	[10]	[9]	[8]

WSTRIDE (Write Stride) <= WSTRIDE_H[4:0] & WSTRIDE _L ;

WSTRIDE range is from –4096 to +4095 (block).

When the value of WSTRIDE is negative, it is used to implement Y-Mirror function.

WYSIZE_L and WYSIZE_H define the window data write vertical high.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	WYSIZE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
09h	WYSIZE_H	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

WYSIZE (Write Y Size) <= WYSIZE_H & WYSIZE_L ;

Write Y Size range is from 0 to 65535 (unsign).

WWCTRL is the register that control window data write function enable/disable and the window mirroring write.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	WWCTRL	[7]	[6]	[5]	0	0	0	0	0

WWCTRL[7] Window Write mode enable

1: enable Window Write mode

0: disable Window Write mode. The memory is operating in standard FIFO write mode.

WWCTRL[6] X-mirror function enable

1: enable X-mirror function

0: disable X-mirror function

WWCTRL[5] Freeze function enable. This function is as same as hardware “Write Mask” function. When Window Write mode is enabled, software freeze function override hardware Write Mask function. On the other hand, in FIFO mode (WWCTRL[7] = ‘0’), Register WWCTRL[5] is ignored.

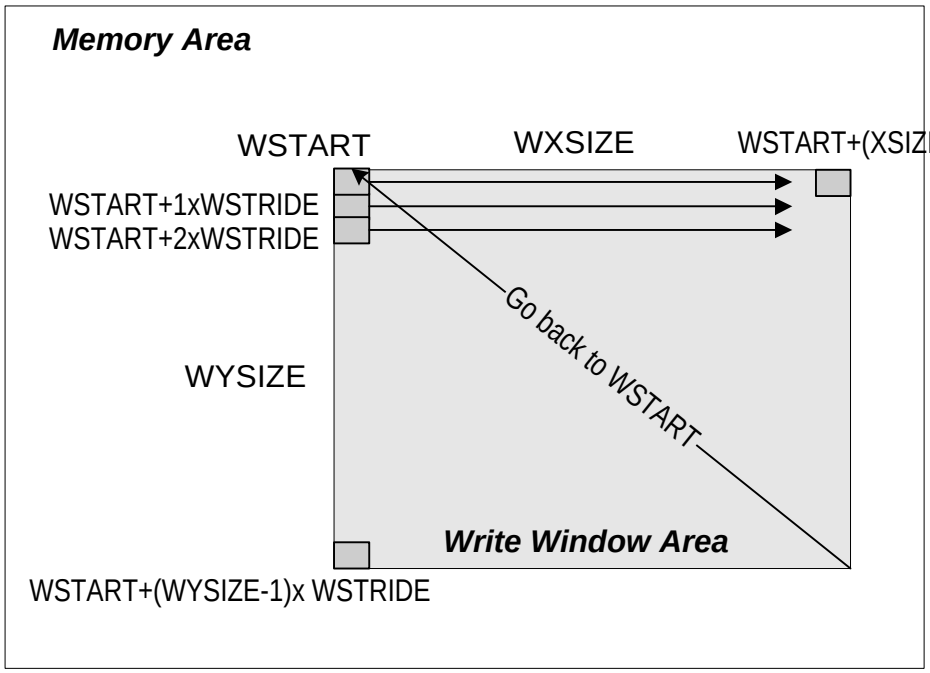
1: enable software Freeze function

0: disable software Freeze function

A mirroring read/write function can be cooperated with the window-block data access function. By turning on the mirroring read/write function in the window block access mode, write data can be

stored in reversed sequence. For some applications like video conferencing, this function can correct reciprocal positioning of a captured object.

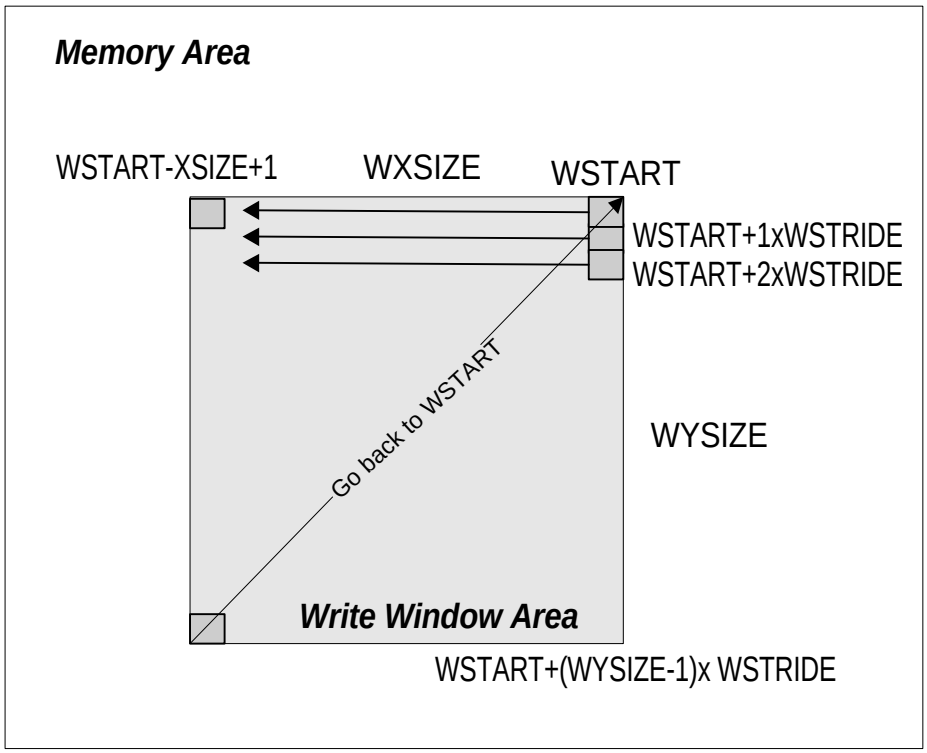
Please refer the following diagrams which illustrate Window Write operation.



Normal Write Window:

WWCTRL[6]: 0
No X-mirror
WSTRIDE: postive numer
No Y-mirror

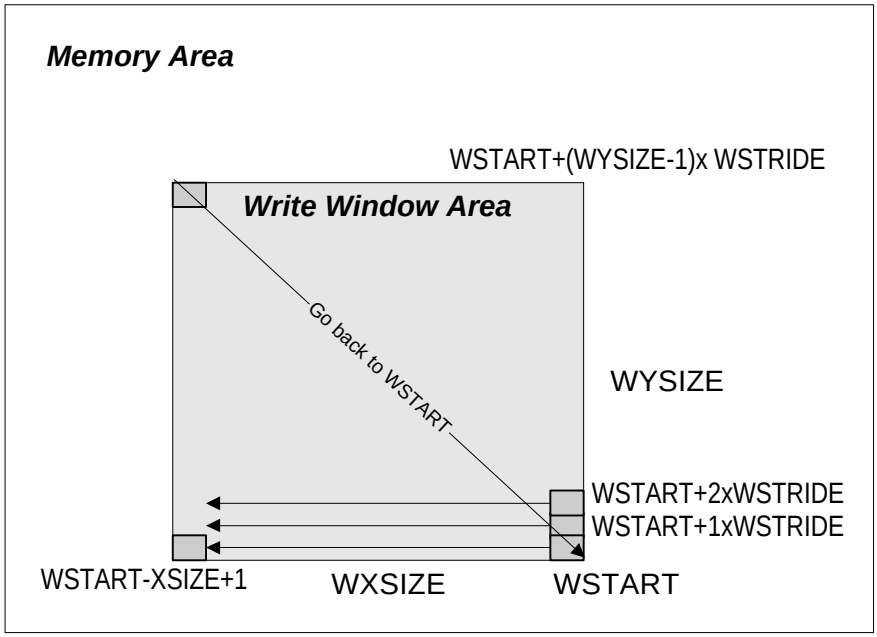
AL440B Write Window(1)



X-mirror Write Window:

WWCTRL[6]: 1
X-mirror
WSTRIDE: postive numer
No Y-mirror

AL440B-03 Write Window(2)



X-mirror & Y-mirror Write Window:

WWCTRL[6]: 1
X-mirror
WSTRIDE: negative numer
Y-mirror

AL440B Write Window(3)

11.8 Window Read Register Programming

The operations of Window Read function are same as Window Write. The operation of Window Read is operated independently from Window Write. The Window Read related registers are listed as follows:

RSTART_L and RSTART_H define the widow data read starting address.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	RSTART_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0Ch	RSTART_H	0	0	0	[12]	[11]	[10]	[9]	[8]

RSTART (Read Start address) <= RSTART_H[4:0] & RSTART_L ;
RSTART range is from 0 to 8191 (block).

RXSIZE_L and RXSIZE_H define the window data read horizontal size.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	RXSIZE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0Eh	RXSIZE_H	0	0	0	0	0	0	[9]	[8]

RXSIZE (Read X Size) <= RXSIZE_H[2:0] & RXSIZE_L ;
WXSIZE range is from 0 to 1023 (block).

RXSTRIDE_L and RXSTRIDE_H define the window data write horizontal width.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	RSTRIDE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
10h	RSTRIDE_H	0	0	0	0	[11]	[10]	[9]	[8]

RSTRIDE (Read Stride) <= RSTRIDE_H[3:0] & RSTRIDE _L ;
RSTRIDE range is from 0 to +4095 (block).

RYSIZE_L and RYSIZE_H define the window data read vertical high.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	RYSIZE_L	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
12h	RYSIZE_H	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

RYSIZE (Read Y Size) <= RYSIZE_H & RYSIZE_L ;
Write Y Size range is from 0 to 65535.

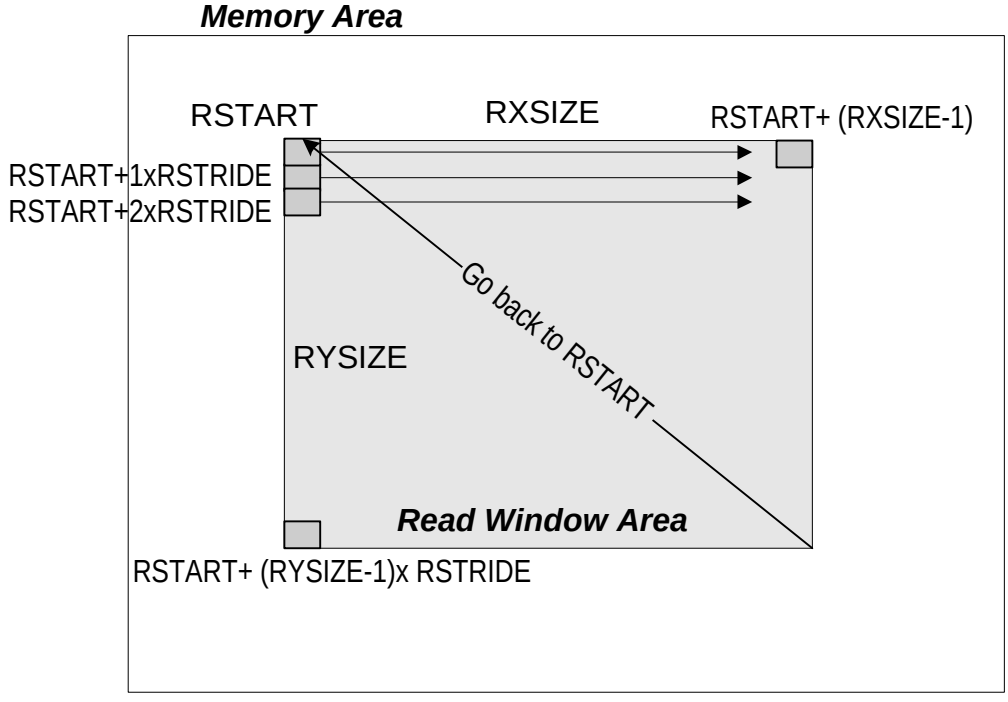
RWCTRL is the register that control window data read function enable/disable .

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	RWCTRL	[7]	0	0	0	0	0	0	0

RWCTRL[7] Read Write mode enable
- 1: enable Window Read mode
- 0: disable Window Read mode. The memory is operating in standard FIFO Read mode.

Note:
1. X-mirror and Y-mirror functions are not needed in Window Read mode, so they are not implemented in Window Read operation.
2. There is no “freeze” function in Window Read mode.

Please refer to the following illustration as an application example for the explanation of Window read operation.



AL440B Read Window

12.0 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter		Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	℃
T_{stg}	Storage temperature	-40 ~ +125	℃

12.2 Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V

12.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		Min	Typ	Max	Unit
I_{DD}	Operating Current	-	52	62	mA
I_{DDS}	Standby Current	-	14	-	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current (No pull-up or pull-down)	-5	-	+5	μA
I_{LO}	Output Leakage Current (No pull-up or pull-down)	-5	-	+5	μA
R_L	Input Pull-up/Pull-down Resistance		50		KΩ

1. Tested with outputs disabled (I_{OUT} = 0)
2. RCLK and WCLK toggle at 20 Mhz and data inputs switch at 10 Mhz.

12.4 AC Characteristics

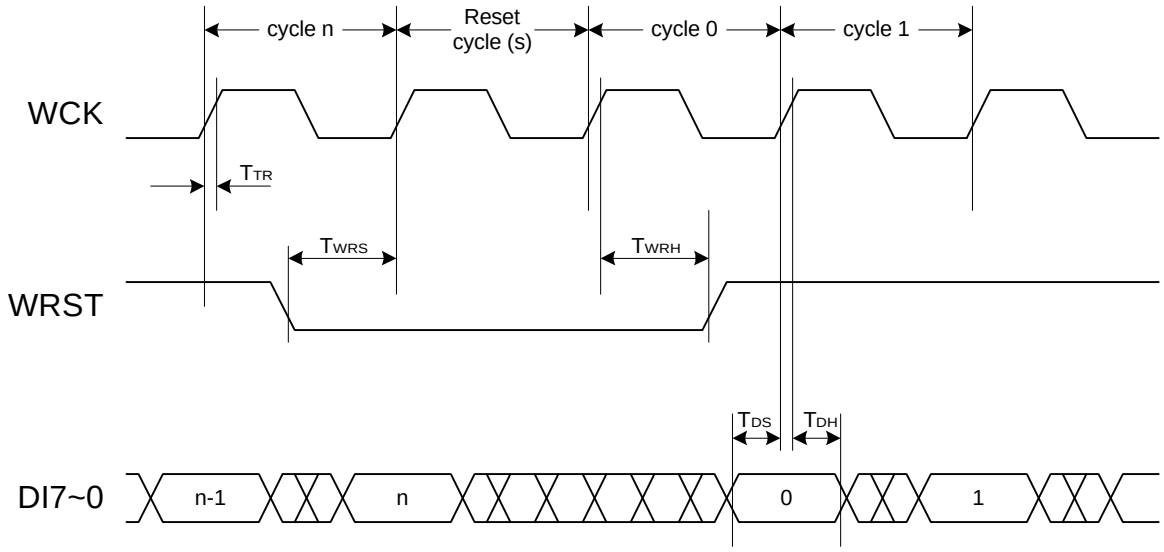
(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

Parameter		40MHz		80MHz		Unit
		Min	Max	Min	Max	
T_{WC}	WCK Cycle Time	25	-	12.5	-	ns
T_{WPH}	WCK High Pulse Width	10	-	5	-	ns
T_{WPL}	WCK Low Pulse Width	10	-	5	-	ns
T_{RC}	RCK Cycle Time	25	-	12.5	-	ns
T_{RPH}	RCK High Pulse Width	10	-	5	-	ns
T_{RPL}	RCK Low Pulse Width	10	-	5	-	ns
T_{AC}	Access Time	-	20	-	12	ns
T_{OH}	Output Hold Time	6	-	4	-	ns
T_{HZ}	Output High-Z Setup Time	5		4		ns
T_{LZ}	Output Low-Z Setup Time	6		5		ns
T_{WRS}	WRST Setup Time	8	-	4	-	ns
T_{WRH}	WRST Hold Time	8	-	5	-	ns
T_{RRS}	RRST Setup Time	8	-	4	-	ns
T_{RRH}	RRST Hold Time	8	-	5	-	ns
T_{DS}	Input Data Setup Time	5	-	4	-	ns
T_{DH}	Input Data Hold Time	6	-	5	-	ns
T_{WES}	WE Setup Time	6	-	4	-	ns
T_{WEH}	WE Hold Time	6	-	5	-	ns
T_{WPW}	WE Pulse Width	15	-	12	-	ns
T_{RES}	RE Setup Time	6	-	4	-	ns
T_{REH}	RE Hold Time	6	-	5	-	ns
T_{RPW}	RE Pulse Width	15	-	12	-	ns
T_{IES}	IE Setup Time	6	-	4	-	ns
T_{IEH}	IE Hold Time	6	-	5	-	ns
T_{IPW}	IE Pulse Width	15	-	12	-	ns
T_{OES}	OE Setup Time	8	-	5	-	ns
T_{OEH}	OE Hold Time	8	-	5	-	ns
T_{OPW}	OE Pulse Width	20	-	12	-	ns
T_{TR}	Transition Time	3		3		ns
C_I	Input Capacitance	-	7	-	7	pF

C_O	Output Capacitance	-	7	-	7	pF

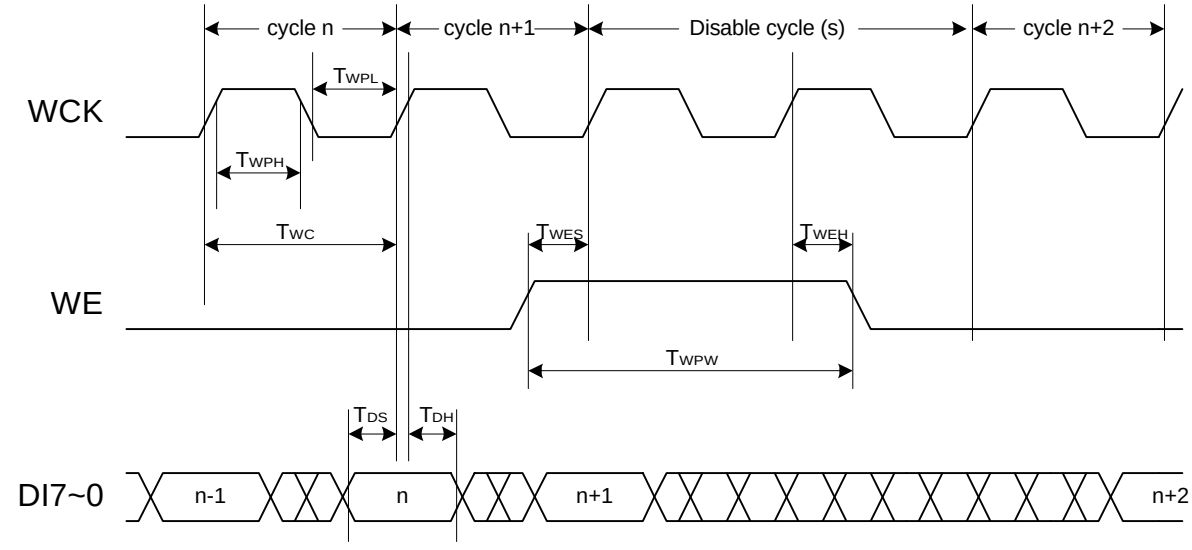
- The read address needs to be at least 192 cycles after the write address.

13.0 Timing Diagrams



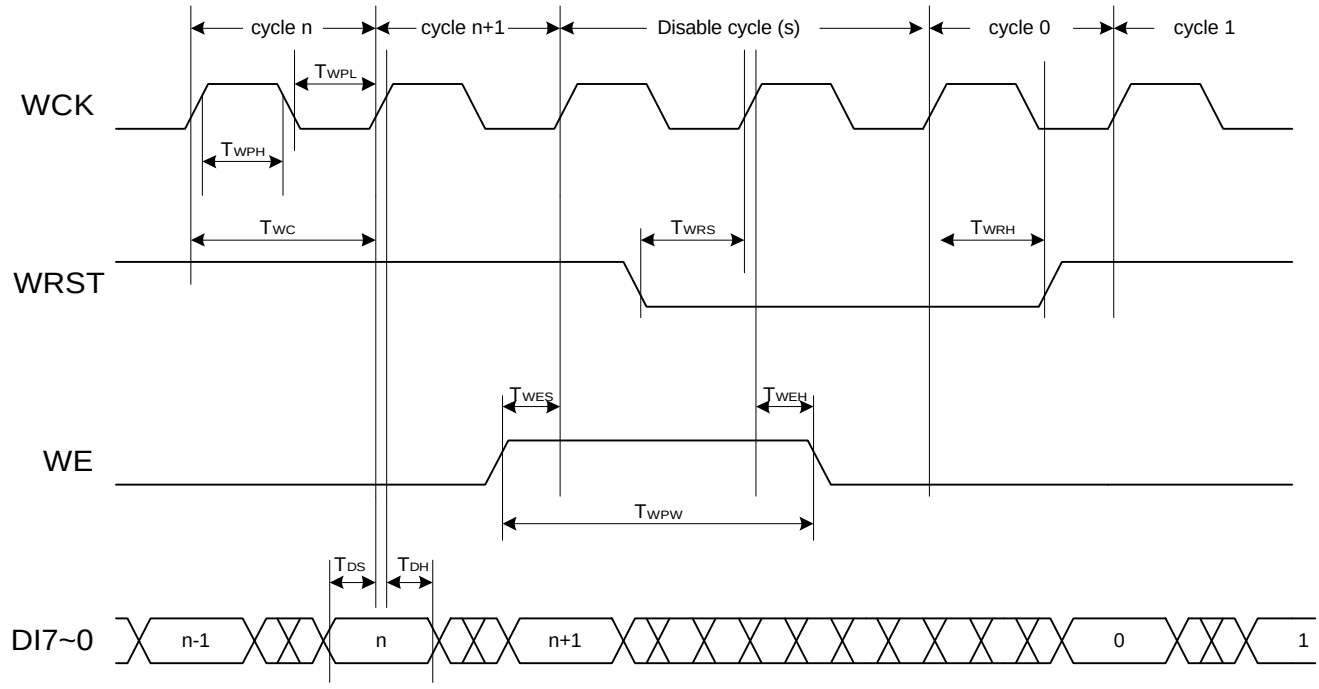
/PLRTY=VDD , WE= "L" , IE= "L"

Write Cycle Timing (Write Reset)



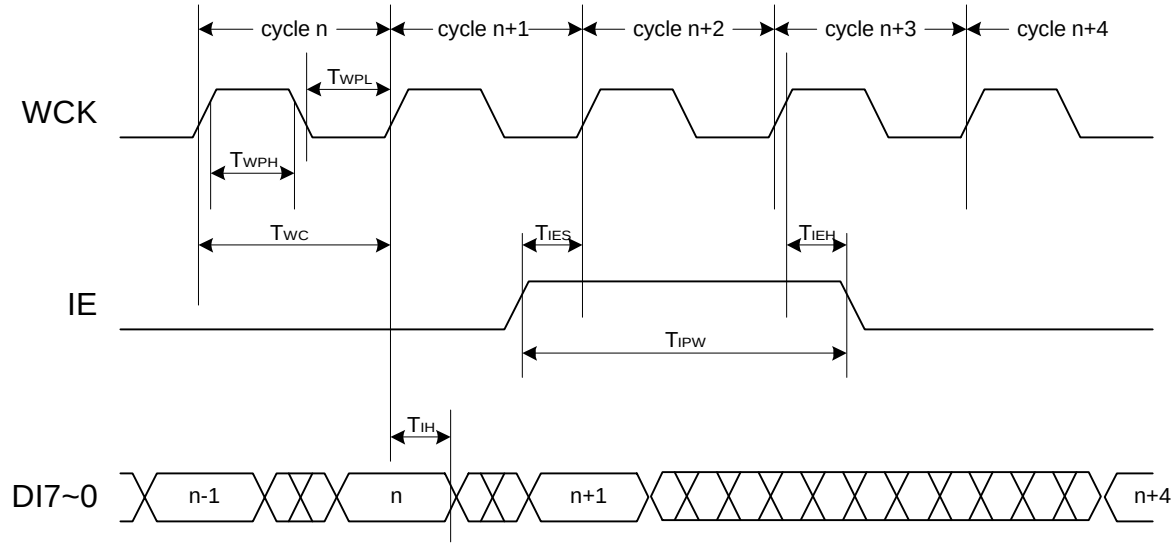
/PLRTY=VDD ,IE="L" ,WRST="H"

Write Cycle Timing (Write Enable)



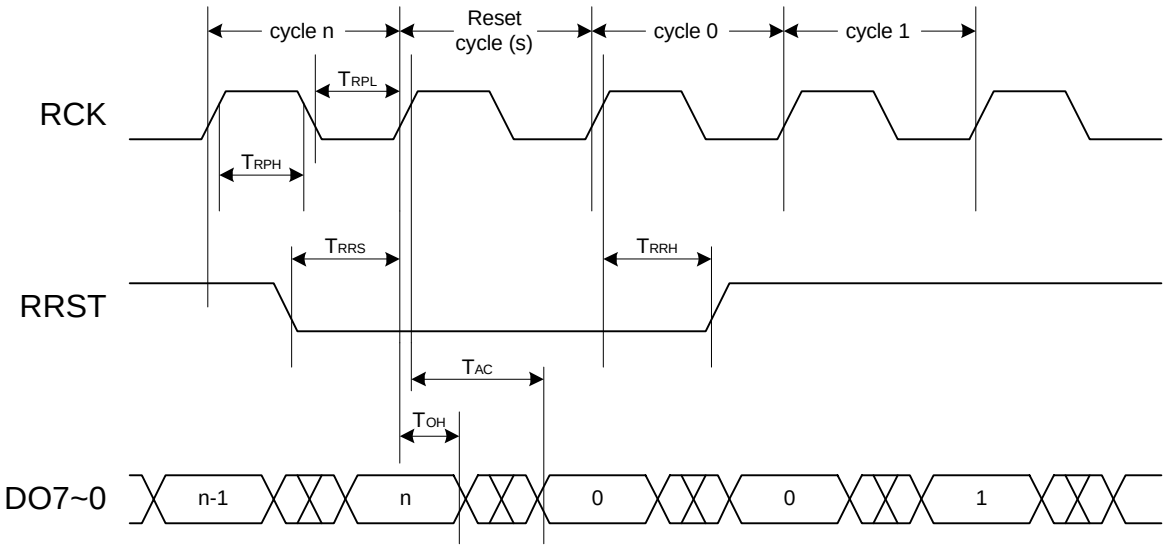
/PLRTY=VDD ,IE="L"

Write Cycle Timing (WE, WRST)



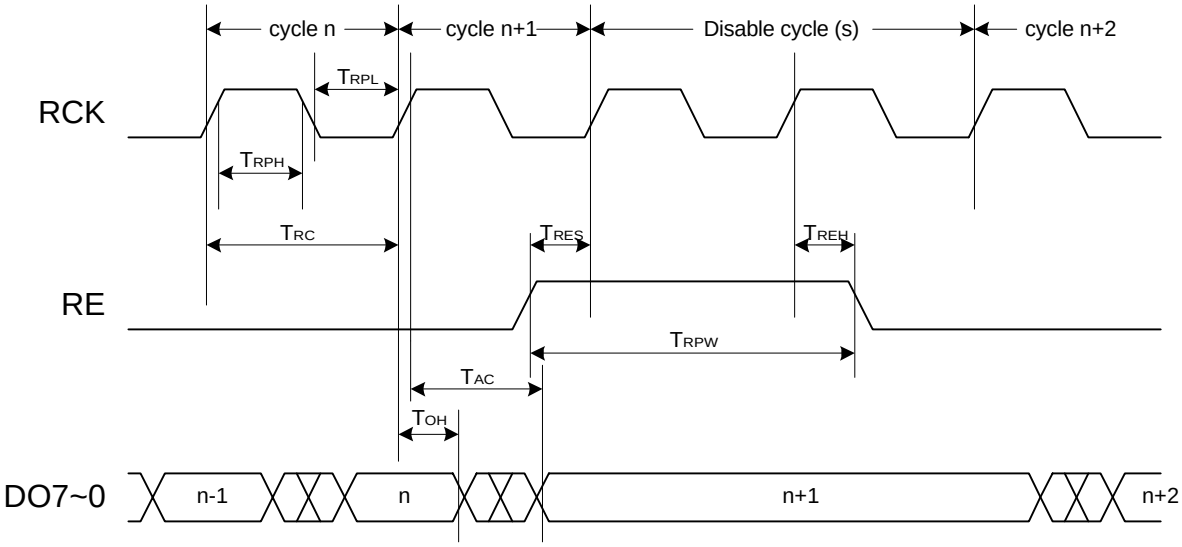
/PLRTY=VDD ,WE="L" ,WRST="H"

Write Cycle Timing (Input Enable)



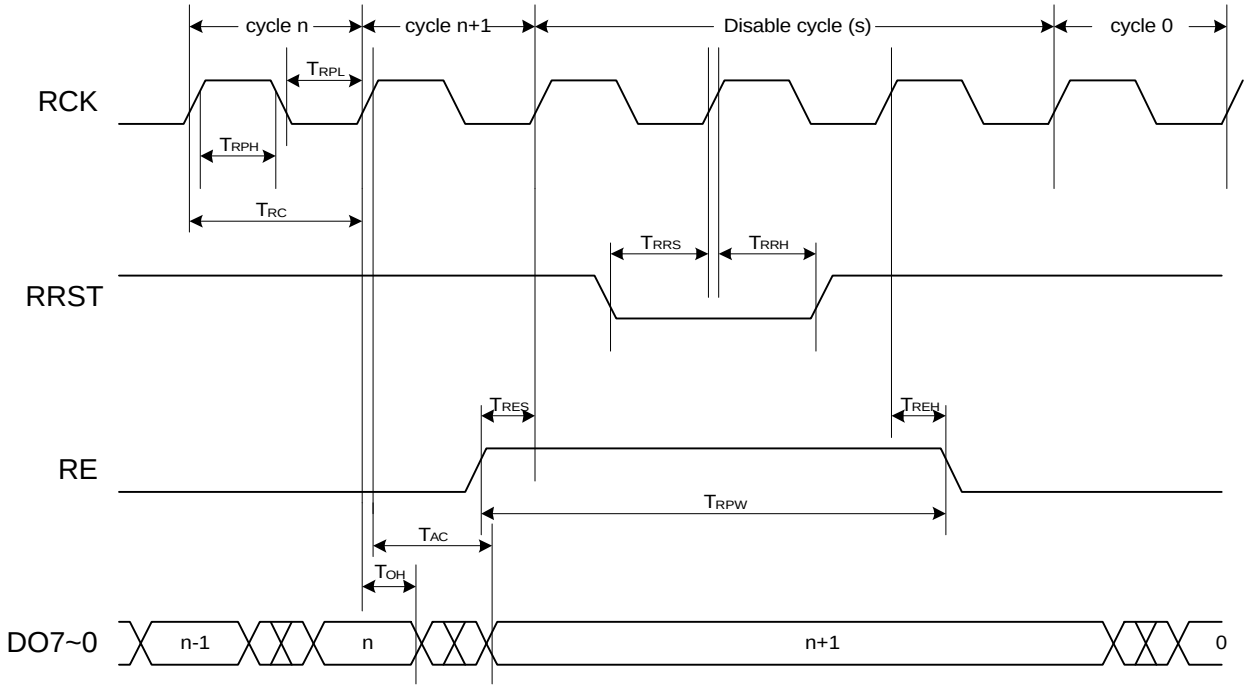
/PLRTY=VDD ,RE= "L" ,OE= "L"

Read Cycle Timing (Read Reset)



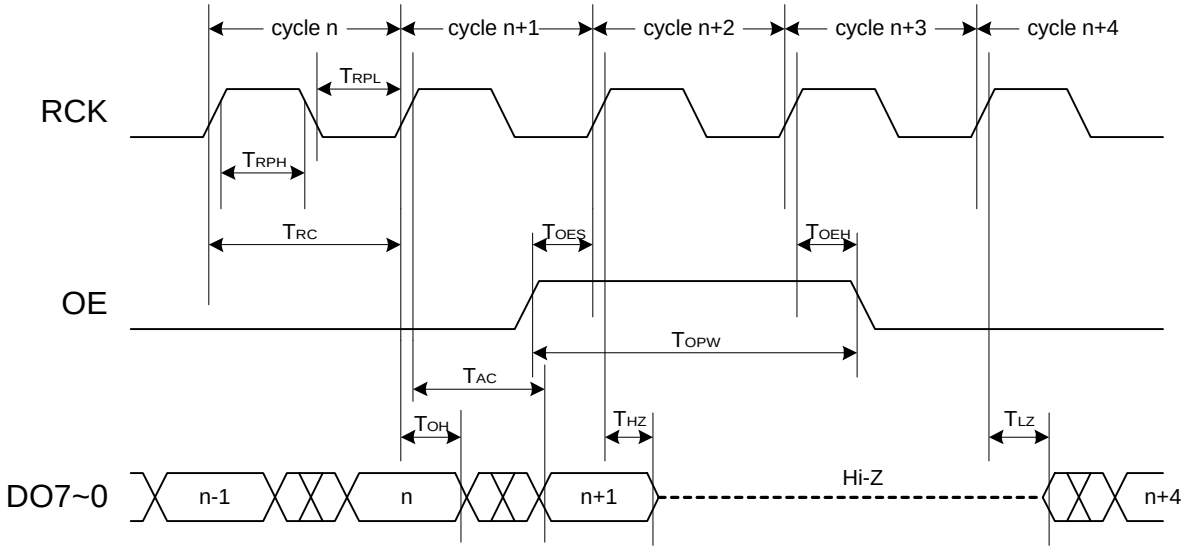
/PLRTY=VDD ,OE="L" ,RRST="H"

Read Cycle Timing (Read Enable)



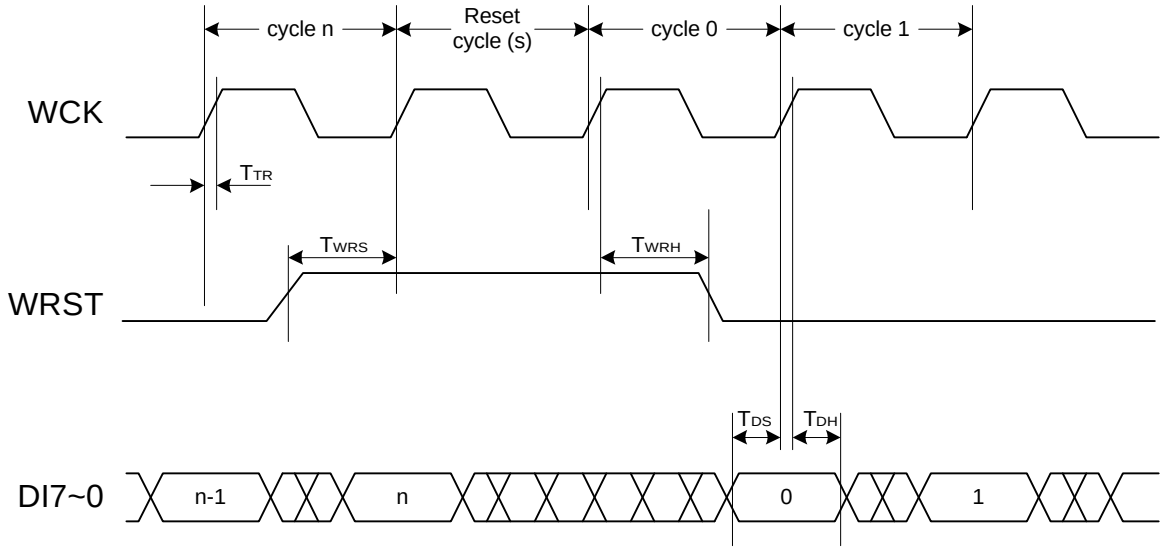
/PLRTY=VDD ,OE="L"

Read Cycle Timing (RE, RRST)



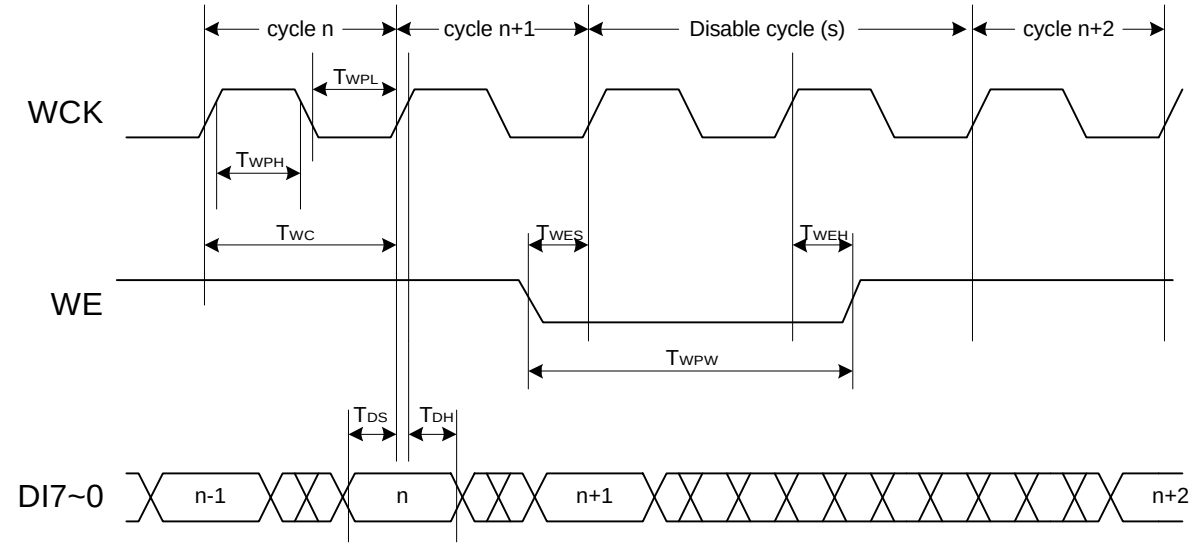
/PLRTY=VDD ,RE="L" ,RRST="H"

Read Cycle Timing (Output Enable)



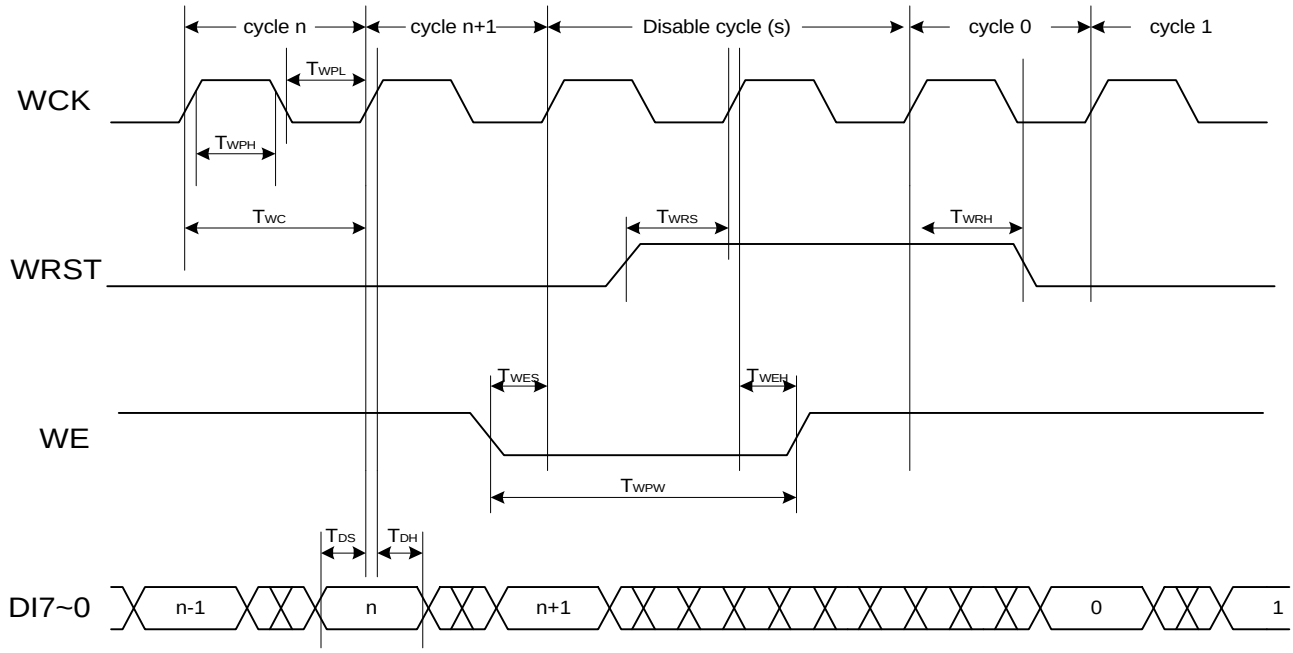
/PLRTY=GND , WE= "H" , IE= "H"

Write Cycle Timing (Write Reset)



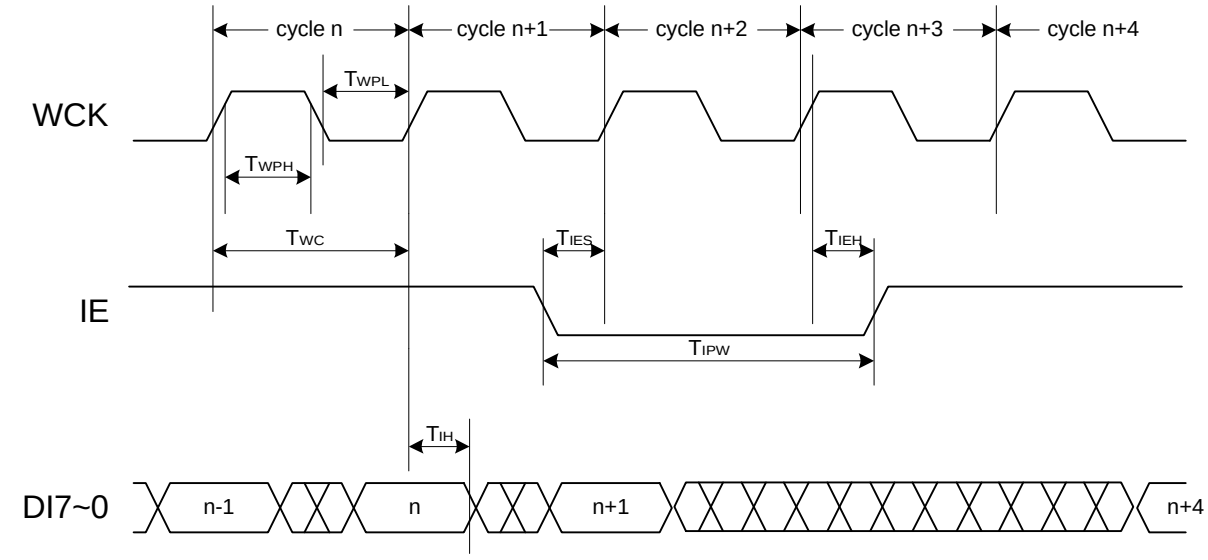
/PLRTY=GND ,IE="H" ,WRST="L"

Write Cycle Timing (Write Enable)



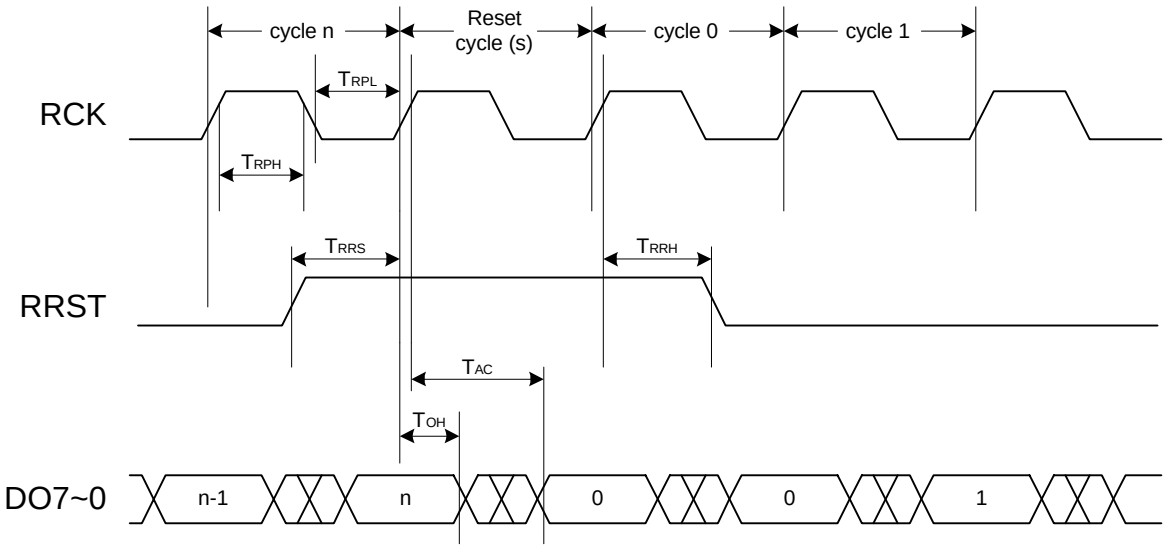
/PLRTY=GND ,IE="H"

Write Cycle Timing (WE, WRST)



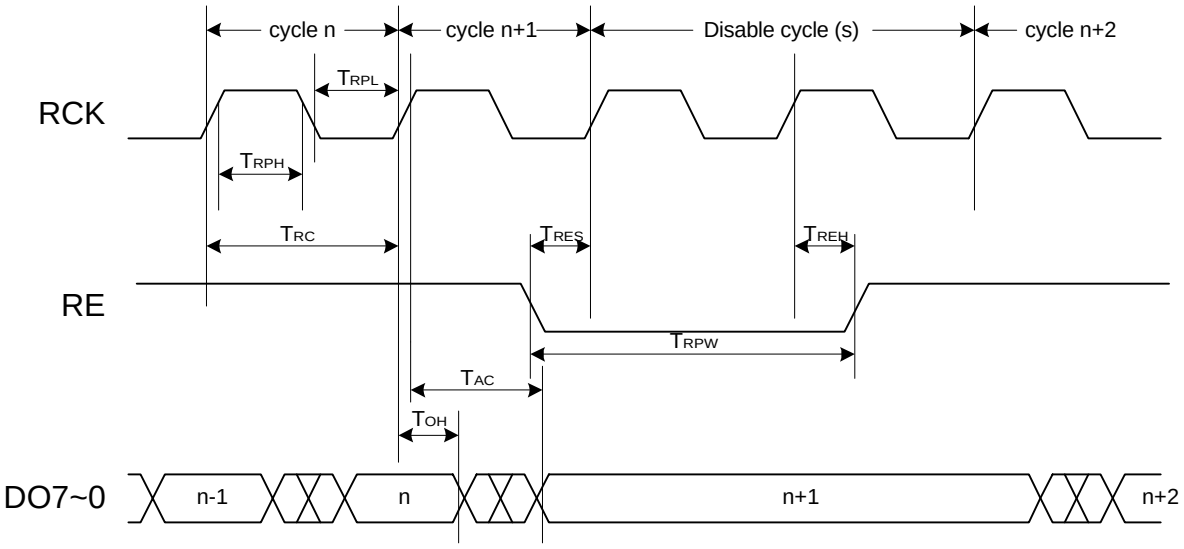
/PLRTY=GND ,WE="H" ,WRST="L"

Write Cycle Timing (Input Enable)



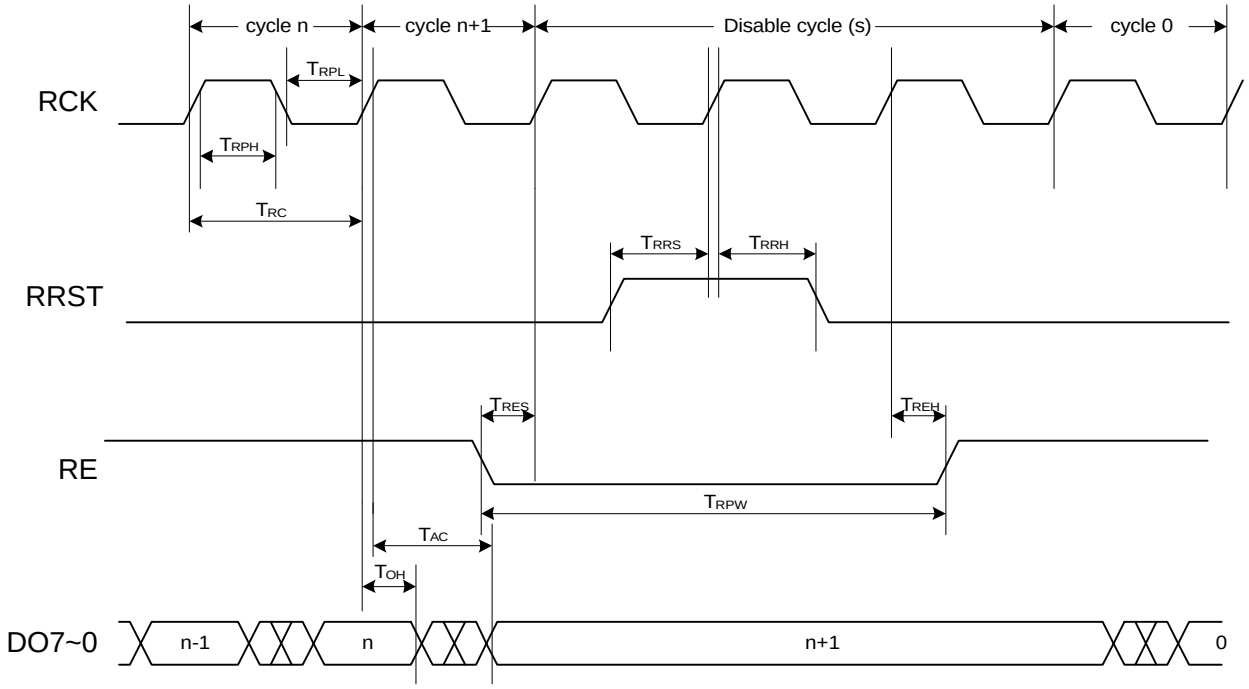
/PLRTY=GND ,RE= "H" ,OE= "H"

Read Cycle Timing (Read Reset)



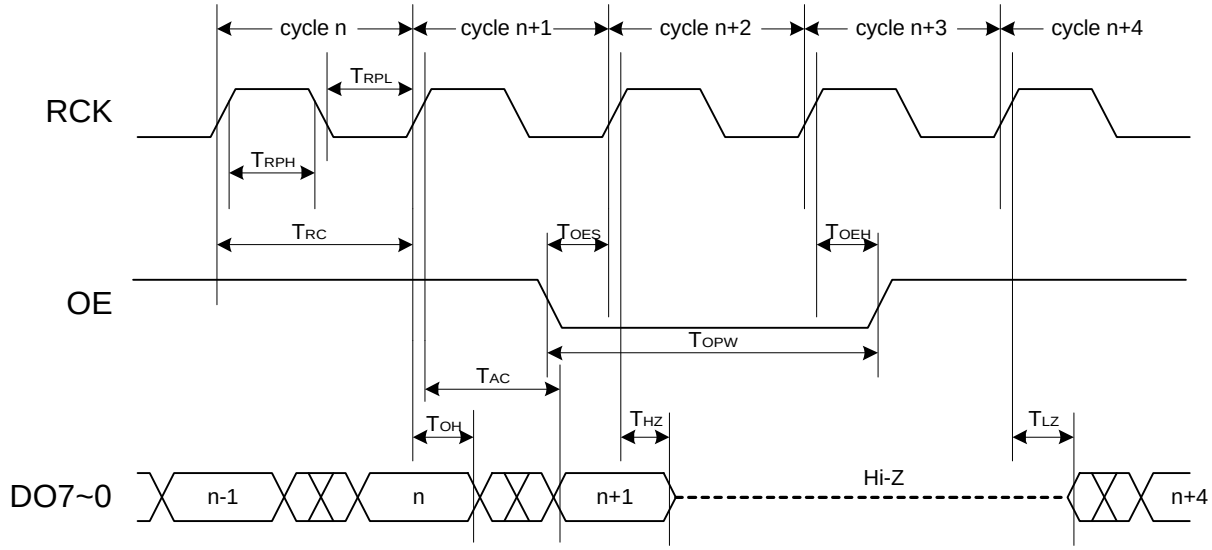
/PLRTY=GND ,OE="H" ,RRST="L"

Read Cycle Timing (Read Enable)



/PLRTY=GND ,OE="H"

Read Cycle Timing (RE, RRST)

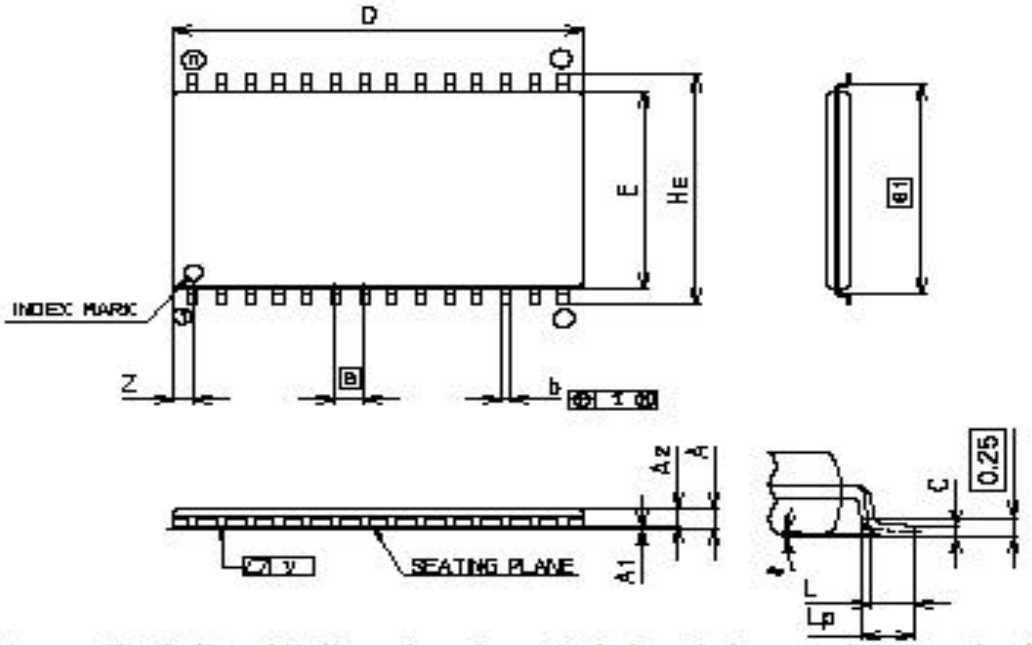


/PLRTY=GND ,RE="H" ,RRST="L"

Read Cycle Timing (Output Enable)

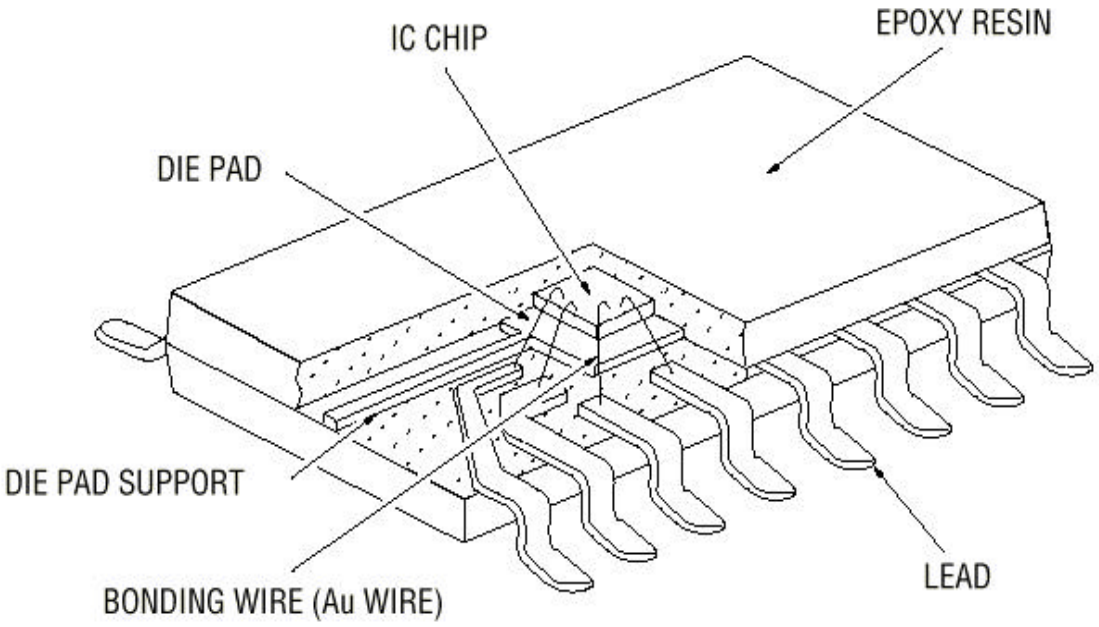
14.0 Mechanical Drawing – 44 PIN PLASTIC TSOP (II)

PLASTIC TSOP (Type II)



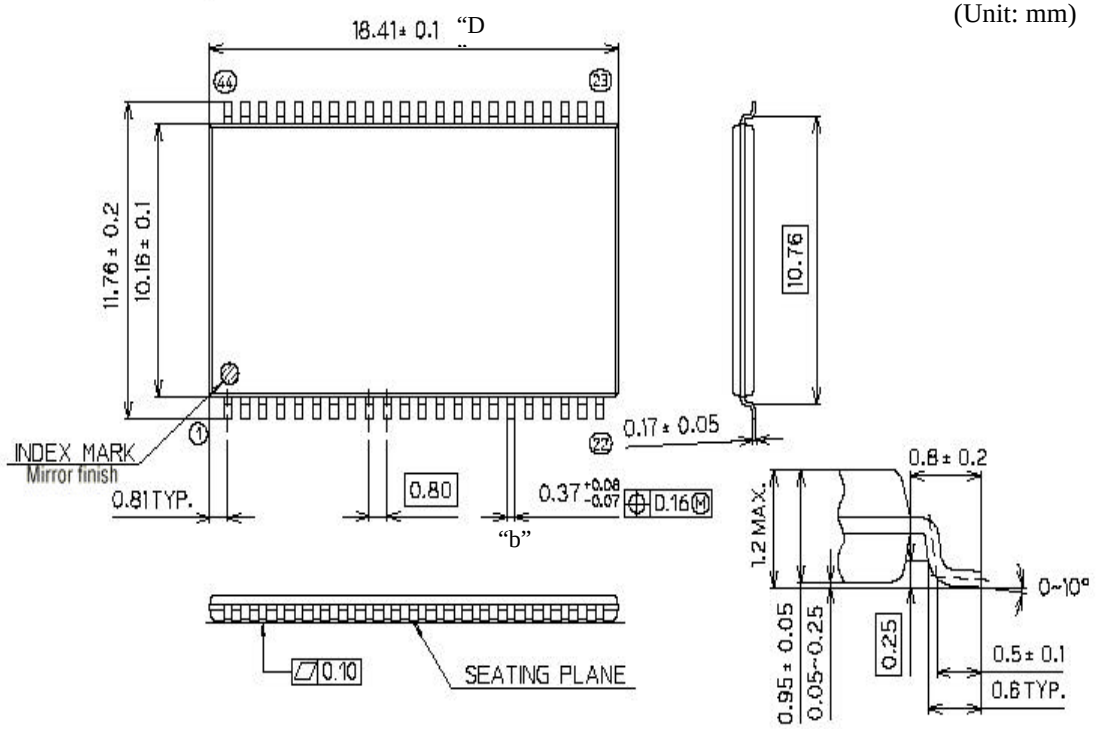
Note: The D, E, and Z dimensions do not include resin burrs and the remains from die pad support.

Package Structural Diagram



TSOPII44-P-400-0.80-K

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	0.54 TYP.

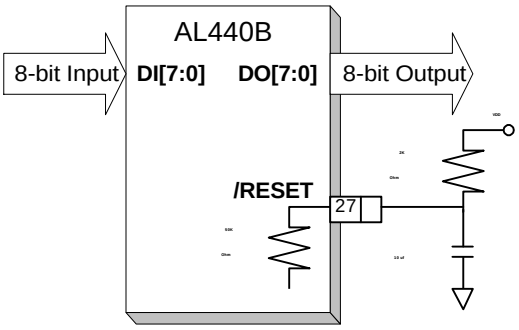
NOTE:

1. Controlling Dimension : Millimeters.
2. Dimension "D" does not include mold protrusion. Mold protrusion shall not exceed 0.15(0.006") per side. Dimension "E1" does not include interlead protrusion. Interlead protrusion shall not exceed 0.25(0.01") per side.
3. Dimension "b" does not include damar protrusions/intrusion. Allowable damar protrusion shall not cause the lead to be wider than the MAX "b" dimension by more than 0.13mm. Damar intrusion shall not cause the lead to be narrower than the MIN "b" dimension by more than 0.07mm.

15.0 Application Notes

15.1 Chip Global Reset Recommend Circuit

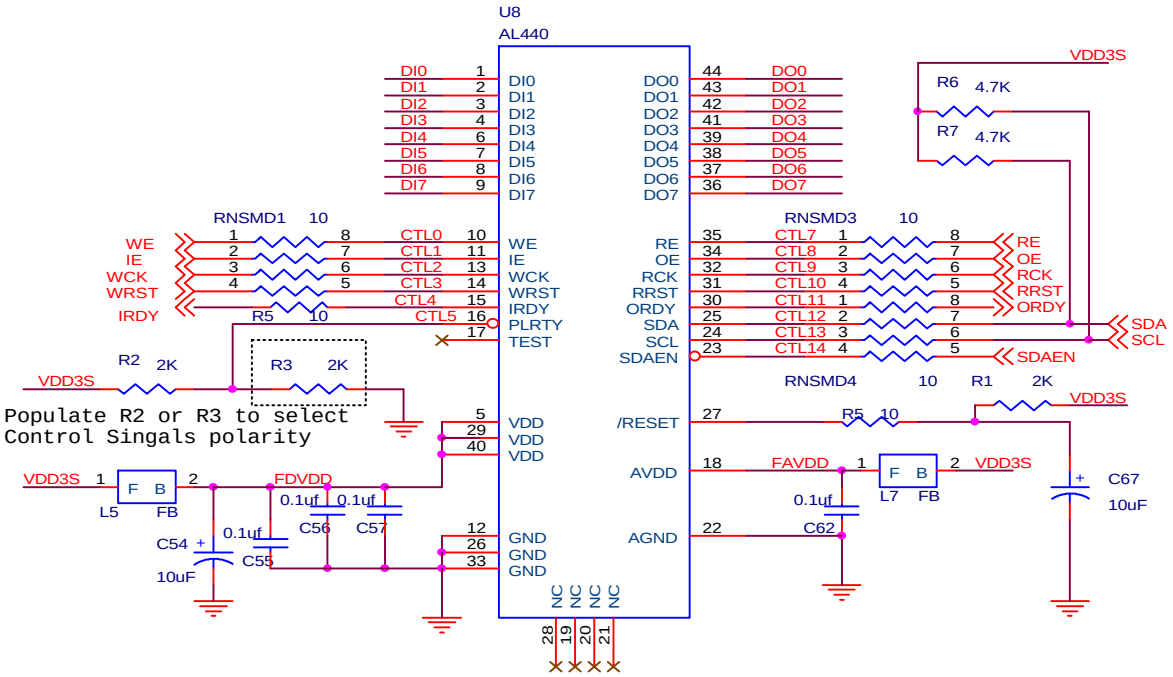
To ensure a proper reset pulse can be applied to /RESET pin (pin 27) to complete the power-on reset, the recommend reset circuit is to connect the AL440B /RESET pin (pin 27) to V_{DD} with a 2k Ω resistor and to Ground with a 10μf capacitor as follows.



AL440B Global Reset Circuit

It is also recommend adding buffers for the power-on reset circuit to increase the driving capability for any application with multiple AL440B chips.

15.2 The AL440B Reference Schematic



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