GRAPHIC DISPLAY MODULE

GP1002C09A INSTRUCTION MANUAL

GENERAL DESCRIPTION

FUTABA GP1002C09A is a graphic display module using a FUTABA 320×240 VFD.
It consists of a VFD, a driver, a control circuit and power source.
The module can be connected directly to the bus line of the host system CPU.
The power sources for the high voltage (Vcc2) 『9P00A003-01 (AC input type)』 and 『9P00A005-01 (5V input type)』 are also available as an option.

CONTENTS

1. FEATURES

1-1. This module is equipped with a FUTABA full-dot Front Luminus VFD (FLVFD) having 320 × 240 pixels.

1) The Front Luminous VFD panel presents clear display with wide visible angle.

2) Pixel selection from the X-Y matrix allows the display to be free from distortion , displacement or flicker.

3) A vertical or horizontal line can be displayed in a continuous line by the use of the dual-wire grid scanning system. Furthermore, utilization of the deflection of electron beams increases luminance and reduces the number of grid drivers.

4) Display color change is available by the use of an adequate filter. (within the range of green to orange , white)

1-2. The high-voltage driver IC permits the module size to be thinner and more compact.

1-3. The built-in control circuit and power circuit enable easier module drive and connection to a host system.

1-4. The module is equipped with RAM having an interface of bit-map system, which facilitates the write-in and read-out of the display data.

1-5. Brightness can be adjusted from a host CPU side.

2. GENERAL SPECIFICATIONS

2-1. DIMENSIONS, WEIGHT (Refer FIG.1)

TABLE-1

ITEM	SPECIFICATION	UNIT
OUTER DIMENSIONS	(L) 180 ±0.5 (W) 160 MAX. (T) 41 MAX.	mm
WEIGHT	Approx.1.5	kg

2-2. OPTICAL CHARACTERISTICS

TABLE-2

ITEM	SPECIFICATION		UNIT
VIEW AREA	120×90		mm
NUMBER OF DOTS	320×240		DOT
DOT PITCH	0.375×0.375		mm
DOT SIZE	0.3×0.3		mm
EMISSION COLOR	Green (505nm)		
LUMINANCE	MIN. 100 (30)	TYP. 200 (60)	cd/m^2 (fL)

(Note)
By using a filter, uniform color ranging from blue to orange (including white) can be displayed.

Luminance represents the value under the typical rated condition (Refer 2-4).

2-3. ABSOLUTE MAXIMUM RATINGS

TABLE-3

ITEM	SYMBOL	MIN.	MAX.	UNIT
SUPPLY VOLTAGE (LOW)	Vcc1	-0.5	6.0	Vdc
SUPPLY VOLTAGE (HIGH)	Vcc2	-0.5	150	Vdc
INPUT SIGNAL VOLTAGE	V_{IS}	-0.5	Vcc1 + 0.5	V
OPERATING TEMPERATURE	Topr	0	+ 50	°C
STORAGE TEMPERATURE	Tstg	-20	+ 70	°C
OPERATING HUMIDITY	Hopr	0	85	%
STORAGE HUMIDITY	Hstg	0	90	%
VIBRATION	-	-	4	G
SHOCK	-	-	40	G

NOTE 1) Always keep the module free from moisture both for operation and storage.

2-4. RECOMMENDED OPERATING CONDITION

TABLE-4

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE (LOW)	Vcc1	4.5	5.0	5.5	Vdc
SUPPLY VOLTAGE (HIGH)	Vcc2	110	135	140	Vdc
H-LEVEL INPUT VOLTAGE	V_{IH}	2.4	-	-	V
L-LEVEL INPUT VOLTAGE	V_{IL}	-	-	0.8	V

2-5. ELECTRICAL AND OPTICAL CHARACTERISTICS UNDER THE TYPICAL OPERATING CONDITION

TABLE-5

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY CURRENT (LOW)	Icc1	Vcc1 = 5.0Vdc Vcc2 = 135Vdc GND = 0 V V_{IH} = 2.4V V_{IL} < 0.8V	-	-	1.9	A
SUPPLY CURRENT (HIGH)	Icc2		-	-	55	mA
H-LEVEL INPUT CURRENT	I_{IH}		-	-	20	µA
L-LEVEL INPUT CURRENT	I_{IL}		-	-	-0.4	mA
H-LEVEL OUTPUT VOLTAGE	V_{OH}		4.2	-	Vcc1	V
L-LEVEL OUTPUT VOLTAGE	V_{OL}		GND	-	0.5	V
H-LEVEL OUTPUT CURRENT	I_{OH}		-	-	-0.4	mA
L-LEVEL OUTPUT CURRENT	I_{OL}		-	-	3.0	mA
POWER CONSUMPTION	-		-	-	17.00	W
LIMINANCE	-		100 (30)	200 (60)	- (-)	cd/m² (fL)

NOTE 2) The supply voltage and power consumption represent the value when all display dots are lit.

3. OUTER DIMENSIONS (FIG.1)

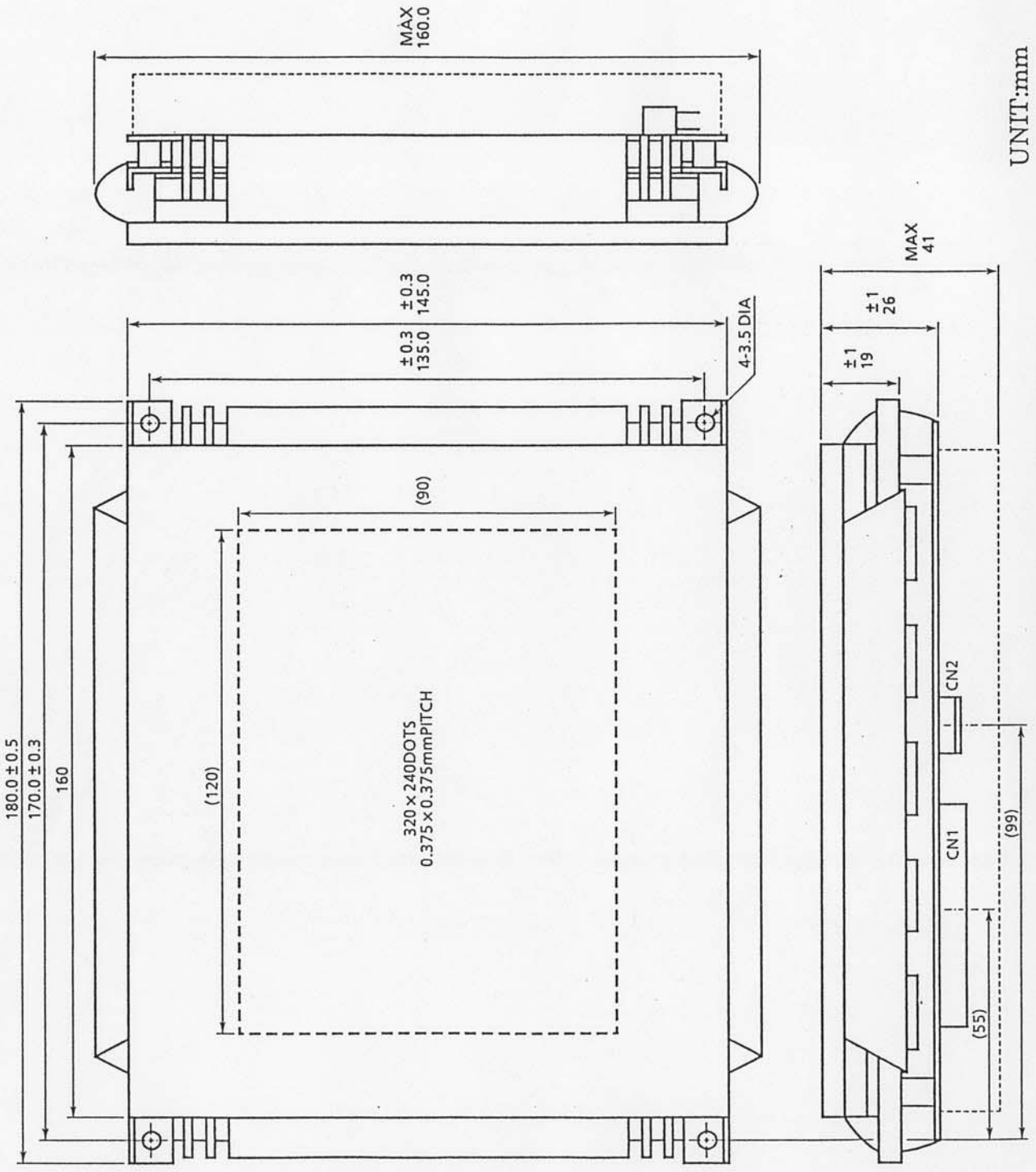


FIG.1 MECHANICAL DRAWING

4. CIRCUIT BLOCKDIAGRAM (FIG.2)

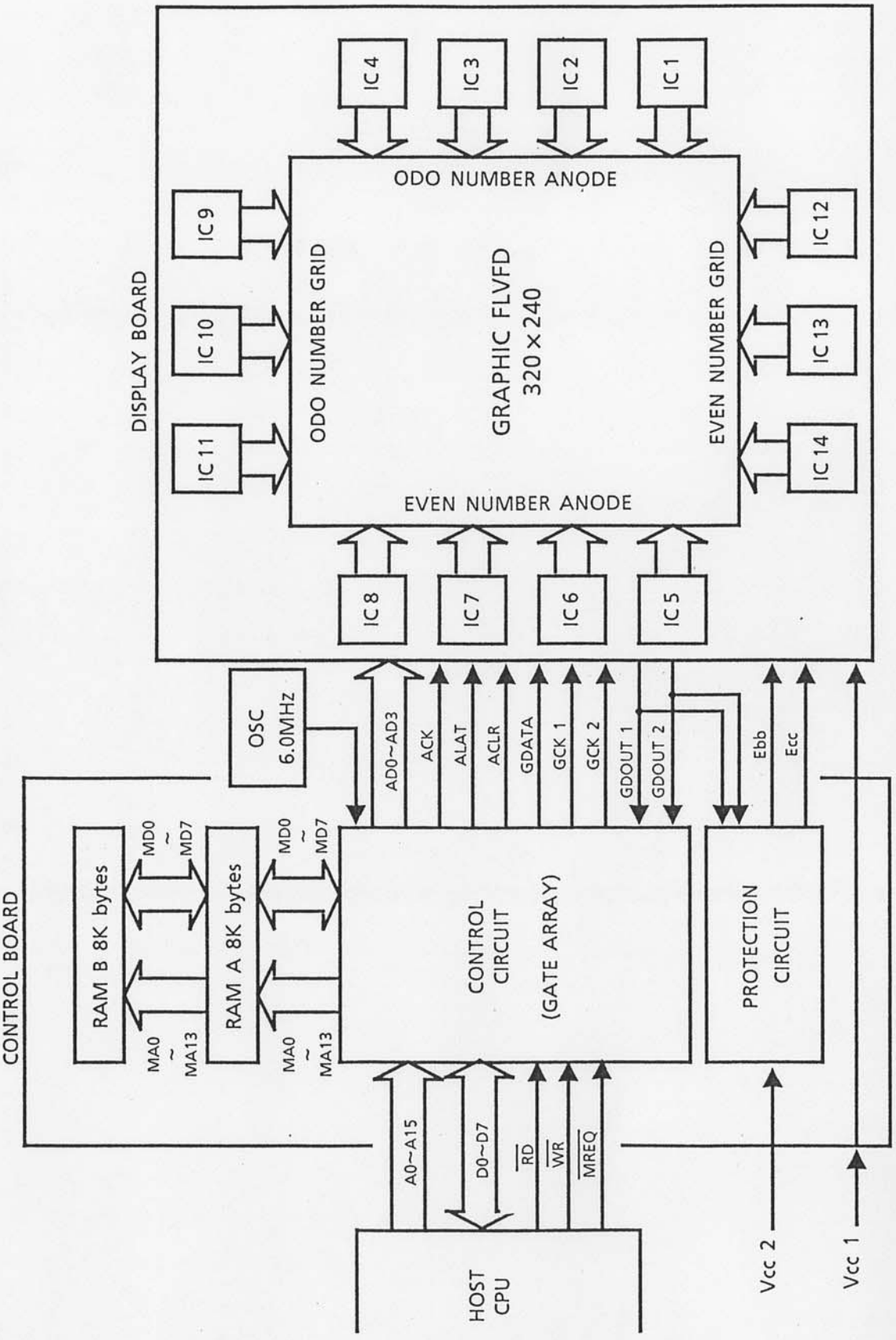


FIG.2 BLOCK DIAGRAM

5. PARTS LAYOUT (FIG.3)

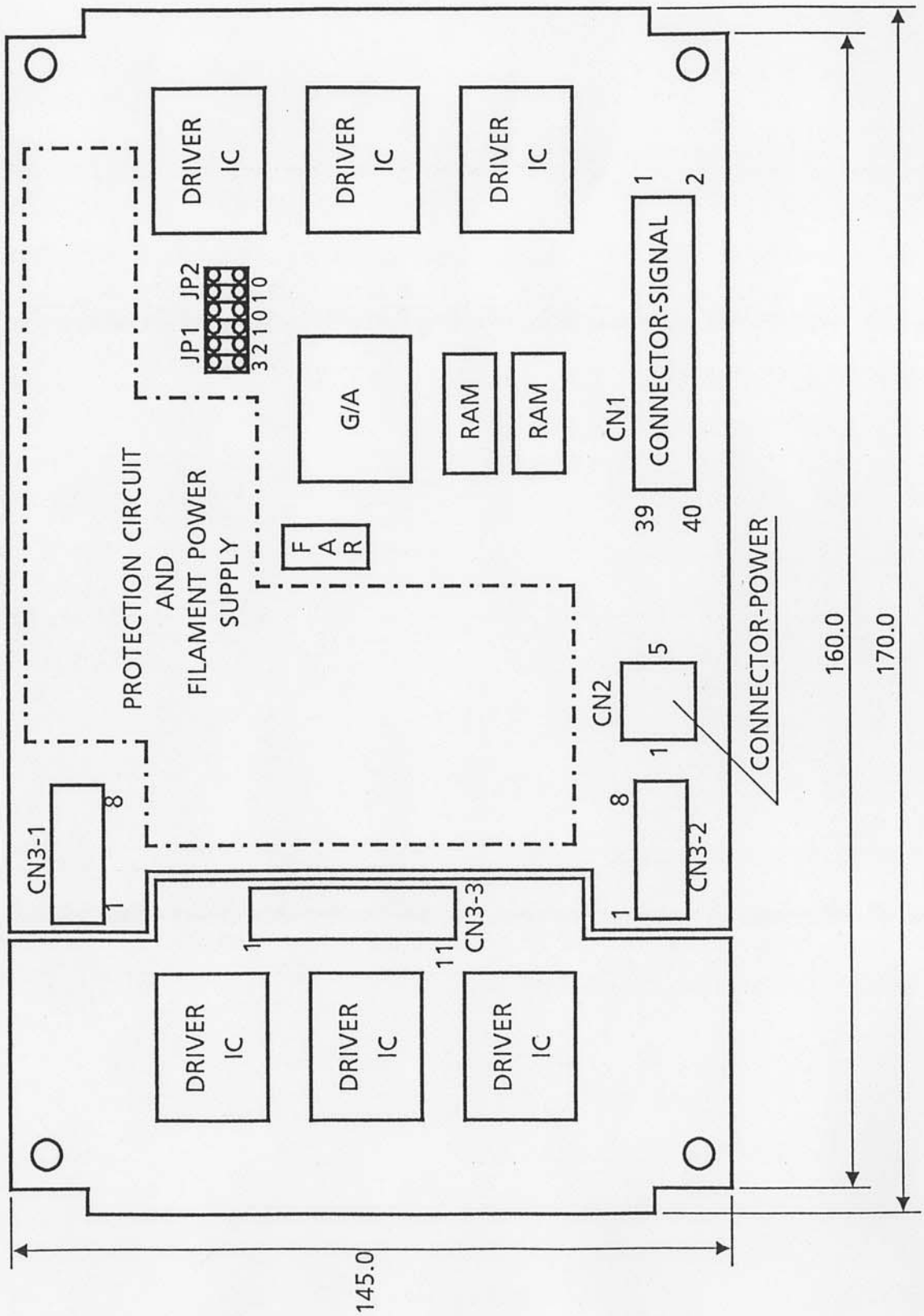


FIG.3 LAYOUT (CONTROL BOARD)

6. CONNECTOR PIN ASSIGNMENT

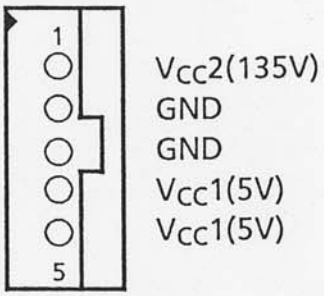
(1) Connector to signal (CN 1)

	HIROSE	HIF3E-40PA-2.54DS
Applicable Connector	HIROSE	HIF3BA-40DA-2.54R

(2) Connector to Power Supply (CN 2)

	JAE	IL-5P-S3FP2	
Applicable Connector	JAE	IL-5S-S3L	(Housing)
	JAE	IL-C2-5000	(Contact)

Connector to Power Supply (CN 2)



NOTE 1)
Both ground pins (2 and 3) and both power (4 and 5) are interally connected.

NOTE 2)
All GND terminal of CN1 and CN2 are connected together on the PCB.

Connector to signal (CN 1)

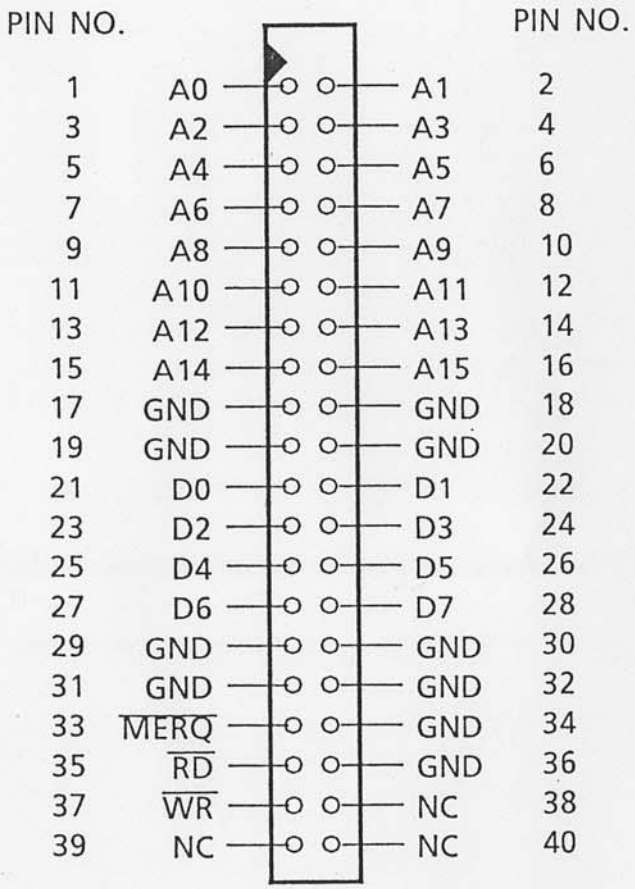


FIG.4 CONNECTOR PIN ASSIGNMENT

7. FUNCTIONS

7-1. Basic Functions

1. Data Write-In
2. Data Read-Out
3. Brightness Adjustment

7-2. Function Table

TABLE-6

$\overline{MERQ}$	$\overline{RD}$	$\overline{WR}$	MODE
L	L	H	READ-OUT
L	H	L	WRITE-IN
×	×	×	DISPLAY

×……either H or L is available

7-3. Jumper Lines of the Decoder Circuit

The address area available for driving the module is 16k byte.
Absolute addressing is available with jumper pins.

TABLE-7

JP 1				
0	1	2	3	RAM (16Kバイト)
○	—	○	—	0000H~3FFFH
—	○	○	—	4000H~7FFFH
○	—	—	○	8000H~BFFFH
—	○	—	○	C000H~FFFFH

○……the state of short-circuit

—……the state of open-circuit

(NOTE) When shipped-out, JP1 is set with NO.2 shorted-cirrcuited ; (8000H~BFFFH)

7-4. Data Write-In

Since the display screen is devided into a 16k byte memory map, display data are written-in in the 8-bit unit.

Data are written-in to the addresses designated by jumper JP1, when $\overline{MERQ}$ = "L", $\overline{RD}$ = "H", $\overline{WR}$ = "L".

FIG.5 shows the relationship of memory address of the control circuit to the location of display dots.

The data in the non-display regions A and B can not be displayed.

<Example of Data Write-In>

To display a letter A on the left top of the display,

1. Allocate the absolute address by JP1.
   In this case, follow the condition at the time of shipment ;8000H~BFFFH.

2. Input data as shown in Table-8.

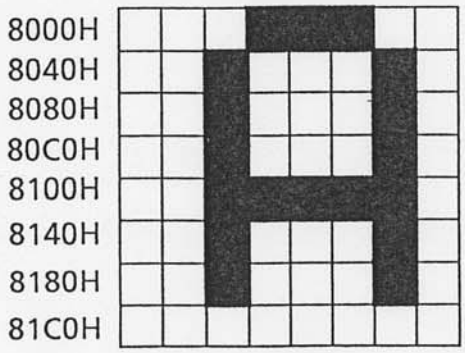


TABLE-8

Address	Data
8000H	38H
8040H	44H
8080H	44H
80C0H	44H
8100H	7CH
8140H	44H
8180H	44H
81C0H	00H

Memory address and the dot position to be displayed
(according to the setting at the time of shipment)

40 × 8dots = 320dots

8dots

Non-Display Region B

Memory Area

240dots

8000H	8001H	8002H		8027H	8028H		803FH
8040H	8041H	8042H		8067H	8068H		807FH
8080H	8081H	8082H		80A7H	80A8H		80BFH
80C0H	80C1H	80C2H		80E7H	80E8H		80FFH
8100H	8101H	8102H		8127H	8128H		813FH
8140H	8141H	8142H		8167H	8168H		817FH
8180H	8181H	8182H		81A7H	81A8H		81BFH
81C0H	81C1H	81C2H		81E7H	81E8H		81FFH
			DISPLAY PANEL				
BBC0H	BBC1H	BBC2H		BBE7H	BBE8H		BBFFH
BC00H	BC01H	BC02H		BC27H	BC28H		BC3FH
BFC0H	BFC1H	BFC2H		BFE7H	BFE8H		BFFFH

Non-Display Region A

D0	D1	D2	D3	D4	D5	D6	D7

Data in 1 byte

240dots

(0 , 0)	(1 , 0)	(2 , 0)		(318 , 0)	(319 , 0)
(0 , 1)	(1 , 1)	(2 , 1)		(318 , 1)	(319 , 1)
(0 , 2)	(1 , 2)	(2 , 2)		(318 , 2)	(319 , 2)
(0 , 3)	(1 , 3)	(2 , 3)		(318 , 3)	(319 , 3)
			DISPLAY PANEL		
(0,239)	(1,239)	(2,239)		(318,239)	(319,239)
(0,240)	(1,240)	(2,240)		(318,240)	(319,240)
(0,255)	(1,255)	(2,255)		(318,255)	(319,255)

Non-Display Region A

FIG.5 MEMORY ADDRESS AND THE DOT POSITION TO BE DISPLAYED

7-5. Data Read-Out

The data of the currently displayed pattern can be read-out by designating the address, when $\overline{MERQ}$ = "L", $\overline{RD}$ = "L", $\overline{WR}$ = "H".

To secure proper execution of the read-out instruction, it should be repeated one time.

The data displayed by the first read-out command is invalid,which shall be made valid by the second read-out.

This two step read-out is a safety measure to guarantee the proper functioning of the module.

Be sure not to execute such an instruction as to set RD to "L" during the first and the secpond read-outs.

7-6. Brightness adjustment

The last address (1 byte) of the 16k byte memory within the module is assigned as the control parameter for brightness adjustment.

When the address space consists of 8000H to BFFFH, BFFFH is assigned as the control parameter for brightness adjustment.

When the upper 4 bits are "0", the maximum brightness (100%) can be obtained. When they are "1", the display goes off.

With these parameters, brightness can be adjusted in 16 levels.

TABLE-9

D7 D6 D5 D4	D3 D2 D1 D0	LUMINANCE
0 0 0 0	0 0 0 0	100%
0 0 0 1	0 0 0 0	level 1
0 0 1 0	0 0 0 0	level 2
⋮	⋮	⋮
1 1 1 1	0 0 0 0	0%

Never fail to set D3 through D0 to "0".

Otherwise, failures may occur, such as no display or data cannot be written-in.

D7 through D0 are automatically initialized into "0" when power-on.

8. WRITE-IN AND READ-OUT TIMING

(1) WRITE-IN (Ref. TIMING CHART)

TABLE-10

ITEM	SYMBOL	MIN.	MAX.	UNIT
ADDRESS SET UP TIME (FROM $\overline{MREQ}$)	tAS1	20	—	ns
ADDRESS SET UP TIME (FROM $\overline{WR}$)	tAS2	20	—	ns
MREQ VALID TIME (FOR $\overline{WR}$)	tMW	100	—	ns
ADDRESS HOLD TIME (FROM $\overline{MREQ}$)	tAH1	20	—	ns
ADDRESS HOLD TIME (FROM $\overline{WR}$)	tAH2	20	—	ns
WRITE PULSE WIDTH	tWP	100	—	ns
WRITE PERIOD *1	tWS	1.9	—	μs
INPUT DATA SET UP TIME	tDW	40	—	ns
INPUT DATA HOLD TIME	tDH	50	—	ns

*1 The time between the rising edge of write pulse and next one.

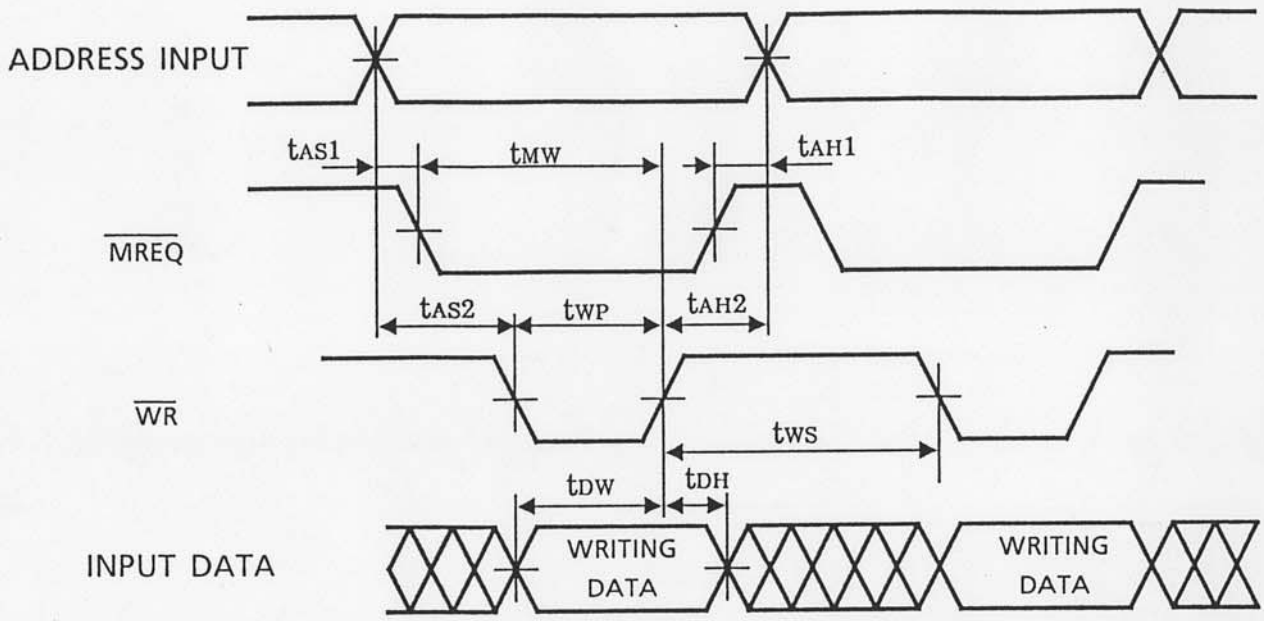
(2) READ-OUT

TABLE-11

ITEM	SYMBOL	MIN.	MAX.	UNIT
ADDRESS SET UP TIME (FROM $\overline{MREQ}$)	tAS1	20	—	ns
ADDRESS SET UP TIME (FROM $\overline{WR}$)	tAS2	20	—	ns
MREQ VALID TIME (FOR $\overline{WR}$)	tMR1	100	—	ns
MREQ VALID TIME (FOR $\overline{WR}$)	tMR2	150	—	ns
ADDRESS HOLD TIME (FROM $\overline{MREQ}$)	tAH1	0	—	ns
ADDRESS HOLD TIME (FROM $\overline{WR}$)	tAH2	0	—	ns
READ PULSE WIDTH	tRP1	100	—	ns
READ PULSE WIDTH	tRP2	150	—	ns
READ PERIOD *1	tRS	1.7	—	μs
OUTPUT ENABLE ACCESS TIME	tOE	—	150	ns
OUT PUT HOLD TIME	tOH	20	—	ns

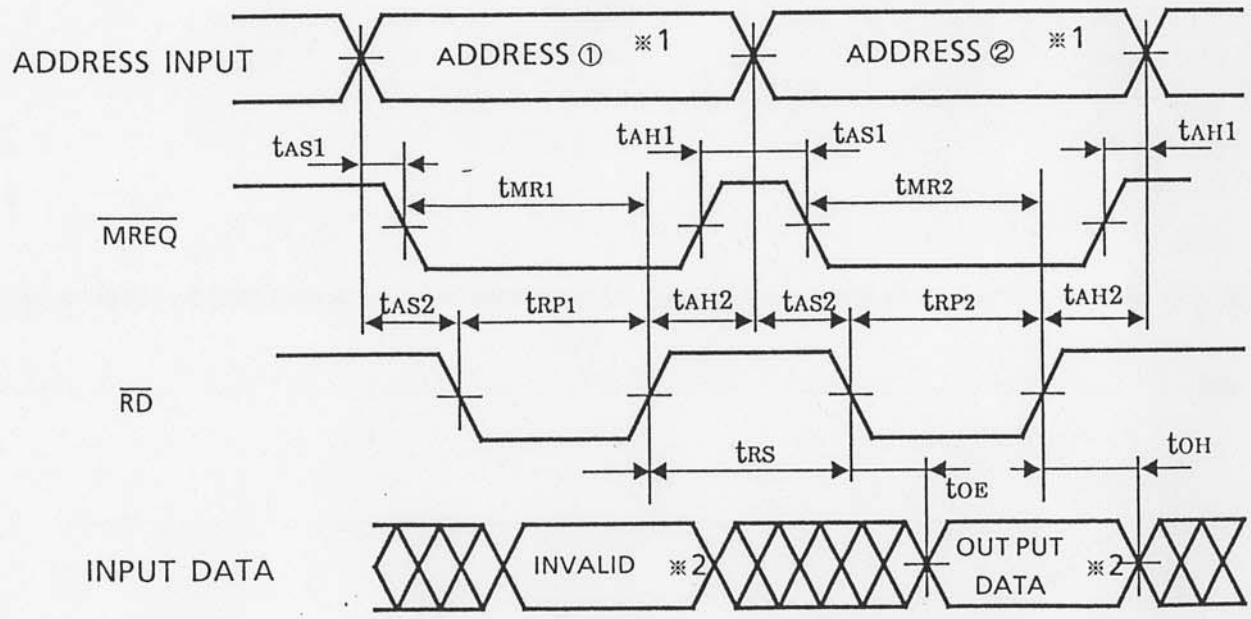
*1 The time between the rising edge of read pulse and next one.

(3) WRITE TIMING



NOTE) $\overline{RD}$ shall be high level when data is written.

(4) READ TIMING



※1 The address① and ② shall be the same.
※2 The data out put is invalid when the timing ①.

NOTE) $\overline{WR}$ shall be high level when data is read.

9. EXAMPLE OF MODULE INTIALIZING

Each time the power is turned on, it is necessary to initilize the module by the program of the host CPU.
This is because the RAM content is in a random state.
Below the procedure for utilizing Z80 CPU memory area 8000H~BFFFH (16k byte) is described.

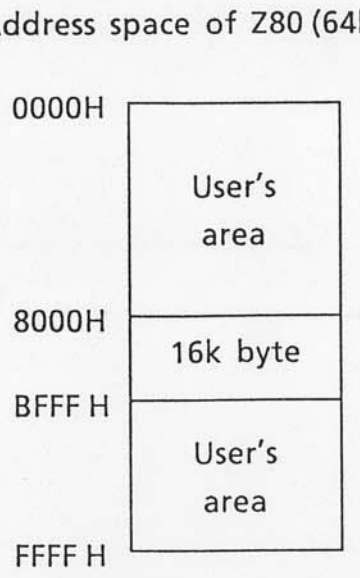


FIG.7 EXAMPLE OF MODULE INTIALIZING

(1) Set the jumper for the module.
Set the adress for the jumper.
Select 0 and 3 of JP1 to be short-circuit ·····to be decoded to address area
Set the adress for the jumper. 8000H~BFFFH.

Select 0 of JP2 to be short-circuit ·····to be used by Z80

(NOTE) When shipped-out, the module is set as shown above.

(2) Supply the power.
When power is supplied, either Vcc1 or Vcc2 comes first.

(NOTE) Never change the setting with the supply voltage applied.

(3) Write-in 00H to the address 8000H~BBF1H.
The whole display screen goes off.

10. INTERFACE CONNECTION

The module can be connected directly to the bus line of the host system CPU. The representative connection is described below.

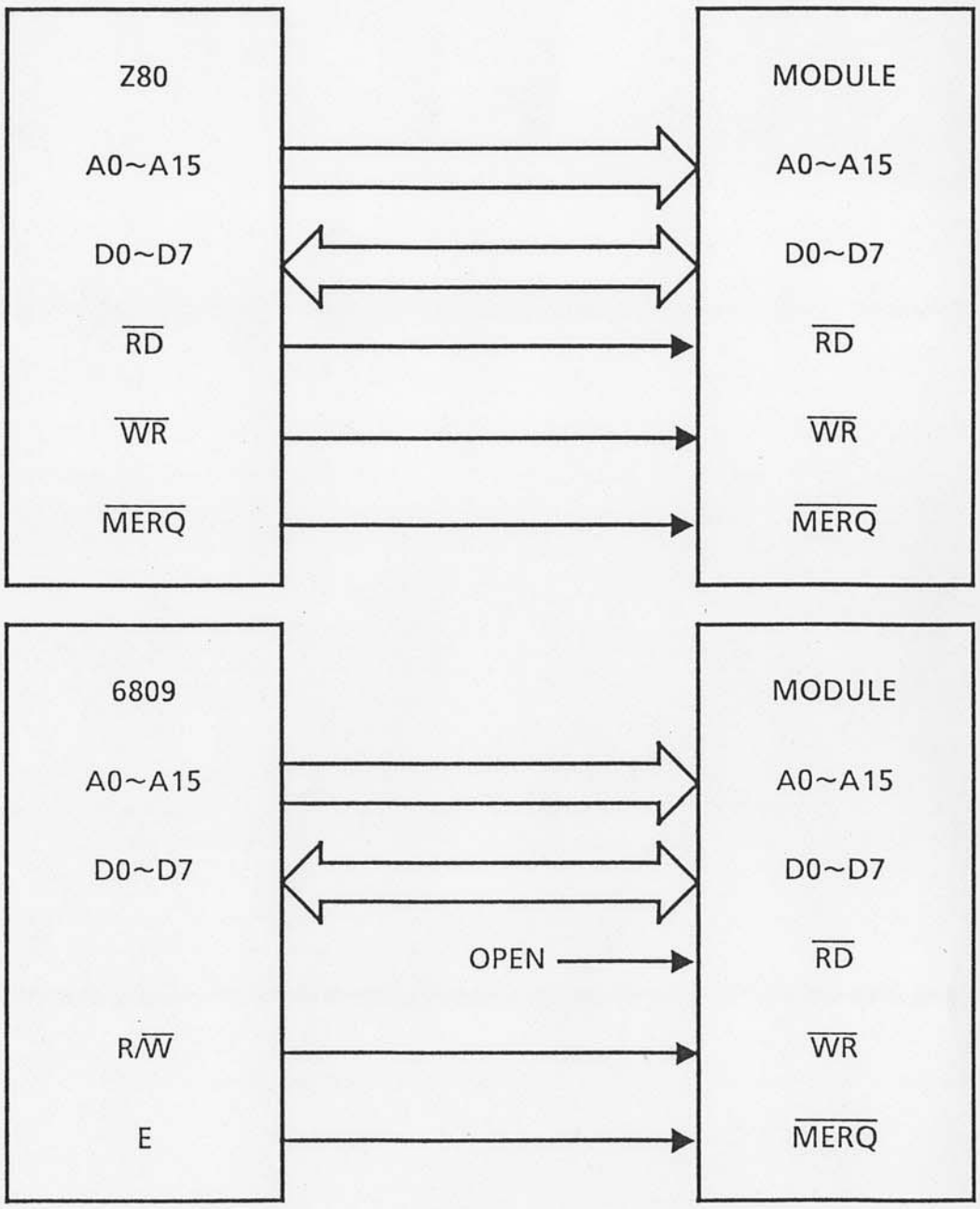


FIG.8 INTERFACE CONNECTION

JP2 selects CPU.

Z80 becomes available by making 0 of JP2 short-circuited.

6809 becomes available by making 1 of JP2 short-circuited.

11. CAUTIONS FOR OPERATION

1. The VFD component of the module is made of glass.
   Careful handling is essential.

2. Confirm the supply voltage is within the specified value.
   Excceding the specified value may disturb proper operation or damage the circuit.

3. Never connect or disconnect the interface connector with the supply voltage applied.

4. Avoid module usage in environments with high noise levels.
   This will cause undesirable interference on the input signals and disturb the operation.
   Keep the cable length for the input signal within 40cm.

★ REMARKS ★

This specification is subject to change without any prior notice.
Please contact us for the latest details before you use the module.