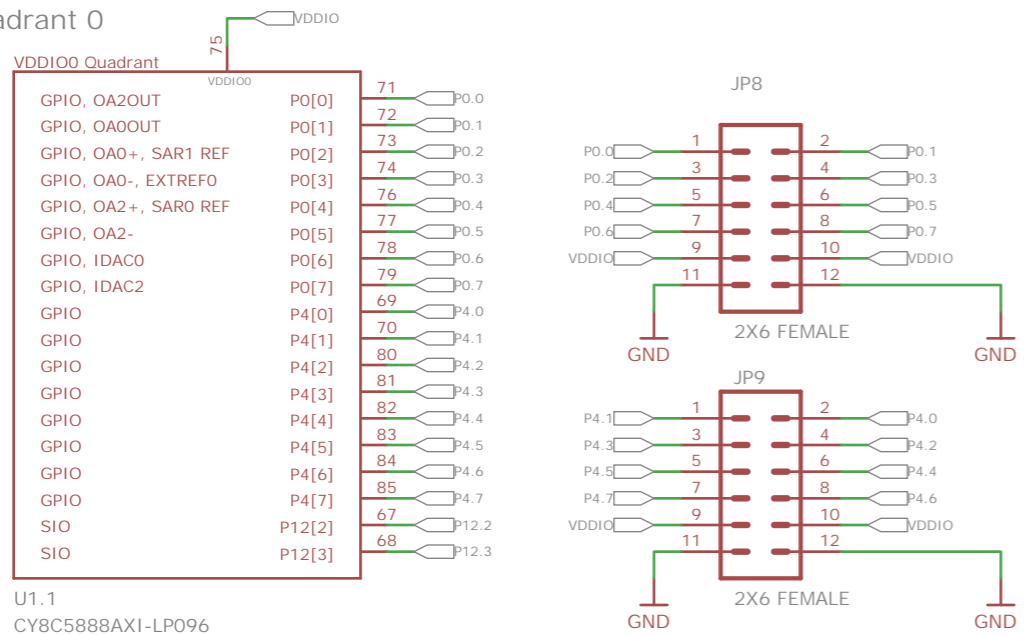
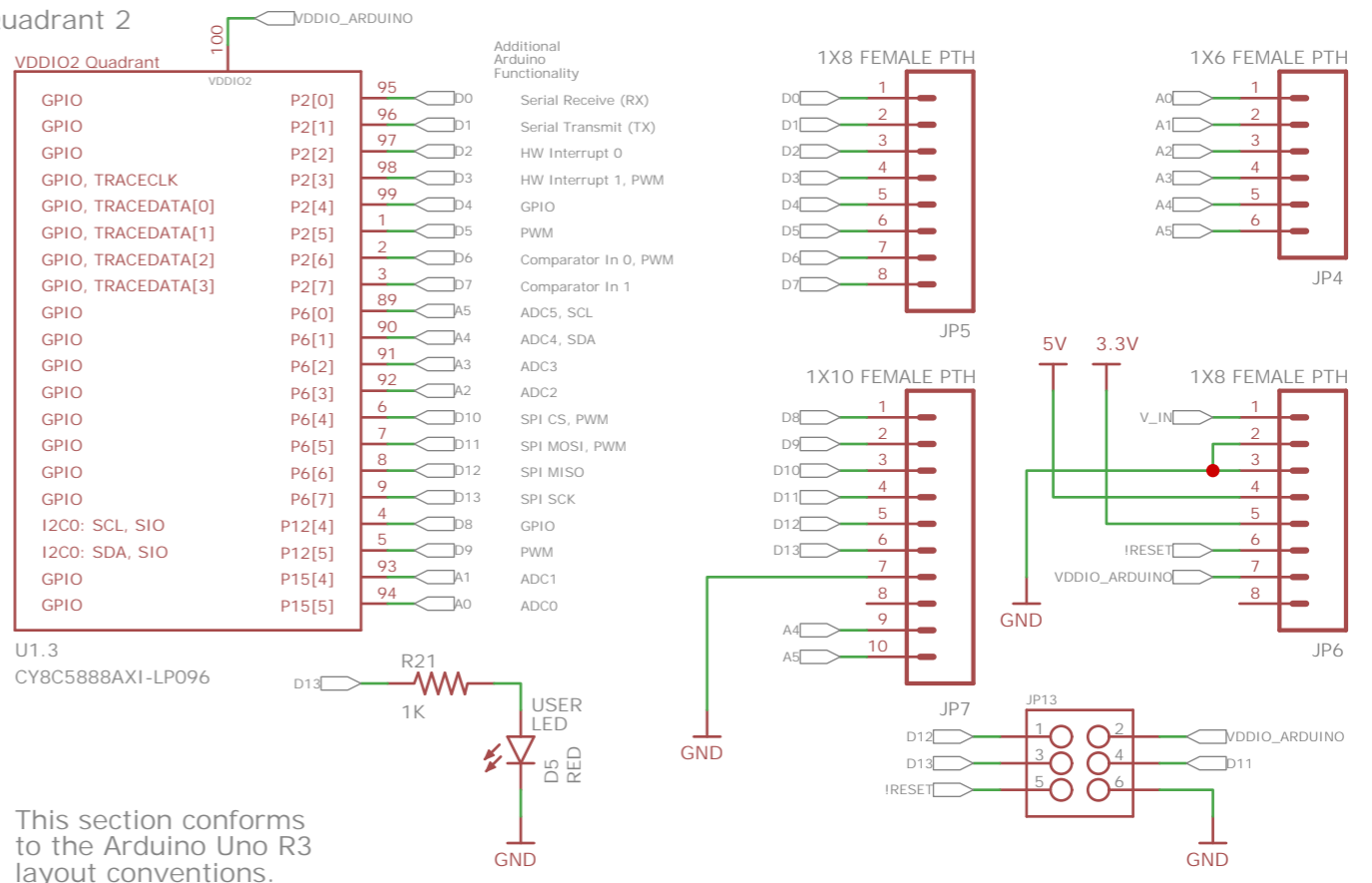


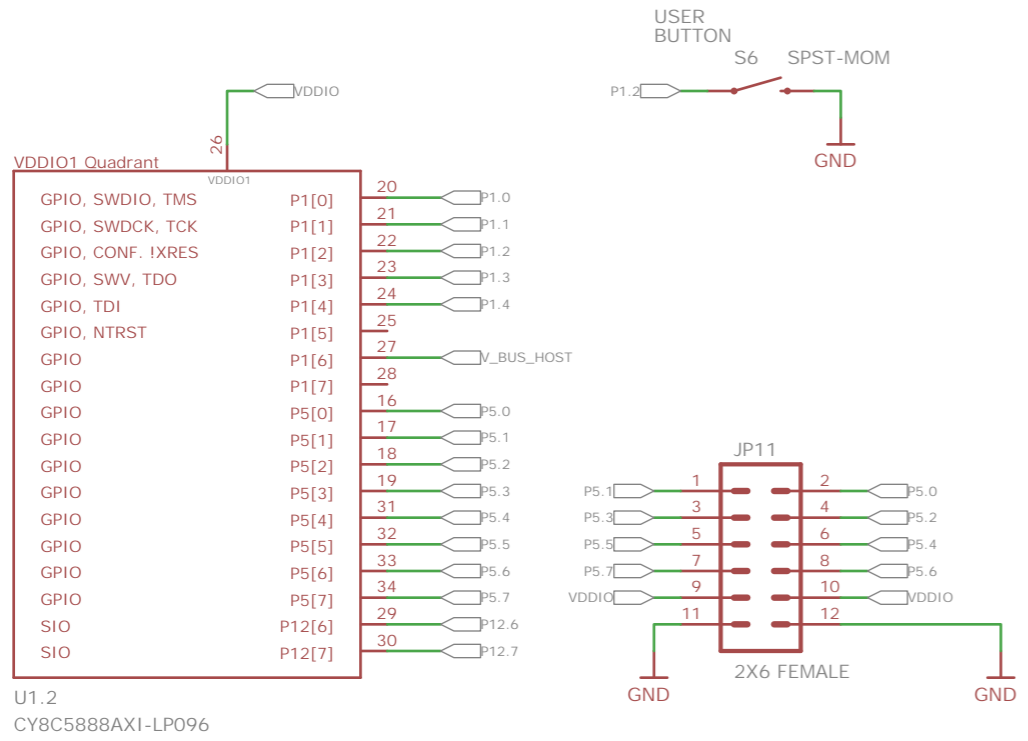
Quadrant 0



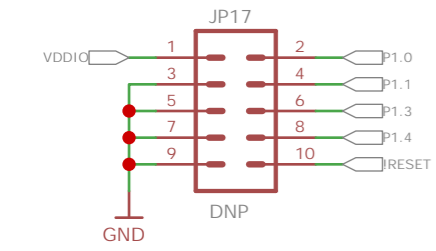
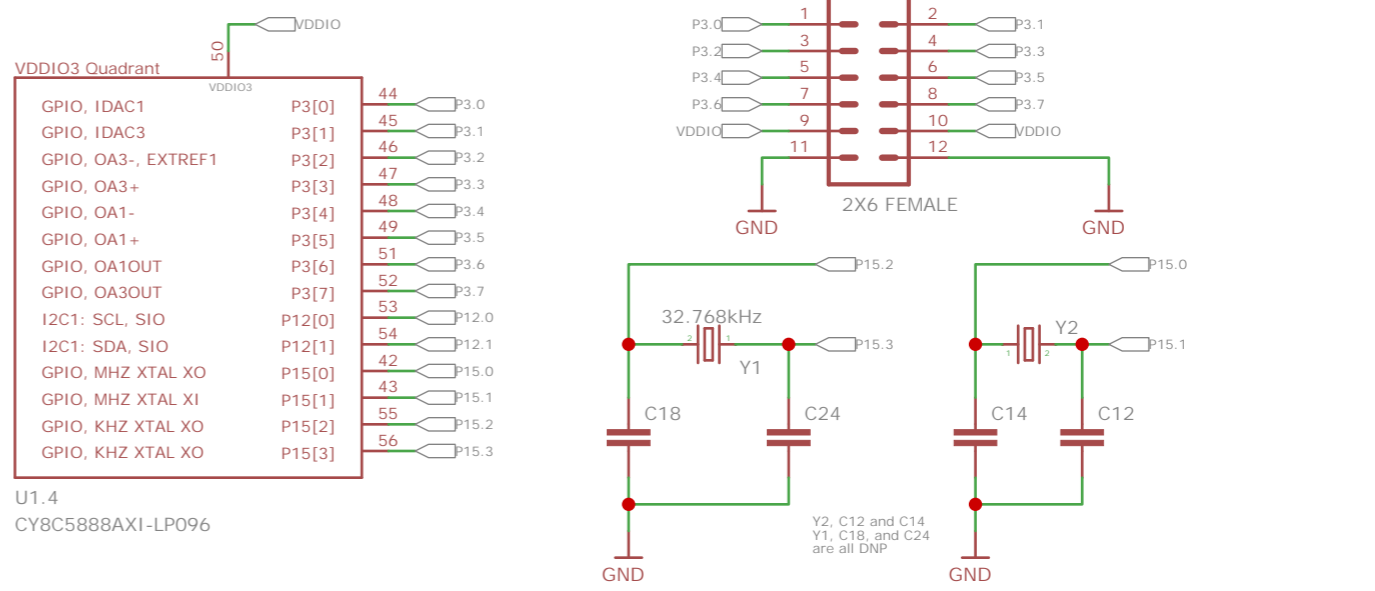
Quadrant 2



Quadrant 1

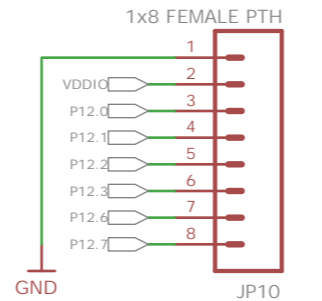


Quadrant 3



Developed with help from Jon Moeller and Cypress Semiconductor

Port 12 (SIO pins)



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TITLE: >DRAWING_NAME

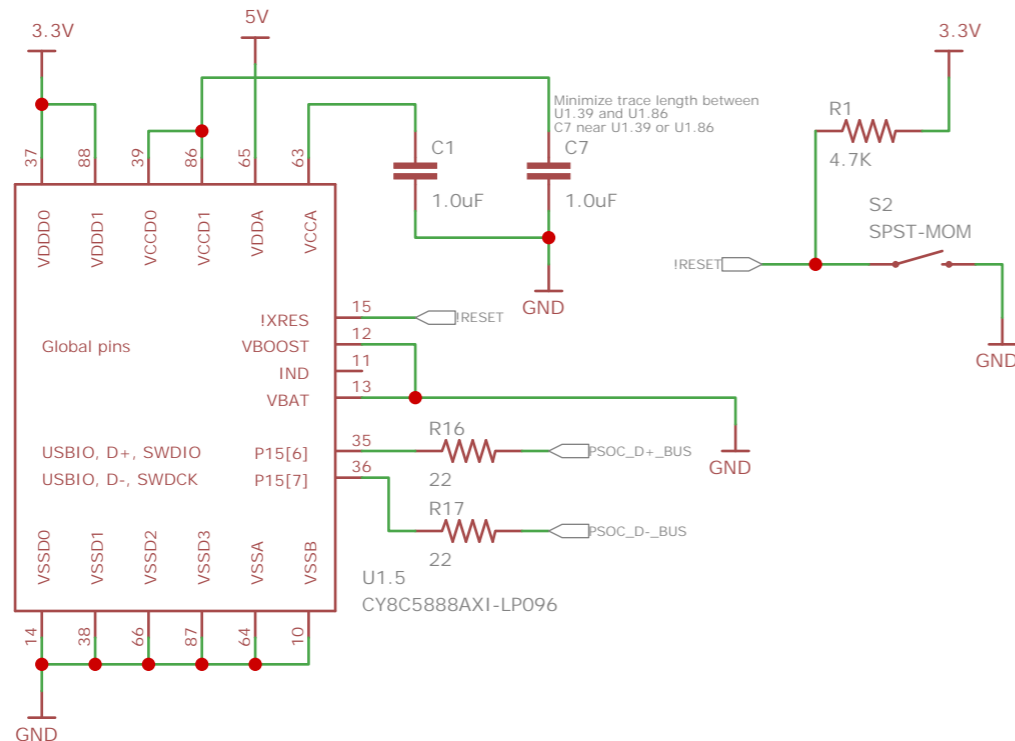
Design by: Mike Hord

Date: >LAST_DATE_TIME

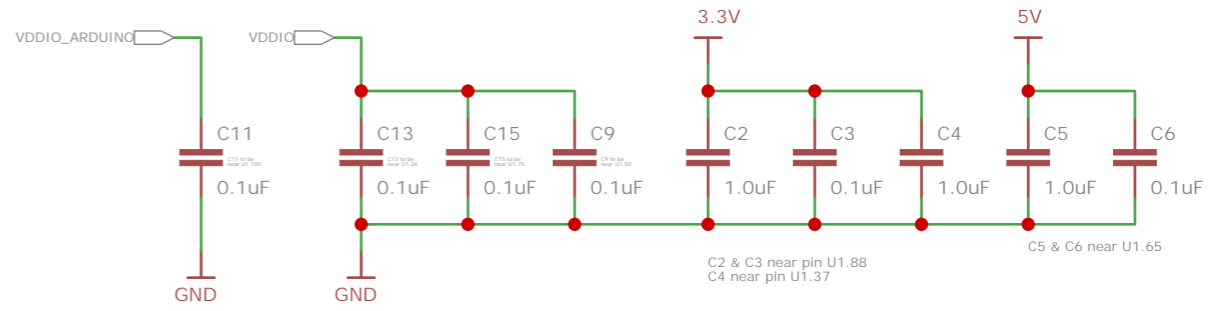
THIS IS A FOUR-LAYER BOARD!

REV: 14

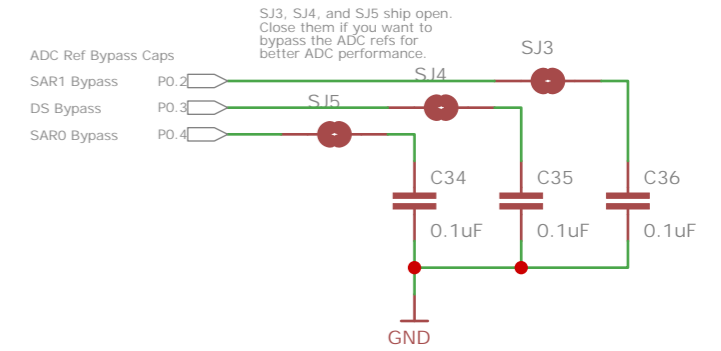
Sheet: >SHEET



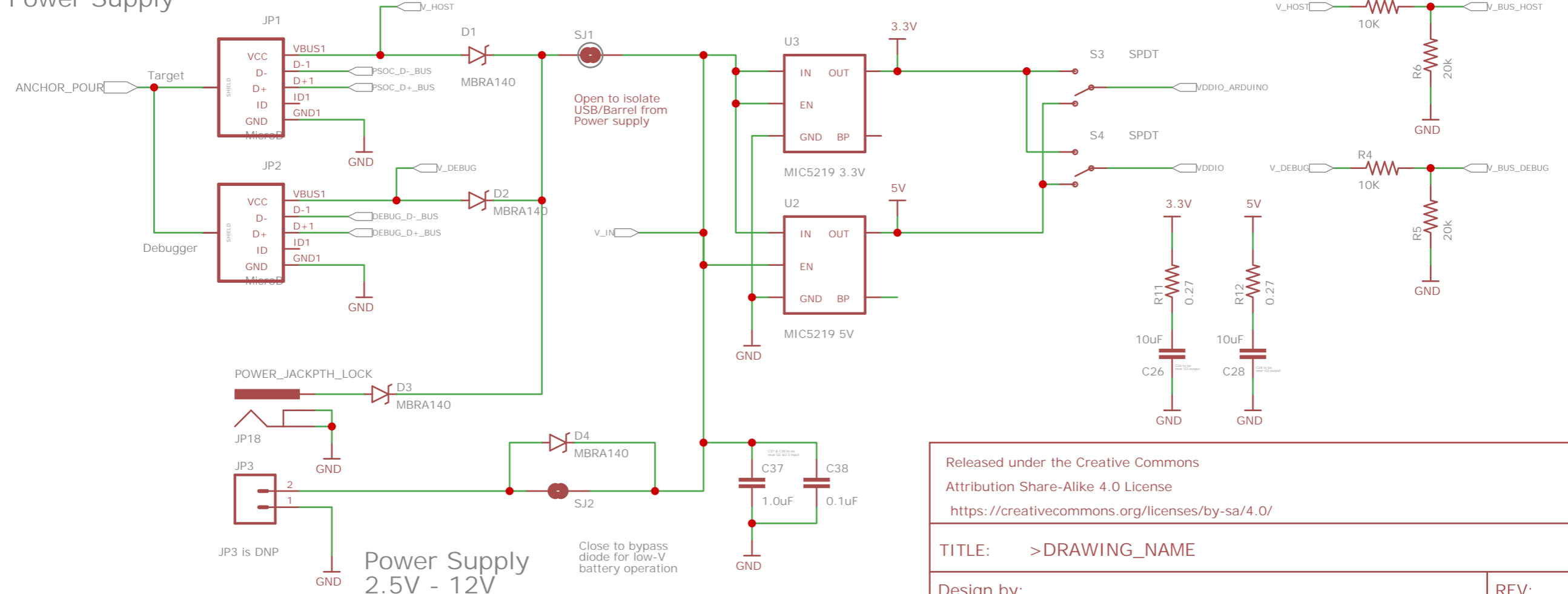
Target Supply Pins



Target Device Decouple/Bypass Caps



Power Supply

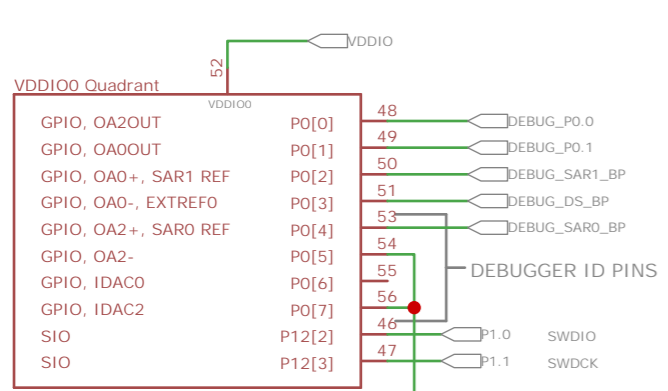


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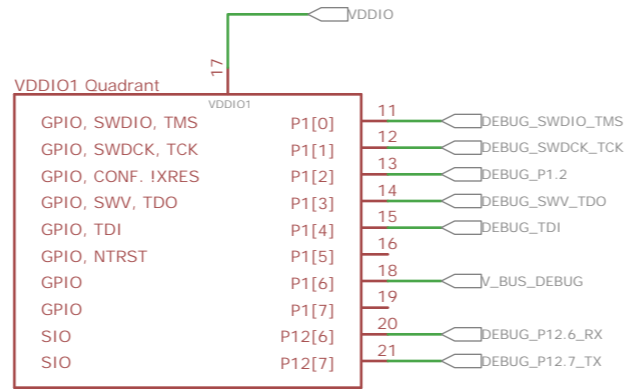
TITLE: >DRAWING_NAME

Design by: Mike Hord
 REV: 14

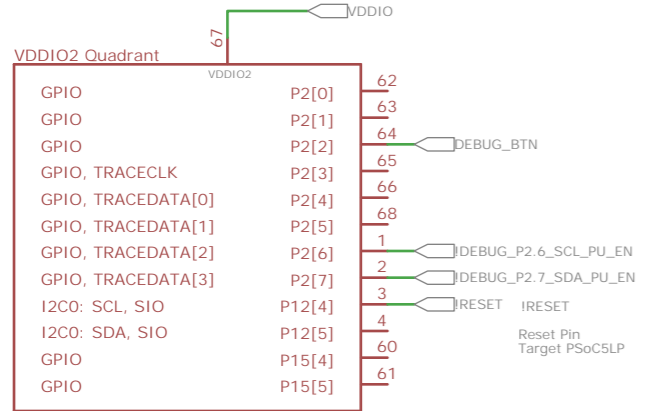
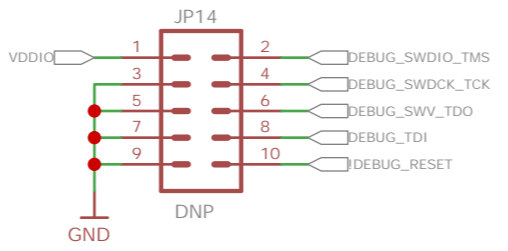
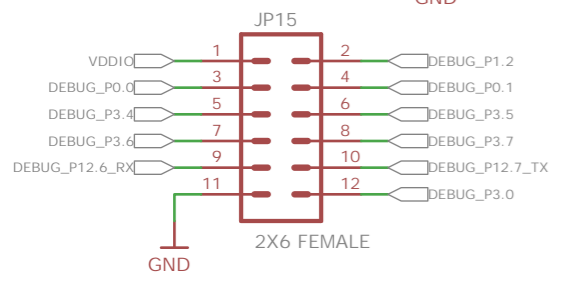
Date: >LAST_DATE_TIME
 Sheet: >SHEET



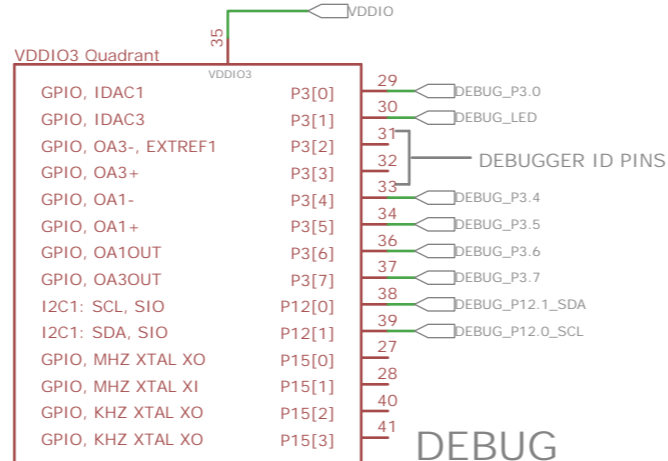
U7.1
CY8C5868LTI-LP039



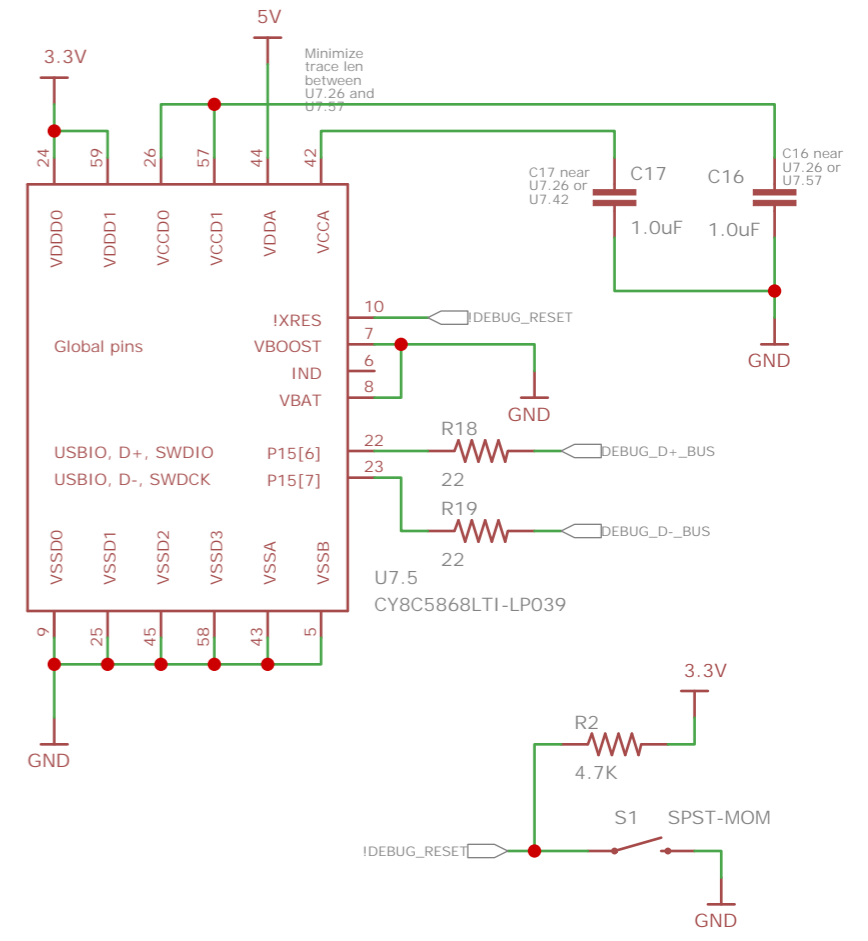
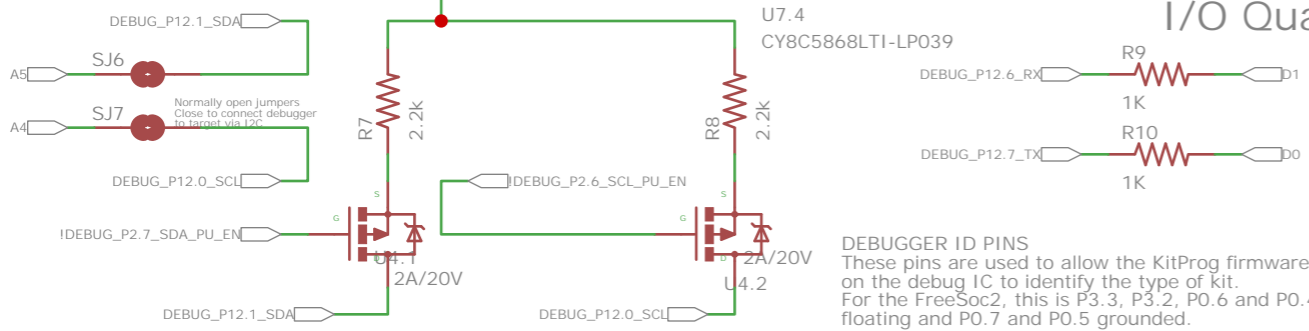
U7.2
CY8C5868LTI-LP039



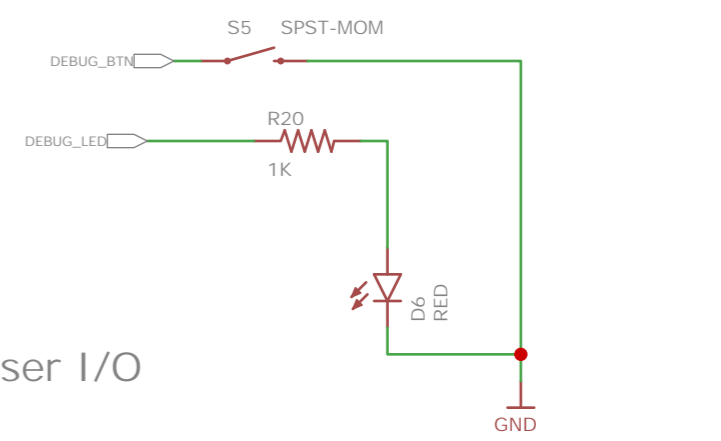
U7.3
CY8C5868LTI-LP039



U7.4
CY8C5868LTI-LP039

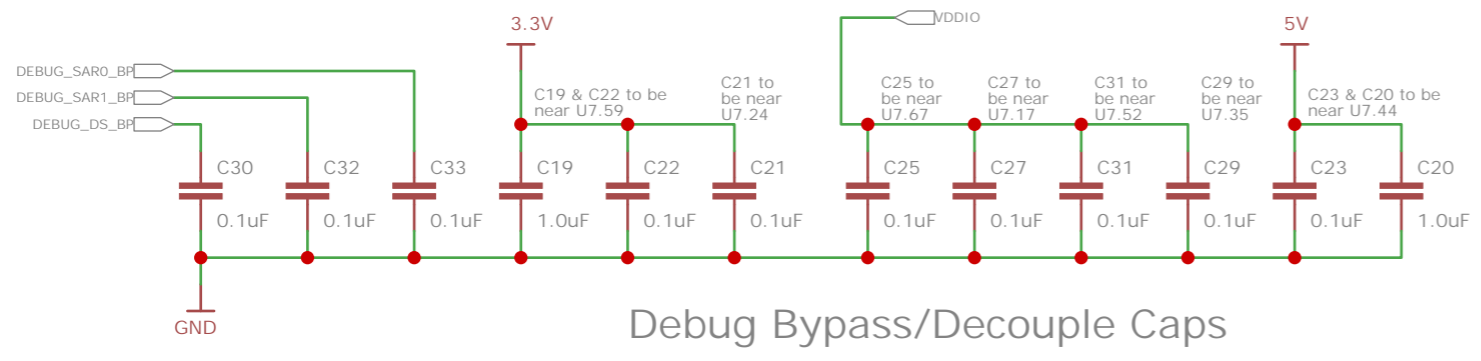


Debug Power Pins



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TITLE: >DRAWING_NAME		REV: 14
Design by: Mike Hord		
Date: >LAST_DATE_TIME	Sheet: >SHEET	



Debug Bypass/Decouple Caps