

1. Introduction

This document illustrates how to setup the 8 Mega Pixel Digital Camera demo on the DE10-Nano and the D8M-GPIO as shown in **Figure 1**. The basic design content is also included. In this demonstration, the HPS DDR3 is used. For details about how to use the HPS DDR3, please refer to the DE10-Nano user manual. For details about the D8M-GPIO, please refer to the user manual of D8M-GPIO daughter card.

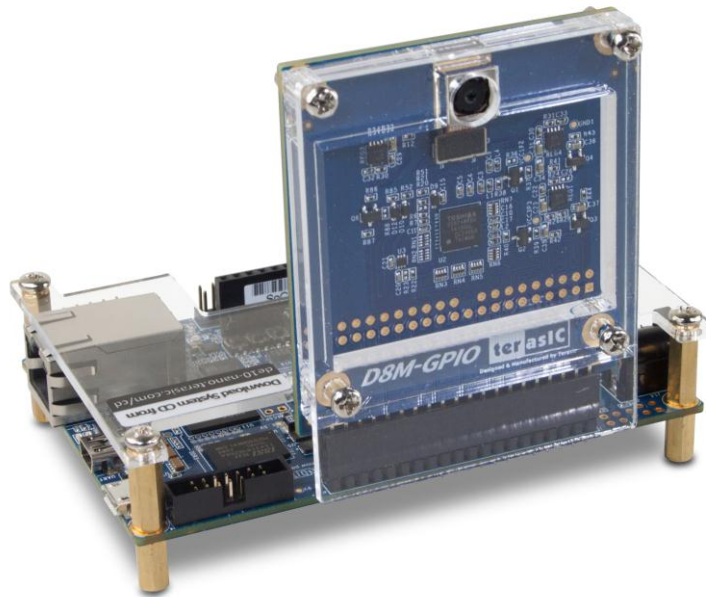


Figure 1 8 Mega Pixel Digital Camera Demo

2. System Requirements

The following items are required to perform this demonstration:

- DE10-Nano and power supply
- One MicroSD Card and card reader
- D8M-GPIO daughter card
- One HDMI monitor

3. Execute Demonstration

The MicroSD card should be programmed by Win32DiskImager.exe with the SD Card image terasic_hps_dds3.img located in the folder:

DE10-Nano CD/Demonstrations/FPGA/SdcardImage

Please follow the procedures below to setup the demonstration by using

DE10_Nano_D8M_DDR3.sof to config the FPGA:

1. Make sure both Quartus Prime and USB-Blaster II driver are installed on the host PC.
2. Program terasic_hps_ddr3.img into a microSD card.
3. Power off the DE10-Nano board.
4. Insert the microSD card into the DE10-Nano board.
5. Make sure the MSEL[4:0] is set to 01010.
6. Connect a mini-USB cable to an UB2 port of the DE10-Nano and the host PC.
7. Mount the D8M-GPIO onto the 2x20 GPIO_0 expansion header of the DE10-Nano.
8. Connect the HDMI output to an HDMI monitor.
9. Power on the DE10-Nano Board.
10. Wait for the HPS LED0 on the DE10-Nano to become lighted. This indicates the DDR3 is ready.
11. Make sure Quartus Prime 16.0 or later is installed on your host PC.
12. Launch the “test.bat” from the folder demo_batch of the DE10_Nano_D8M_DDR3 Project.
13. Now, you should see the HDMI monitor start showing the video captured from the camera.
14. Press KEY0 to trigger the system reset.
15. Press KEY1 to trigger the auto-focus function

4. Project Description

Figure 2 shows the system block diagram of this demonstration design. DE10_Nano_D8M_DDR3 reference design is developed based on Altera’s Video and Image Processing (VIP) Suite, and the HPS_DDR3 is used as video memory. The Terasic Camera IP translates the parallel Bayer pattern data into RGB data to meet the specification of the Altera VIP video streaming. The Frame Buffer II from VIP is used for buffering image data in DDR3 and matching the frame rate from the Terasic camera IP to the Clocked Video Output of VIP. The FOCUS_ADJ is used to get a better image quality by finding the optimized focus setting.

The project is built by Quartus Prime 16.0.2 Standard Edition. If developers want to recompile the project, the same Quartus build is recommend for best compatibility.

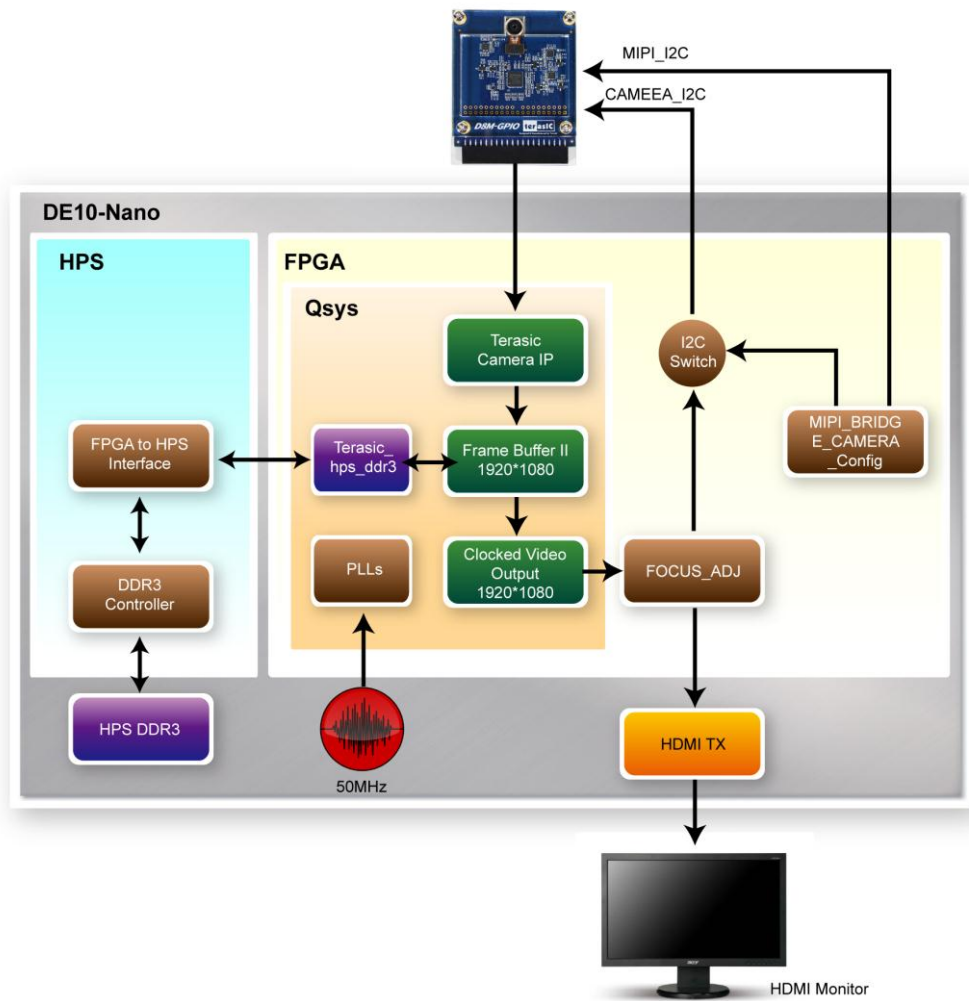


Figure 2 System Block Diagram