APPLICATION NOTE

Digital Video Decoder/Encoder Module System

AN96055

Philips
Semiconductors

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Digital Video Decoder/Encoder Module System

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Abstract

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The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analogue and digital signal processing.

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Digital Video Decoder/Encoder Module System

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Keywords

SAA7110(A) / SAA7111(A), OCF / VIP
Digital Video Decoder
SAA7124/25
SAA7182/83
SAA7182A/83A
Digital Video Encoder (DENC)
I²C Bus
MultiMedia

Date: 31th May 1996

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Summary

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The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

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CONTENTS

1. Introduction

The Digital Video Decoder/Encoder Modules provide the basis to evaluate various Philips digital video decoders and encoders and give the opportunity to simply insert the modules into customized applications and systems.

On the following pages the schematics of the Digital Video Decoder Module DECMOD01 and Digital Video Encoder Module ENCMOD02 are shown. Both modules can be operated in stand alone operation (interconnected directly) as well as extension to other systems like PCI-bridges, MPEG decoders or Video input/output systems.

Each module has a socket for an I²C-bus EEPROM (e.g. PCF8582, PCF8594, PCF8598, X24164) in order to store data for initialization and for simple control functionality operated by a (future) microcontoller module. Software for IBM compatible personal computers enables access to all features and settings of the devices. It handles the I²C-bus via a printer port adapter.

This modular concept was designed to combine different video decoders with various video encoders. Each module can be configured for several devices and packages without the necessity of having a new PCB. This could be achieved by using multiple footprints for one IC and some configurational parts. For interfacing a 26-pin and a 16-pin flat ribbon cable connector is used. The 26-pin YUV-Feature Connector is used for the signal path while the other one is used for power supply and I²C-bus.

2. Digital Video Decoder Module DECMOD01

The digital decoder module DECMOD01 contains the decoder types SAA7110(A) or SAA7111(A) and allows the assembly of PLCC68 and LQFP64 packages.

The module has two RCA jacks for CVBS input signals and a DIN connector for S-Video input. For the 3.3V device SAA7111A the input termination is constructed as resistor divider (27R + 47R) to meet the input voltage range of approx. 0.7Vpp. For all other devices the series resistor is 0R and the termination 75R. The coupling capacitors are 22 nF for SAA7111A and 10 nF for all other. As crystal a 3rd order type is used for SAA7110(A) and SAA7111 (see data sheets for details on crystal parameters).

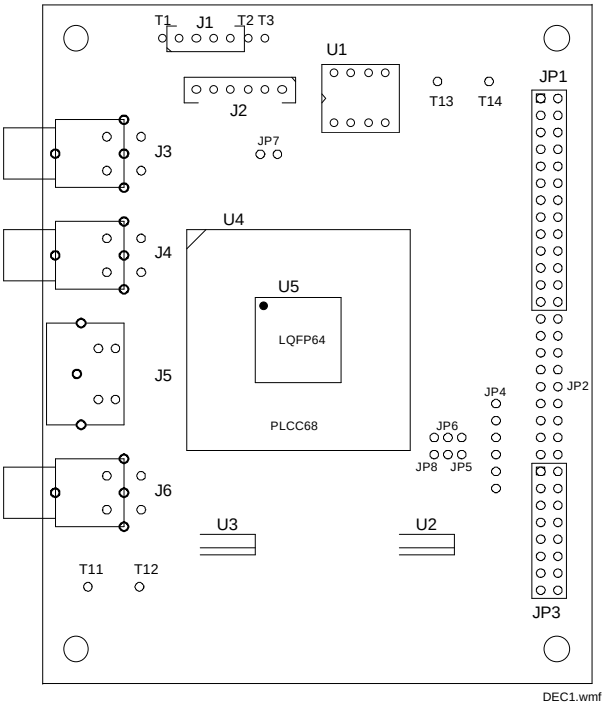


Fig.1 Location of ICs, jumpers and connectors on the DECMOD01 PCB

The digital output port is fed to the YUV-Feature Connector. It is possible to insert SMD resistors into the lines to suppress high frequent ringing due to long wires (resistor arrays U6, U7). This holds also for clock and sync. outputs. The I²C-bus can be fed via the 16 pin connector JP3 (install jumpers JP5 and JP6) and/or via 4pin connector J1 which can be assembled in various pinning schemes using additionally pins (T1~T3). R17 and R20 are foreseen to add serial resistors for protection purpose. Resistors R18, R19 and R33 are foreseen to adapt the slightly different pinning of SAA7110(A) and SAA7111.

For the different board configurations see tables below.

TABLE 1 Power Supply

Part	SAA7110(A), SAA7111	SAA7111A	Remark
U2	OPEN	3.3V regulator	digital supply
R12	0R	OPEN	digital supply
U3	5V regulator	3.3V regulator	analog supply

The separate voltage regulator for the analog supply is to ensure a clean power supply for the analog part even when using long wires to the module

TABLE 2 Differencies in Pinning Schemes and Part Values

Part	SAA7110(A)	SAA7111	Pin (PLCC68)	Remark
R18	0R	OPEN	12	VDDA4 for SAA7110(A)
R19	OPEN	10k	12	pull-up TDI for SAA7111
R33	0R	OPEN	10	AGND4/nc
X1	26.800 MHz	24.576 MHz		crystal

TABLE 3 Configuration DECMOD01

Part	Value	Description
JP7	**closed** open	**slaveaddress 9Ch for SAA7110, 48h for SAA7111(A)** slaveaddress 9Eh for SAA7110(A), 4Ah for SAA7111(A)
JP8	closed **open**	only for SAA7111(A): CE pin (chip enable) if pin is low (JP8 closed) chip in tristate mode (reset)
JP2		additional pins for using a 60 pin header for JP1, JP2 and JP3
JP4		additional testpins connected to reserved pins on JP3
R29	open	FEIN input connected to DIR pin on feature connector
R30	0R	HREF
R31	0R	HS
R32	0R	VS
R34	0R	LLC
R36	0R	LLC2
R37	0R	CREF
R38	0R/open	connection AGND to DGND near decoder
J2	BSCAN	boundary scan connector for SAA7111, SAA7111A
J6	AOUT	connector only for test purposes

Remark:

the parts mentioned in Table 3 are only for evaluation pupose and can be left out in an application

Performance reports are available on request for the SAA7110(A) and SAA7111.

3. Digital Video Encoder Module ENCMOD02

The digital encoder module ENCMOD02 contains the encoder types SAA7182/83, SAA7182A/83A or SAA7124/25 and allows the assembly of PLCC84, QFP80 and LQFP64 package. The digital data is fed via the 26-pin YUV Feature Connector, power and I²C-bus via 16-pin header. Depending on the assembled IC the data can be in CCIR 656 format (D1) or 16-bit YUV (SAA7182/83/82A/83A only). The outputs of the D/A converters are fed through analog postfilters to the connectors. Depending on the signal type the serial resistor varies. Therefor the filters are assigned to the connectors and the signals out of the D/A converters are routed via jumpers to adapt the different output modes of the SAA7124/25 (JP16, JP17, JP18; see tables below).

On connector J1 On-Screen-Display (OSD) signals can be fed to the encoders SAA7182/83/82A/83A. The SAA7182A/83A also features RGB input pins which are connected to J3 via optional resistor dividers to adapt the input voltage range.

The clock and synchronization signals can be fed to the encoder via jumper (JP10, JP11, JP14, JP15) when operating the slave mode (pin CDIR high; JP13 open). Using the encoder as clock master (pin CDIR low; JP13 closed) LLC and CREF are outputs. The pins RCV1 and RCV2 can be configured to outputs via I²C-bus setting (see I²C-bus register 6Bh in datasheets) to provide horizontal and vertical synchronization signals.

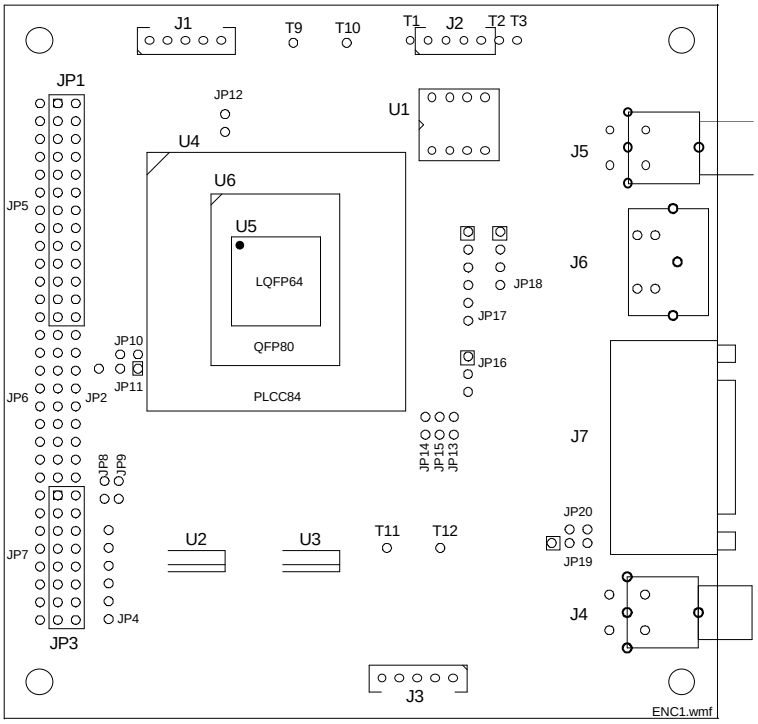
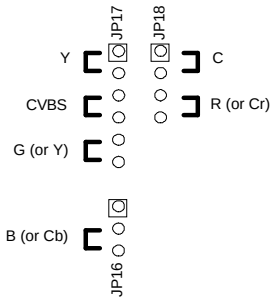
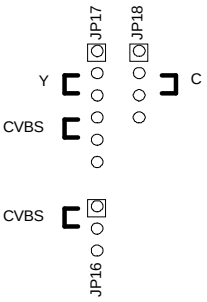


Fig.2 Location of ICs, jumpers and connectors on the ENCMOD02 PCB



RGB (or YUV) mode



S-Video mode
(SAA7124/25 only)

The jumper configuration for the S-Video mode is only for the SAA7124/25. This mode can be configured via I²C-bus. The four D/A converters deliver Y,C and two times CVBS.

The configuration for RGB mode can be used for all devices. In this configuration the four D/A converters of the SAA7124/25 can deliver either CVBS and RGB signals or CVBS and analog YUV signals (Y and C is not available). Additionally the SAA7182/83/82A/83A delivers S-Video output signals (Y and C).

TABLE 4 Power Supply

Part	SAA7124/25, SAA7182/83	SAA7182A/83A	Remark
U2	OPEN	3.3V regulator	digital supply
R12	0R	0R	digital supply
R14	0R	OPEN	digital supply
U3	5V regulator	3.3V regulator	analog supply

The separate voltage regulator for the analog supply is to ensure a clean power supply for the analog part even when using long wires to the module

TABLE 5 Configuration ENCMOD02

Part	Value	Description
JP12	**closed** open	**slaveaddress 88h** slaveaddress 8Ch
JP13	closed **open**	CDIR pin (clock direction): pins LLC and CREF are outputs and the internal oszillator will be used if CDIR is low (JP13 closed)
JP2		additional pins for using a 60 pin header for JP1, JP2 and JP3
JP4		additional testpins connected to reserved pins on JP3
JP5 JP6 JP7		additional pins for using reverse connectors
R33	open	termination CREF
R34	open	termination LLC
R35	0R	connection AGND to DGND near encoder
JP14		jumper CREF
JP15		jumper LLC
JP11		HS/HREF to/from RCV2
JP10		VS to/from RCV1
J2	OSD	OSD connector for SAA7182/83(A)
J3	RGBin	RGB input connector for SAA7183A R15,16,17,18,23,24,26,27 used to adapt input voltage range
T5	RESN	testpin (active low reset input)
T7	TTXRQ	testpin (output signal for teletext request)
T8	TTX	testpin (input signal for teletext data)
R25/R28	0R	I²C-bus serial resisitors for protection
JP16	1-2 2-3	S-Video-Mode (SAA7124/25 only) RGB-Mode
JP17	1-2, 3-4, 5-6 2-3, 4-5	RGB-Mode S-Video-Mode (SAA7124/25 only)
JP18	1-2, 3-4 2-3	RGB-Mode S-Video-Mode (SAA7124/25 only)
JP19	1-2 2-3	HSYNC to J7 pin13 (VGA connector) CVBS to J7 pin14 (VGA connector)
JP20	closed	VSYNC to J7 pin14 (VGA connector)

Remark:

the parts mentioned in Table 5 are only for evaluation pupose and can be left out in an application

4. I²C-bus EEPROM on DECMOD01 and ENCMOD02

The IC U1 on each module can be assembled with different IC types depending on the desired memory size. Additionally the I²C-bus device address can be adapted by soldering corresponding SMD resistors which is described in the tables below.

TABLE 6 Configuration of I²C-bus EEPROMs

IC type	Size	Pin 1	Pin 2	Pin 3	Pin 7	Address Range
PCF8582x-2	256 bytes	**A0:** "0" "1" "0" "1" "0" "1" "0" "1"	**A1:** "0" "0" "1" "1" "0" "0" "1" "1"	**A2:** "0" "0" "0" "0" "1" "1" "1" "1"	PTC	A0h **or** A2h **or** A4h **or** A6h **or** A8h **or** AAh **or** ACh **or** AEh
PCF8594x-2	512 bytes	WP	**A1:** "0" "1" "0" "1"	**A2:** "0" "0" "1" "1"	PTC	A0h and A2h **or** A4h and A6h **or** A8h and AAh **or** ACh and AhE
PCF8598x-2	1024 bytes	WP	n.c.	**A2:** "0" "1"	PTC	A0h, A2h, A4h and A6h **or** A8h, AAh, ACh and AEh
X24164	2048 bytes	**S0:** "0" "1" "0" "1" "0" "1" "0" "1"	**S1:** "1" "1" "0" "0" "1" "1" "0" "0"	**S2:** "0" "0" "0" "0" "1" "1" "1" "1"	TEST	80h, 82h, 84h, 86h, 88h, 8Ah, 8Ch and 8Eh **or** 90h, 92h, 94h, 96h, 98h, 9Ah, 9Ch and 9Eh **or** A0h, A2h, A4h, A6h, A8h, AAh, ACh and AEh **or** B0h, B2h, B4h, B6h, B8h, BAh, BCh and BEh **or** C0h, C2h, C4h, C6h, C8h, CAh, CCh and CEh **or** D0h, D2h, D4h, D6h, D8h, DAh, DCh and DEh **or** E0h, E2h, E4h, E6h, E8h, EAh, ECh and EEh **or** F0h, F2h, F4h, F6h, F8h, FAh, FCh and FEh

TABLE 7 Board Configuration for I²C-bus EEPROMS

Pin	"0"	"1"	Remark
PTC or TEST	R4: OPEN R8: 0R	R4: 0R R8: OPEN	Leave pin PTC open; apply "0" to pin TEST
A2 or S2	R5: OPEN R9: 0R	R5: 0R R9: OPEN	
A1 or S1	R6: OPEN R10: 0R	R6: 0R R10: OPEN	pin S1 (X24164) is inverted internally
WP, A0 or S0	R7: OPEN R11: 0R	R7: 0R R11: OPEN	WP: "1" --> write protect of upper 256[512] bytes "0" --> write enabled (only PCF8594[PCF8598])

5. Module System Connectors

The YUV connector (feature connector) provides access to the digital YUV data input coming from a digital video decoder or from an MPEG video source supplied to a video encoder. Two YUV data formats are supported, 16-bit “decoder format” or 8-bit CCIR656 compatible (D1). The control lines are set either as inputs or outputs. The connector has the following pin assignment:

Pin 1, 3, 5, 7, 9, 11, 13, 15	UV0: UV7 digital UV data
Pin 2, 4, 6, 8, 10, 12, 14, 16	Y0: Y7 digital Y data **or** digital CCIR656 data
Pin 17	LLC digital clock
Pin 18	LLC2
Pin 19	CREF, clock reference
Pin 20	HREF, optional horizontal reference (blanking)
Pin 21	RTC, real time control
Pin 22	HS, horizontal synchronisation pulse
Pin 23	digital ground
Pin 24	VS, vertical synchronisation pulse
Pin 25	DIR
Pin 26	digital ground

The 16-pin header for power supply and I²C-bus has the following pin assignment:

Pin 1	SCL
Pin 2	SDA
Pin 3, 4, 9, 10, 15, 16	reserved for future use
Pin 5, 6	digital power supply (5V)
Pin 7, 8	digital groundl
Pin 11, 12	analog power supply (12V)
Pin 13, 14	analog ground

On each module in addition (or as alternative) a 4 pin connector can be used for I²C-bus control:

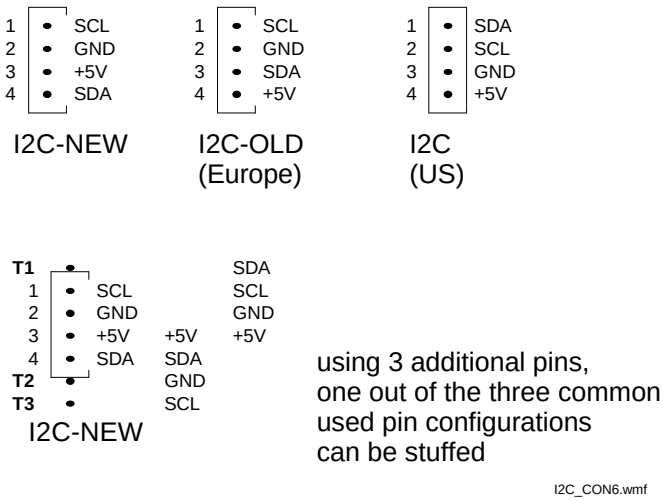


Fig.3 I²C-bus connector pinnings

Note: always supply the I²C-bus with pull-up resistors, but avoid too high currents (see I²C-bus specification)
On each module pull-up resistors can be added (R1 and R2), but preferably only one pull-up should be done on the I²C-bus master IC.

6. Desktop Video Evaluation Board DTV7183

SAA7110(A) or SAA7111; PLCC68 (Digital Video Decoder)
SAA7185 or SAA7187 or SAA7188A or SAA7184/85B; PLCC68 (Digital Video Encoder)
SAA7182/83; QFP80 (Digital Video Encoder); note: only samples for demo purposes in this package!

The DTV7183 Demonstration Board shows the features and the application of the digital video decoder and encoder families.

The board operates in stand alone mode as well as an extension board for other Desktop Video boards. It incorporates the ICs of the digital encoder family SAA7185, SAA7187, SAA7188A and SAA7184/85B, the EURO-DENC SAA7182/SAA7183 and the video decoders SAA7110(A)/SAA7111. The digital datapath is connected to the YUV Feature Connector, which can be used as input or output.

The on-board microcontroller delivers different I²C-bus setups for easy demonstration.

The User Manual HSM/UM95003 gives a detailed description of the board, summarises the control software features and provides the schematics and the board layout.

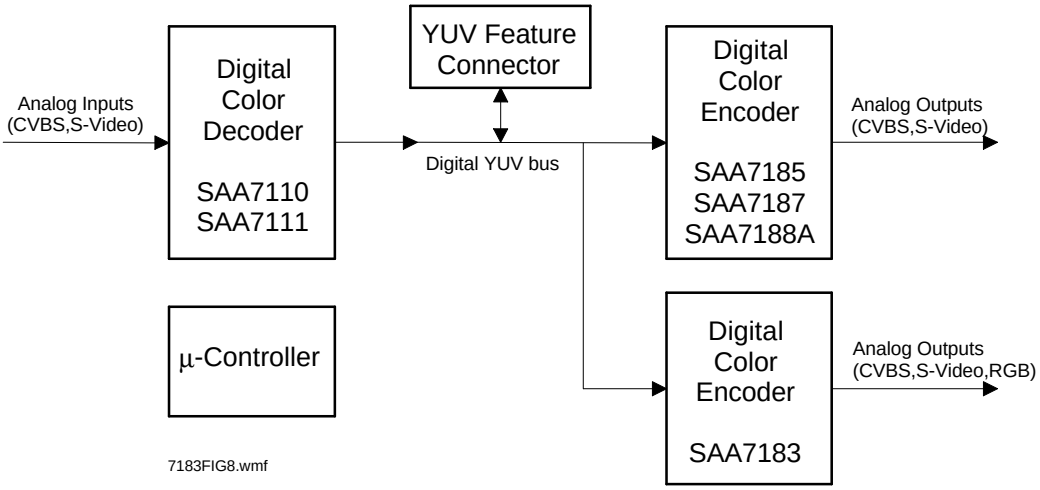


Fig.4 Blockdiagram of the DTV7183 demonstration board

7. Digital Video Encoder Board DENC2

SAA7185 or SAA7187 or SAA7188A; PLCC68

The DENC2 Demonstration Board operates as a stand alone video pattern generator as well as an extension board for the other Desktop Video decoder boards. It incorporates the ICs of the digital encoder famliy SAA7185, SAA7187 and SAA7188A. The digital input data from the YUV Feature Connector is sent directly to the encoder and the processed analog video output signals are CVBS and S-Video.

The on-board microcontroller delivers eigth different I²C setups for easy demonstration.

The User Manual HVS/UM94008 gives a detailed description of the board, summarises the control software features and provides the schematics and the board layout.

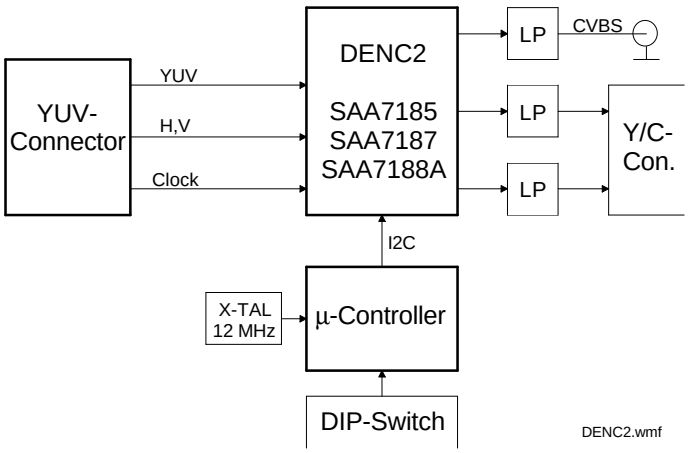


Fig.5 Blockdiagram of the DENC2 board

8. Desktop Video Evaluation Board DTV4

The DTV4 evaluation board demonstrates features and functionality of digital video decoding and encoding devices from Philips Semiconductors. For analog video input the board accepts CVBS, S-VHS as well as RGB in PAL, NTSC or SECAM video standards. Fast RGB/CVBS or RGB/S-VIDEO input switching is provided as an additional feature. On the encoding side the DTV4 board offers CVBS and simultanous S-VHS output in a wide range of PAL and NTSC standards plus full genlock capability.

DTV4 features the following ICs:

SAA7151B (Digital Video Decoder)
SAA7152 (Digital Comb Filter)
SAA7197 (Clock Generator Circuit)
SAA7199B (Digital Video Encoder)
TDA8708A (A/D Converter)
TDA8709A (A/D Converter)

The DTV4 frontend offers a video static switch and a RGB matrix. It comprises I²C bus controlled input switching and RGB fast switch mode.

After digitizing video signals are processed by the digital comb filter, in case of CVBS separated into Y and C and then fed into the digital multi-standard decoder (DMSD) for synchronisation processing, line-locked clock generation and colour decoding. The digital YUV data is stored in a two-field frame memory (FIFO buffer for GENLOCK mode). A memory freeze function is provided. The colour space converter (DCSC) transforms the 16-bit YUV output of the frame memory into 24-bit RGB format. This signal is fed to the triple D/A-converter (TRIDAC) to generate the board´s analog RGB output signal. The same 24-bit RGB signal is used as input for the digital encoder (DENC) to produce genlocked and non-genlocked analog TV standard output signals.

All operation modes can be controlled via I²C-Bus. Various configurations are supported via jumper settings and reprogramming of the relevant devices.

In addition a 26-pin header is provided to allow external connection of digital YUV data between the frame buffer input and DMSD output.

An onboard microprocessor is used to send initial configuration data to all programmable devices via I²C bus (uC master mode) and to operate as a control device for various board functions. The board can be set to different configurations which cover most of the possible modes the board can operate in.

To access all internal registers of the I²C controlled devices on DTV4 the interface has to be connected to the I²C bus and the µC has to be switched to slave mode. Then the board can be fully controlled via the MMCS*) software package (DOS based), which is supplied with each board.

To operate the board inside the PC-AT an interface from AT to I²C bus has been implemented which features the I²C controller PCD8584. Appropriate driver software is also enclosed in the MMCS package.

*) MMCS = MultiMedia Control Software

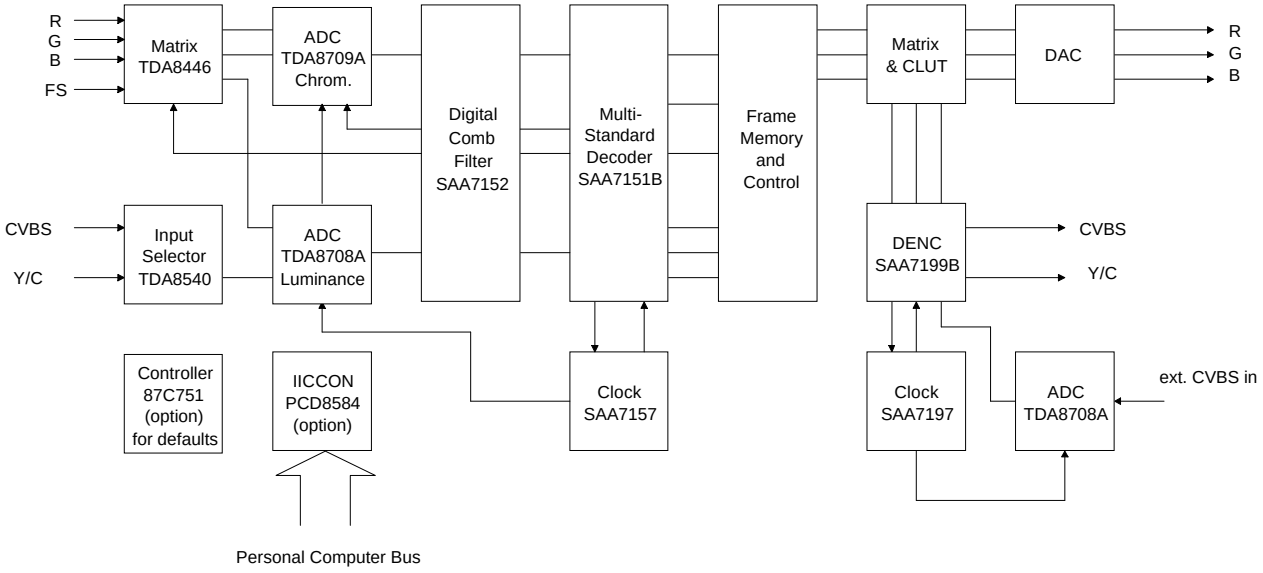


Fig.6 Blockdiagram DTV4 board

9. Tips for a PCB layout with analog and digital signal processing

- use separate ground planes for analog and digital supply in one layer (no overlapping!)
- use separate supply planes for analog and digital with the same shape (or smaller) as ground (no overlap of analog supply with digital ground and vice versa!)
- if there are different (asynchronous) clock domains, use separate ground and supply planes (place the analog areas not in a direct neighbourhood; separate the clock domains)
- always use the inner layers for ground and supply planes (no signal layer in between!)
- try to keep digital signals away from analog areas
- place analog areas close to the border of a PCB
- avoid long tracks for analog signals
- place decoupling capacitors (22nF to 100nF) close to the power pins of the ICs
- prepare several provisions for connecting places for analog and digital ground on the PCB for further optimization on the final board

10. Programming tables for SAA7111, SAA7182/83 and SAA7184/85B/88A

SAA7184/85B:
- init data NTSC

Slave:	8Ch
Sub	Data
3Ah	0Fh
3Bh	00h
3Ch	00h
3Dh	00h
3Eh	00h
3Fh	00h
40h	00h
41h	00h
42h	6Bh
43h	00h
44h	00h
45h	52h
46h	90h
47h	12h
48h	2Ah
49h	26h
4Ah	90h
4Bh	11h
4Ch	B6h
4Dh	A2h
4Eh	EAh
4Fh	4Ah
50h	5Eh
51h	D1h
52h	DAh
53h	70h
54h	A9h
55h	70h
56h	EEh
57h	90h
58h	00h
59h	00h
5Ah	00h
5Bh	**76h**
5Ch	**A5h**
5Dh	**3Ch**
5Eh	**3Ah**
5Fh	00h
60h	00h
61h	**11h**
62h	**66h**
63h	**1Fh**
64h	**7Ch**
65h	**F0h**
66h	**21h**
67h	55h
68h	56h
69h	67h
6Ah	58h
6Bh	91h
6Ch	20h
6Dh	07h
6Eh	28h
6Fh	00h
70h	84h
71h	E8h
72h	88h
73h	60h
74h	00h
75h	00h
76h	00h
77h	00h
78h	40h
79h	00h
7Ah	**0Ch**
7Bh	**12h**
7Ch	**02h**
7Dh	22h

SAA7184/85B:
- init data PAL

Slave:	8Ch
Sub	Data
3Ah	0Fh
3Bh	00h
3Ch	00h
3Dh	00h
3Eh	00h
3Fh	00h
40h	00h
41h	00h
42h	6Bh
43h	00h
44h	00h
45h	52h
46h	90h
47h	12h
48h	2Ah
49h	26h
4Ah	90h
4Bh	11h
4Ch	B6h
4Dh	A2h
4Eh	EAh
4Fh	4Ah
50h	5Eh
51h	D1h
52h	DAh
53h	70h
54h	A9h
55h	70h
56h	EEh
57h	90h
58h	00h
59h	00h
5Ah	00h
5Bh	**7Dh**
5Ch	**AFh**
5Dh	**2Dh**
5Eh	**3Fh**
5Fh	00h
60h	00h
61h	**06h**
62h	**4Bh**
63h	**CBh**
64h	**8Ah**
65h	**09h**
66h	**2Ah**
67h	55h
68h	56h
69h	67h
6Ah	58h
6Bh	91h
6Ch	20h
6Dh	07h
6Eh	28h
6Fh	00h
70h	84h
71h	E8h
72h	88h
73h	60h
74h	00h
75h	00h
76h	00h
77h	00h
78h	40h
79h	00h
7Ah	**70h**
7Bh	**18h**
7Ch	**34h**
7Dh	22h

SAA7182/83:
- init data NTSC

Slave:	88h
Sub	Data
3Ah	07h
3Bh	00h
3Ch	00h
3Dh	00h
3Eh	00h
3Fh	00h
40h	00h
41h	00h
42h	90h
43h	00h
44h	00h
45h	A9h
46h	70h
47h	EEh
48h	D1h
49h	DAh
4Ah	70h
4Bh	EAh
4Ch	4Ah
4Dh	5Eh
4Eh	11h
4Fh	B6h
50h	A2h
51h	2Ah
52h	26h
53h	90h
54h	52h
55h	90h
56h	12h
57h	6Bh
58h	00h
59h	00h
5Ah	**68h**
5Bh	**76h**
5Ch	**A5h**
5Dh	**3Ch**
5Eh	**3Ah**
5Fh	**3Ah**
60h	00h
61h	**15h**
62h	**66h**
63h	**1Fh**
64h	**7Ch**
65h	**F0h**
66h	**21h**
67h	55h
68h	56h
69h	67h
6Ah	58h
6Bh	20h
6Ch	**28h**
6Dh	**00h**
6Eh	**30h**
6Fh	F1h
70h	80h
71h	E8h
72h	10h
73h	00h
74h	FFh
75h	30h
76h	0Fh
77h	10h
78h	0Fh
79h	10h
7Ah	**12h**
7Bh	**06h**
7Ch	40h
7Dh	00h

SAA7182/83:
- init data SECAM

Slave:	88h
Sub	Data
3Ah	07h
3Bh	00h
3Ch	00h
3Dh	00h
3Eh	00h
3Fh	00h
40h	00h
41h	00h
42h	90h
43h	00h
44h	00h
45h	A9h
46h	70h
47h	EEh
48h	D1h
49h	DAh
4Ah	70h
4Bh	EAh
4Ch	4Ah
4Dh	5Eh
4Eh	11h
4Fh	B6h
50h	A2h
51h	2Ah
52h	26h
53h	90h
54h	52h
55h	90h
56h	12h
57h	6Bh
58h	00h
59h	00h
5Ah	**70h**
5Bh	**6Ah**
5Ch	**7Fh**
5Dh	**2Dh**
5Eh	**BFh**
5Fh	**3Fh**
60h	00h
61h	**0Eh**
62h	**4Bh**
63h	**B2h**
64h	**3Bh**
65h	**A3h**
66h	**28h**
67h	55h
68h	56h
69h	67h
6Ah	58h
6Bh	20h
6Ch	**40h**
6Dh	**00h**
6Eh	**90h**
6Fh	F1h
70h	80h
71h	E8h
72h	10h
73h	00h
74h	FFh
75h	30h
76h	0Fh
77h	10h
78h	0Fh
79h	10h
7Ah	**18h**
7Bh	**38h**
7Ch	40h
7Dh	00h

SAA7182/83:
- init data PAL

Slave:	88h
Sub	Data
3Ah	07h
3Bh	00h
3Ch	00h
3Dh	00h
3Eh	00h
3Fh	00h
40h	00h
41h	00h
42h	90h
43h	00h
44h	00h
45h	A9h
46h	70h
47h	EEh
48h	D1h
49h	DAh
4Ah	70h
4Bh	EAh
4Ch	4Ah
4Dh	5Eh
4Eh	11h
4Fh	B6h
50h	A2h
51h	2Ah
52h	26h
53h	90h
54h	52h
55h	90h
56h	12h
57h	6Bh
58h	00h
59h	00h
5Ah	**70h**
5Bh	**7Dh**
5Ch	**AFh**
5Dh	**2Dh**
5Eh	**3Fh**
5Fh	**3Fh**
60h	00h
61h	**06h**
62h	**4Bh**
63h	**CBh**
64h	**8Ah**
65h	**09h**
66h	**2Ah**
67h	55h
68h	56h
69h	67h
6Ah	58h
6Bh	20h
6Ch	**28h**
6Dh	**01h**
6Eh	**20h**
6Fh	F1h
70h	80h
71h	E8h
72h	10h
73h	00h
74h	FFh
75h	30h
76h	0Fh
77h	10h
78h	0Fh
79h	10h
7Ah	**18h**
7Bh	**38h**
7Ch	40h
7Dh	00h

SAA7111:
- init data

Slave:	48h
Sub	Data
02h	D0h
03h	00h
04h	00h
05h	00h
06h	F9h
07h	E9h
08h	A8h
09h	00h
0Ah	80h
0Bh	47h
0Ch	40h
0Dh	00h
0Eh	00h
0Fh	00h
10h	50h
11h	0Ch
12h	01h

note: for operating the SAA7111 with the SAA7124/25 the output has to be set to 8-bit CCIR656 format (register 10h: D0h)

INIT_I2C.wmf
V1.4 05.06.96

The settings of SAA7188A are equal to the SAA7184/85B except register 6Eh (value for H-trigger) which should be 29h for PAL and 2Ah for NTSC.

11. Programming tables for SAA7110(A), SAA7187 and SAA7124/25

SAA7187:
- init data PAL

Slave:	8Ch
Sub	Data
REG 3a	= d
REG 42	= 6b
REG 43	= 0
REG 44	= 0
REG 45	= 52
REG 46	= 90
REG 47	= 12
REG 48	= 2a
REG 49	= 26
REG 4a	= 90
REG 4b	= 11
REG 4c	= b6
REG 4d	= a2
REG 4e	= ea
REG 4f	= 4a
REG 50	= 5e
REG 51	= d1
REG 52	= da
REG 53	= 70
REG 54	= a9
REG 55	= 70
REG 56	= ee
REG 57	= 90
REG 58	= 0
REG 59	= 0
REG 5a	= 0
REG 5b	= 7d
REG 5c	= af
REG 5d	= 2d
REG 5e	= 3f
REG 5f	= 3f
REG 60	= 38
REG 61	= e
REG 62	= 4b
REG 63	= c
REG 64	= 8c
REG 65	= 79
REG 66	= 26
REG 67	= 55
REG 68	= 56
REG 69	= 67
REG 6a	= 58
REG 6b	= 91
REG 6c	= 20
REG 6d	= 07
REG 6e	= 84
REG 6f	= 0
REG 70	= 80
REG 71	= e8
REG 72	= 88
REG 73	= 60
REG 77	= 0
REG 78	= 40
REG 79	= 0
REG 7a	= 70
REG 7b	= 18
REG 7c	= 34
REG 7d	= 22

D2_OCFP.187

SAA7187:
- init data NTSC

Slave:	8Ch
Sub	Data
REG 3a	= d
REG 42	= 6b
REG 43	= 0
REG 44	= 0
REG 45	= 52
REG 46	= 90
REG 47	= 12
REG 48	= 2a
REG 49	= 26
REG 4a	= 90
REG 4b	= 11
REG 4c	= b6
REG 4d	= a2
REG 4e	= ea
REG 4f	= 4a
REG 50	= 5e
REG 51	= d1
REG 52	= da
REG 53	= 70
REG 54	= a9
REG 55	= 70
REG 56	= ee
REG 57	= 90
REG 58	= 0
REG 59	= 0
REG 5a	= 0
REG 5b	= 76
REG 5c	= a5
REG 5d	= 3c
REG 5e	= 3a
REG 5f	= 3a
REG 60	= 38
REG 61	= 19
REG 62	= 66
REG 63	= 55
REG 64	= 55
REG 65	= 55
REG 66	= 25
REG 67	= 55
REG 68	= 56
REG 69	= 67
REG 6a	= 58
REG 6b	= 91
REG 6c	= 20
REG 6d	= 07
REG 6e	= 2a
REG 6f	= 0
REG 70	= 80
REG 71	= e8
REG 72	= 88
REG 73	= 60
REG 77	= 0
REG 78	= 40
REG 79	= 0
REG 7a	= c
REG 7b	= 12
REG 7c	= 2
REG 7d	= 22

D2_OCFN.187

SAA7110(A):
- init data

Slave:	9Ch
Sub	Data
REG 0	= 4c
REG 1	= 3c
REG 2	= d
REG 3	= ef
REG 4	= bd
REG 5	= e2
REG 6	= 2
REG 7	= 0
REG 8	= f8
REG 9	= f8
REG a	= 60
REG b	= 60
REG c	= 0
REG d	= 6
REG e	= 18
REG f	= 90
REG 10	= 0
REG 11	= 59
REG 12	= 40
REG 13	= 40
REG 14	= 42
REG 15	= 1a
REG 16	= ff
REG 17	= da
REG 18	= ef
REG 19	= 80
REG 20	= b8
REG 21	= 5
REG 22	= 91
REG 23	= 41
REG 24	= 80
REG 25	= 41
REG 26	= 80
REG 27	= 4f
REG 28	= fe
REG 29	= 1
REG 2a	= cf
REG 2b	= f
REG 2c	= 3
REG 2d	= 1
REG 2e	= 9a
REG 2f	= 3
REG 30	= 60
REG 31	= 75
REG 32	= 2
REG 33	= 8c
REG 34	= 3

D2_OCFN.110

INITcI2C.wmf
7110/7187 11.10.95

The tables show the programming for the One Chip Frontend (SAA7110(A)) and the DENC2-SQ (SAA7187).

E.g. the DTV7183 board can be stuffed with these ICs. The I²C-bus initialization has to be done with an external controller (e.g. PC with register debugger software).

The data tables below show the programming for the SAA7124/25 for operation with SAA7111 (e.g. DECMOD01 connected to ENCMOD02)

SAA7124/25:
- init data PAL

Slave:	88h
Sub	Data
REG 3a	= 13
REG 5a	= 77
REG 5b	= 7d
REG 5c	= af
REG 5d	= 3c
REG 5e	= 3f
REG 5f	= 3f
REG 60	= 70
REG 61	= 6
REG 62	= 4b
REG 63	= ad
REG 64	= 8a
REG 65	= 9
REG 66	= 2a
REG 67	= 55
REG 68	= 56
REG 69	= 67
REG 6a	= 58
REG 6b	= 36
REG 6c	= 1
REG 6d	= 30
REG 6e	= a0
REG 6f	= d1
REG 70	= 80
REG 71	= e8
REG 72	= 10
REG 7a	= 2e
REG 7b	= fb
REG 7c	= 0
REG 7d	= 0

PAL00.124

SAA7124/25:
- init data NTSC

Slave:	88h
Sub	Data
REG 3a	= 13
REG 5a	= 77
REG 5b	= 76
REG 5c	= a5
REG 5d	= 3c
REG 5e	= 3f
REG 5f	= 3a
REG 60	= 70
REG 61	= 5
REG 62	= 6a
REG 63	= 1f
REG 64	= 7c
REG 65	= f0
REG 66	= 21
REG 67	= 55
REG 68	= 56
REG 69	= 67
REG 6a	= 58
REG 6b	= b6
REG 6c	= 11
REG 6d	= 31
REG 6e	= a0
REG 6f	= d1
REG 70	= 80
REG 71	= e8
REG 72	= 10
REG 7a	= 2e
REG 7b	= fb
REG 7c	= 0
REG 7d	= e0

NTSC00.124

INITdI2C.wmf
7124 12.04.96

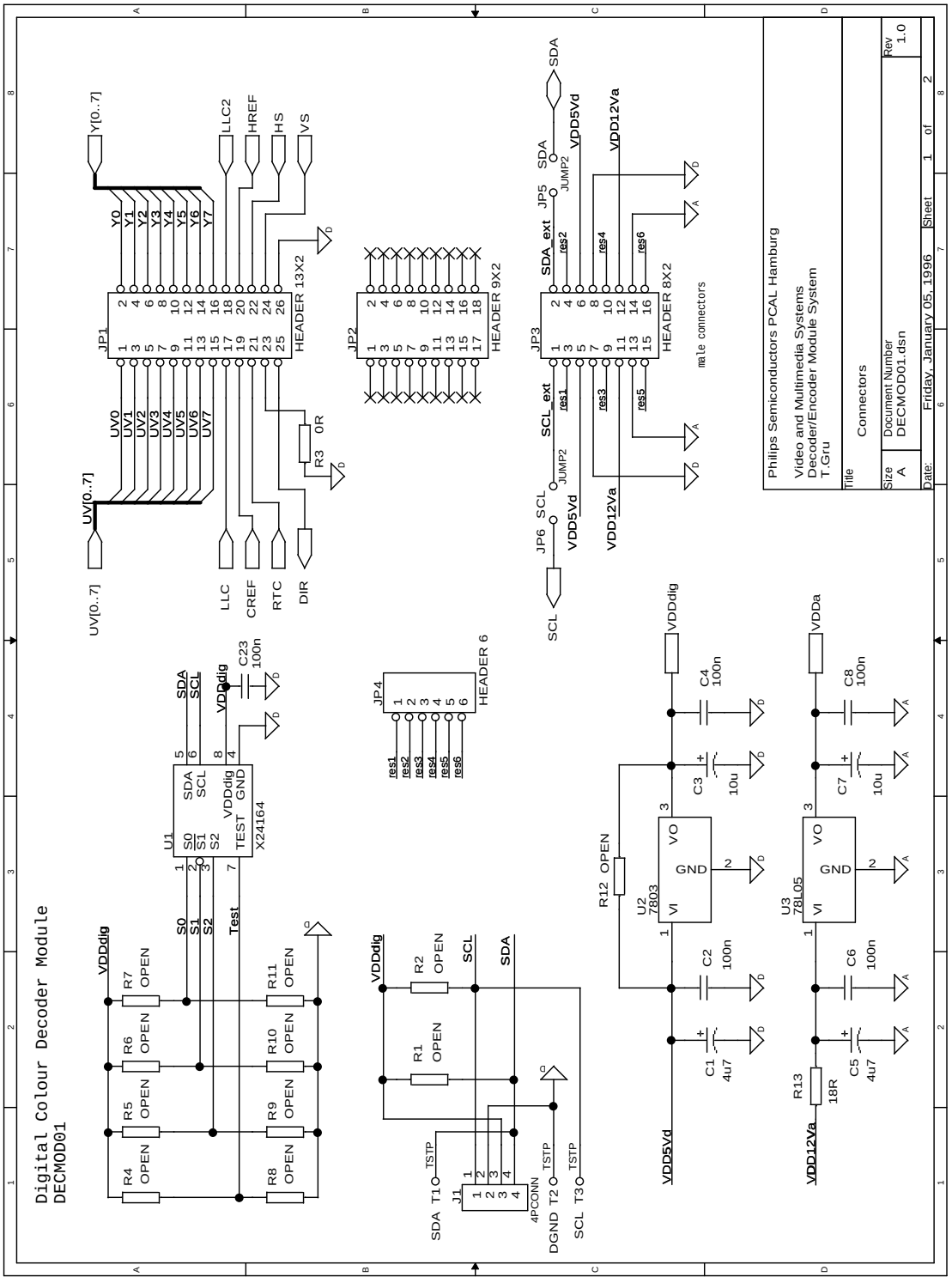
12. Appendix: Schematics and Layout

The schematics are made in OrCAD and the files can be delivered on request.

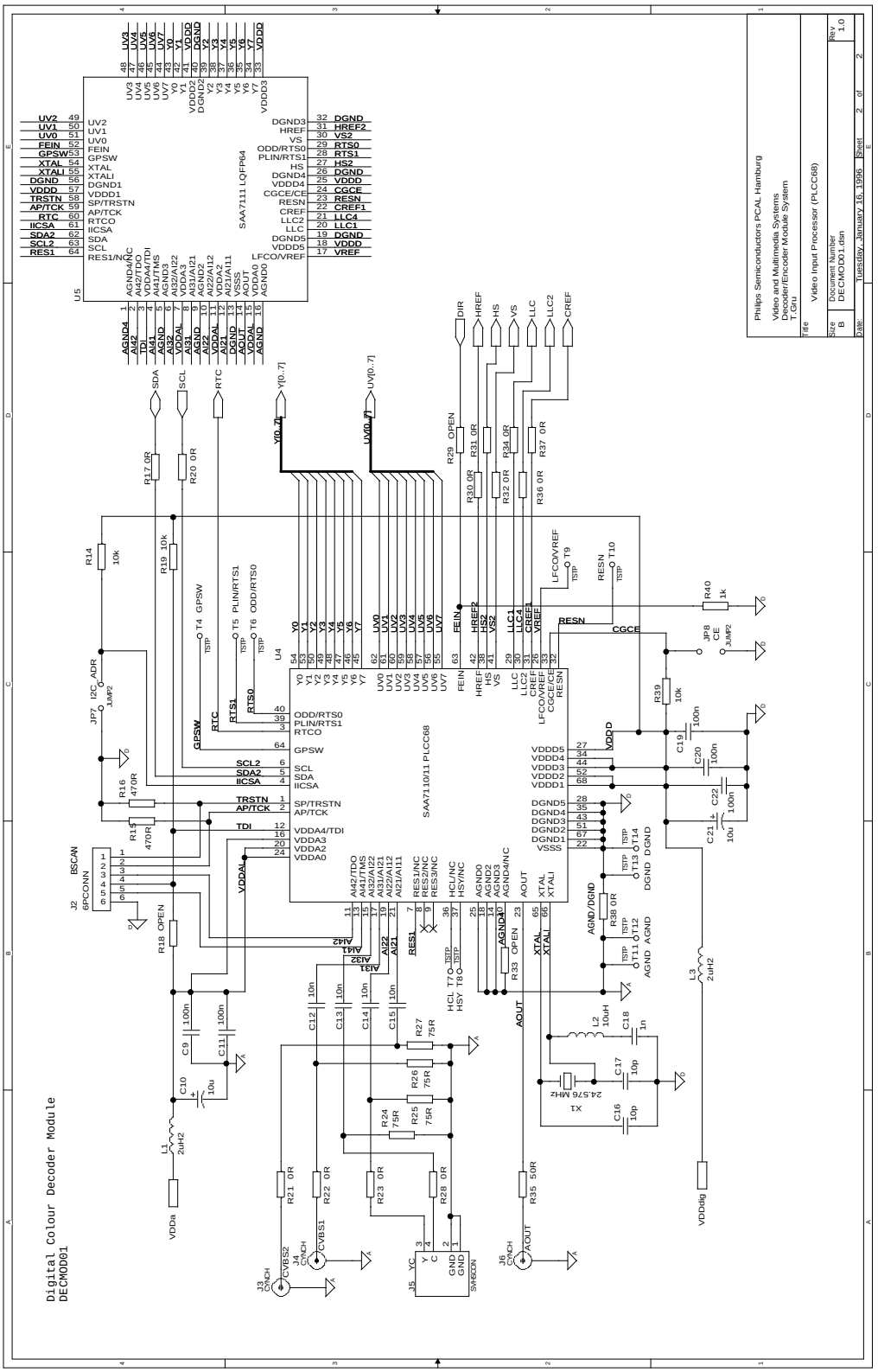
For the board layout GERBER files are available.

12.1 Schematics

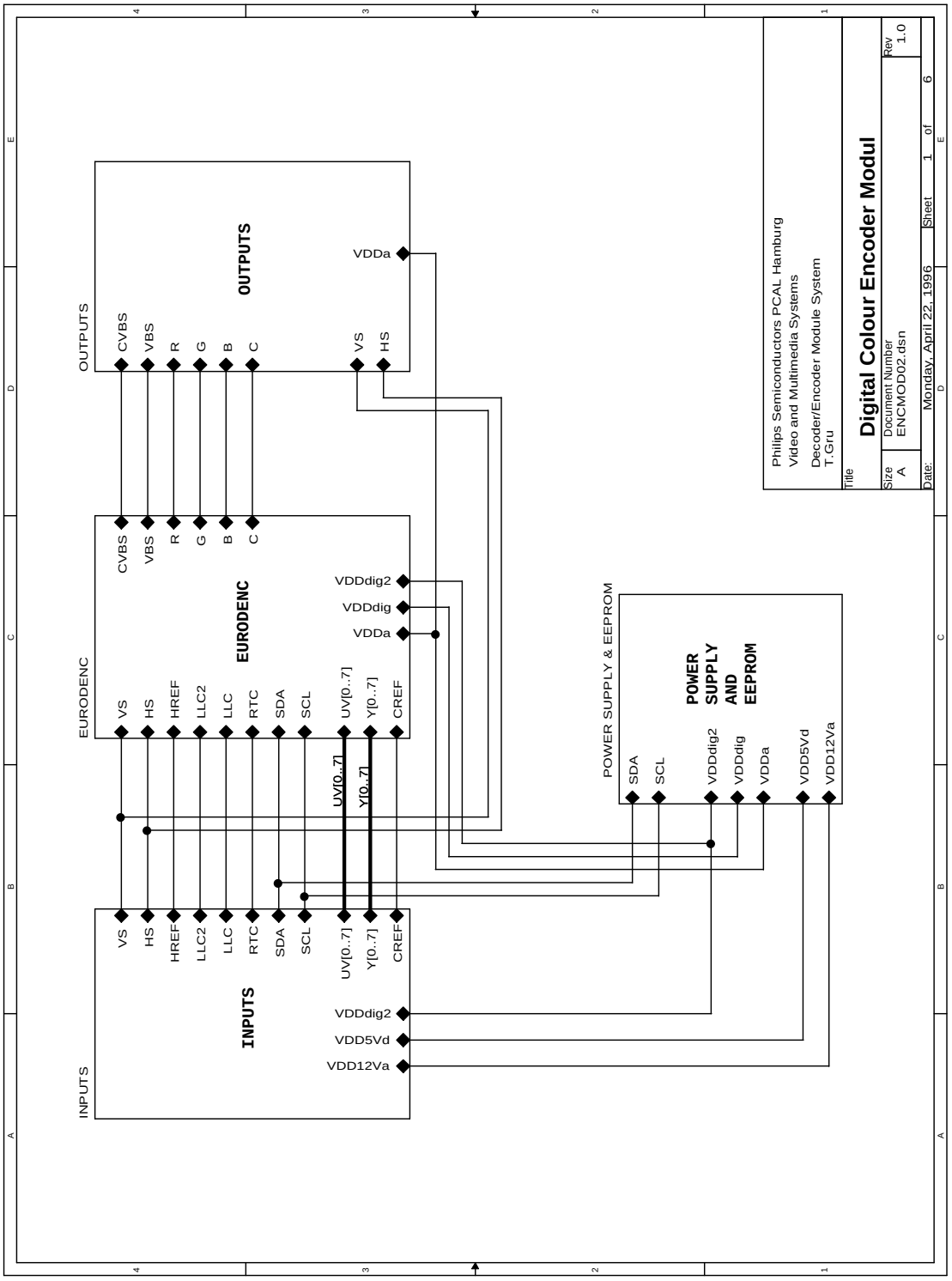
12.1.1 Power Supply, EEPROM and Connectors of DECMOD01



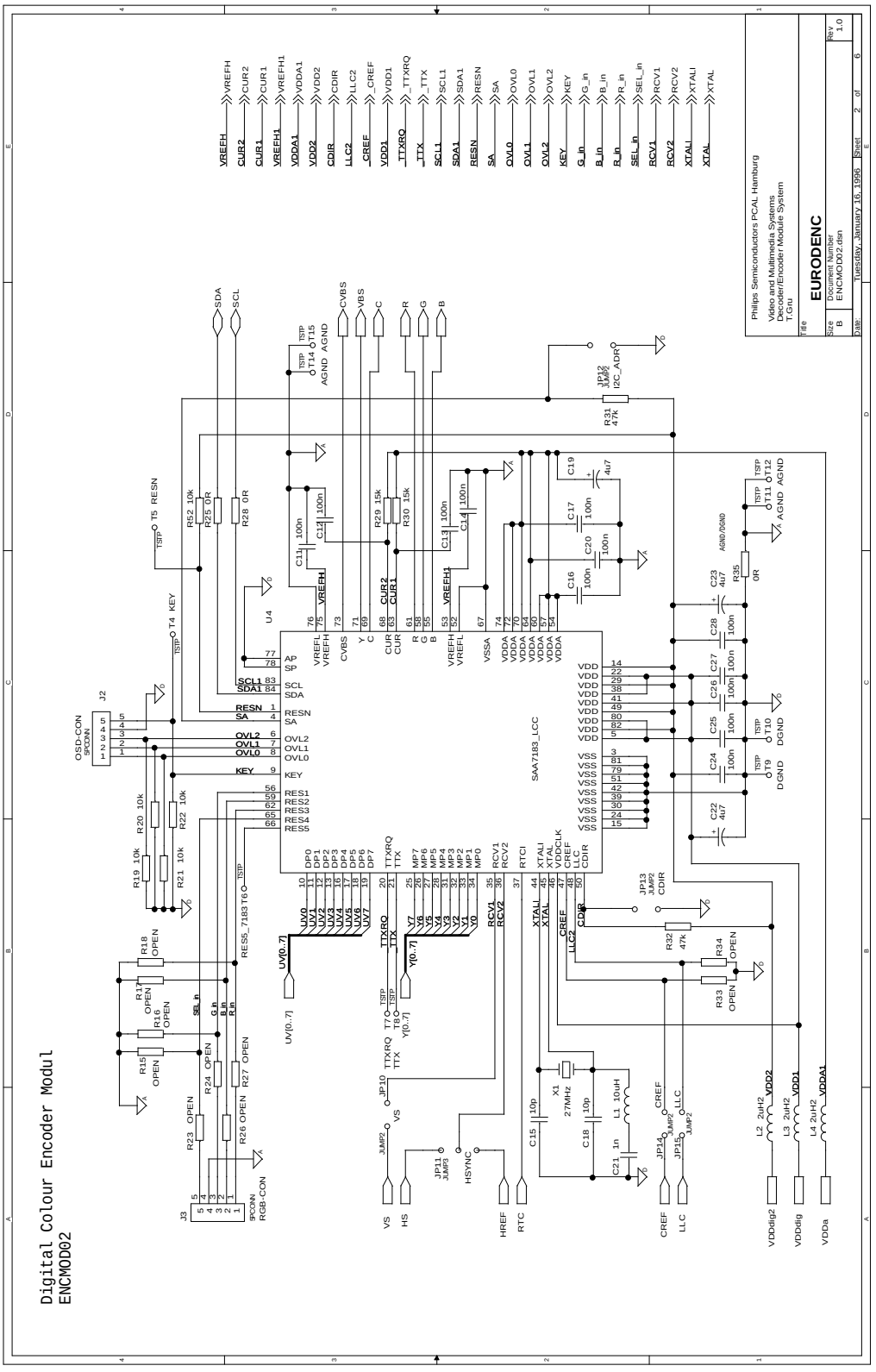
12.1.2 Digital Video Decoder of DECMOD01



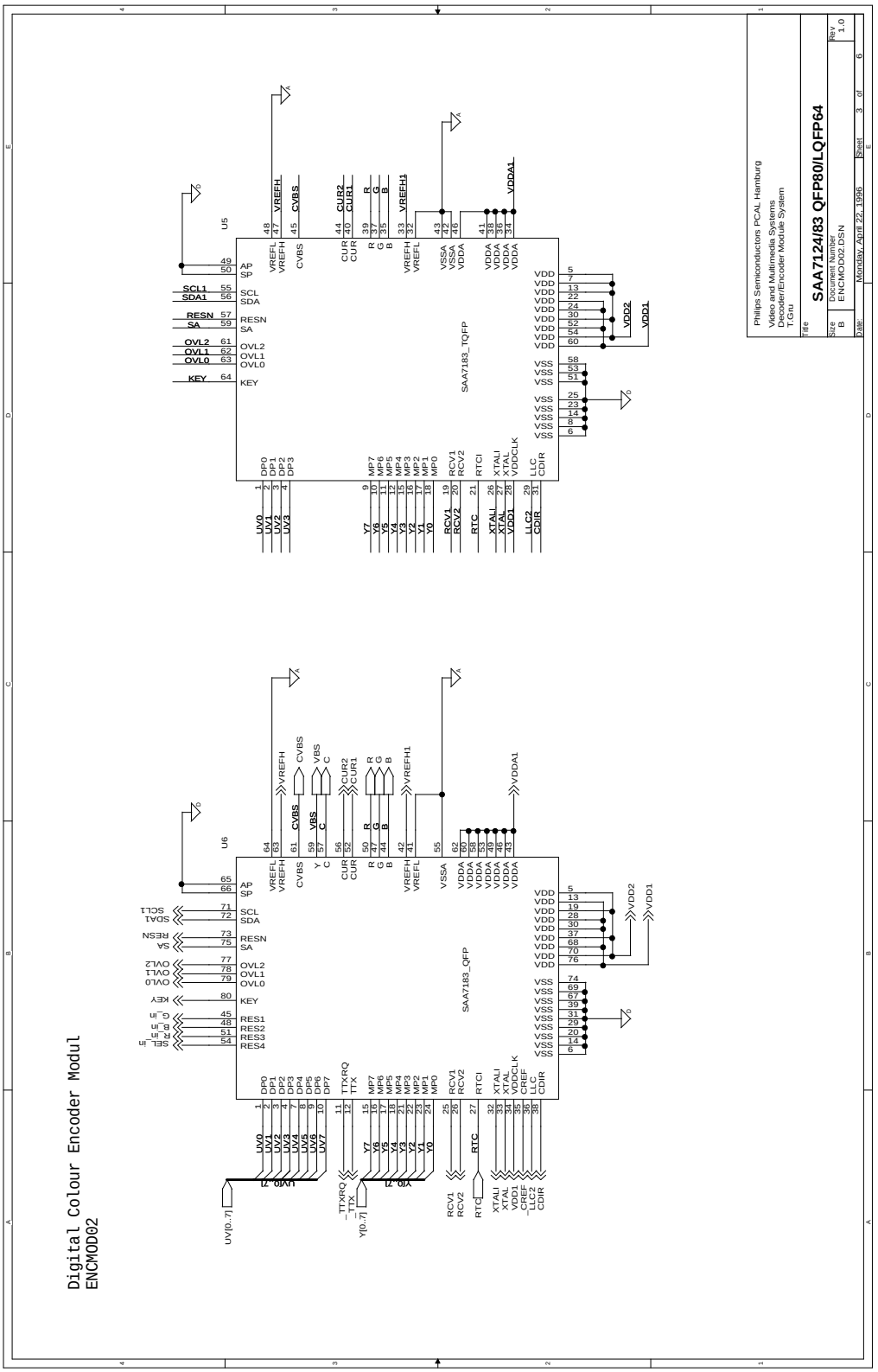
12.1.3 Top sheet of ENCMOD02



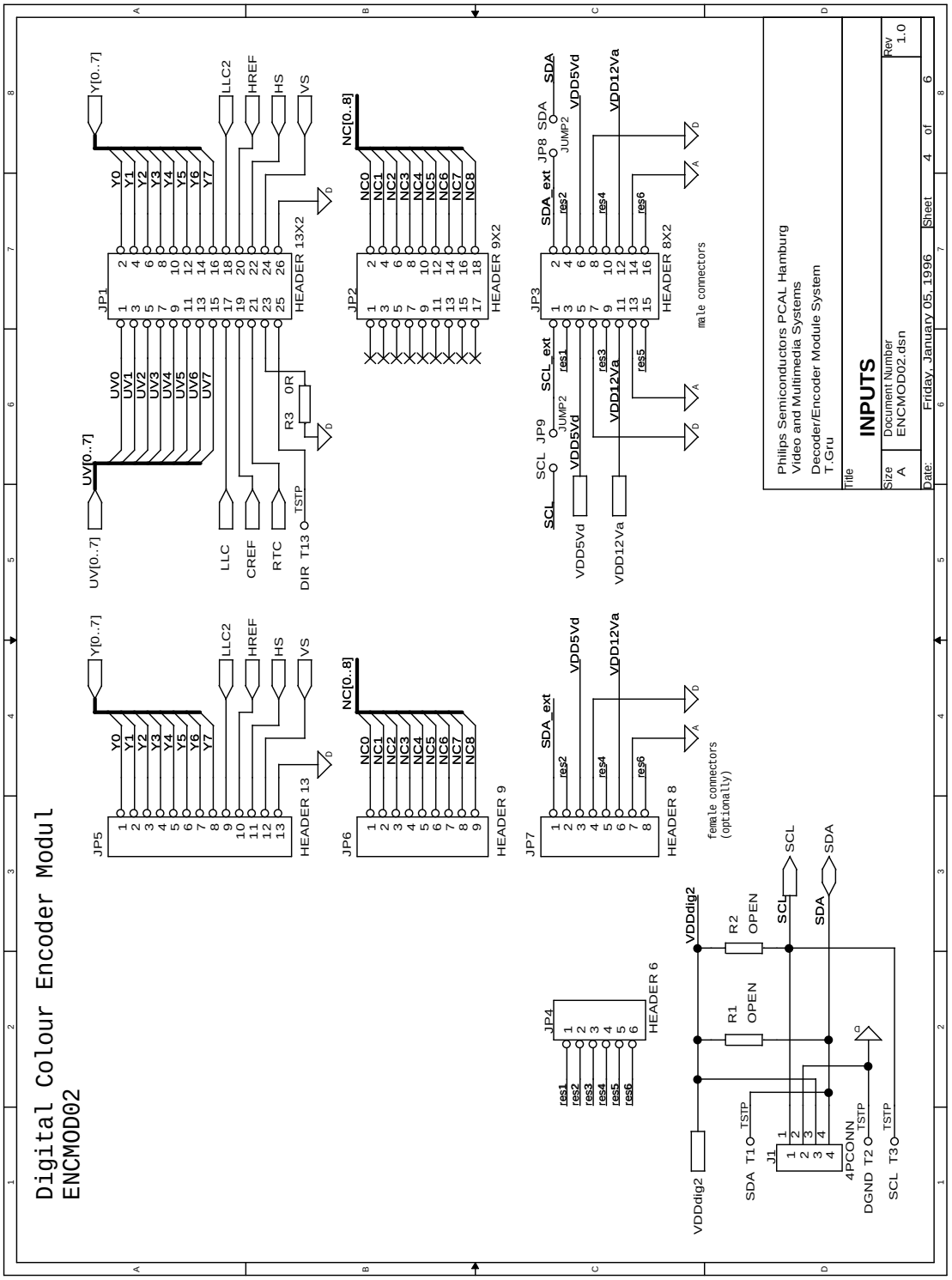
12.1.4 Digital Video Encoder of ENCMOD02



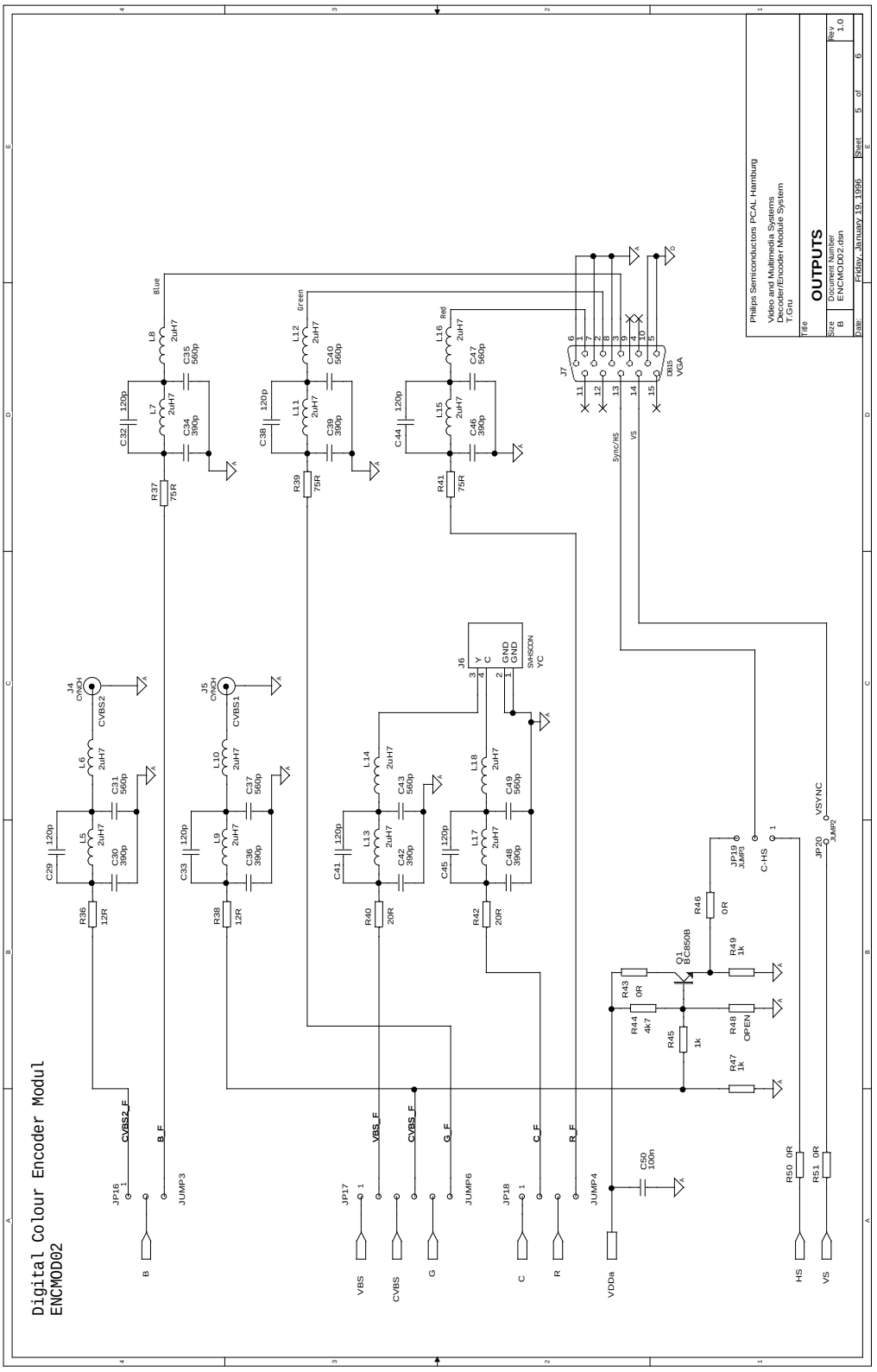
12.1.5 Additional IC packages for ENCMOD02



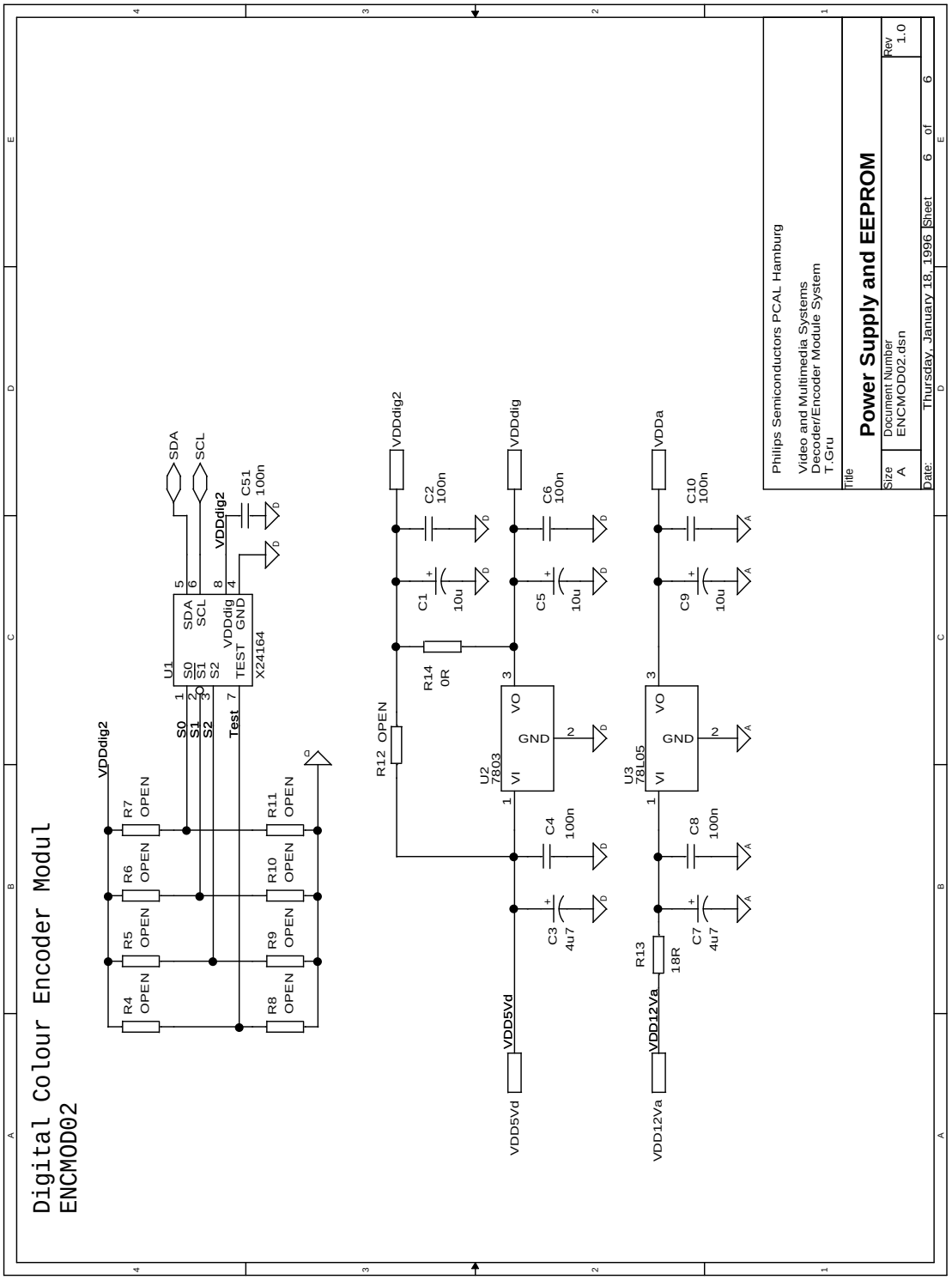
12.1.6 Inputs of ENCMOD02



12.1.7 Outputs of ENCMOD02

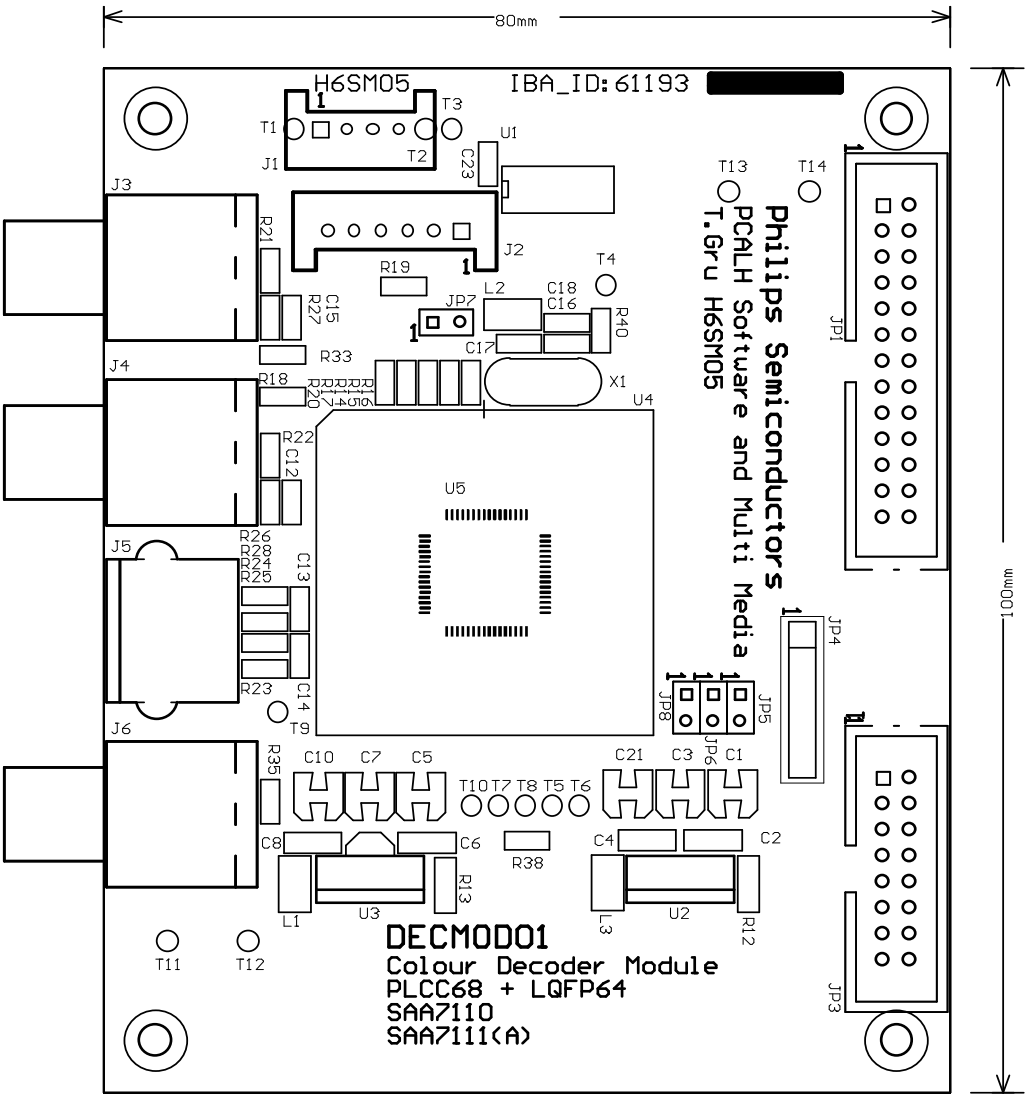


12.1.8 Power Supply and EEPROM of ENCMOD02

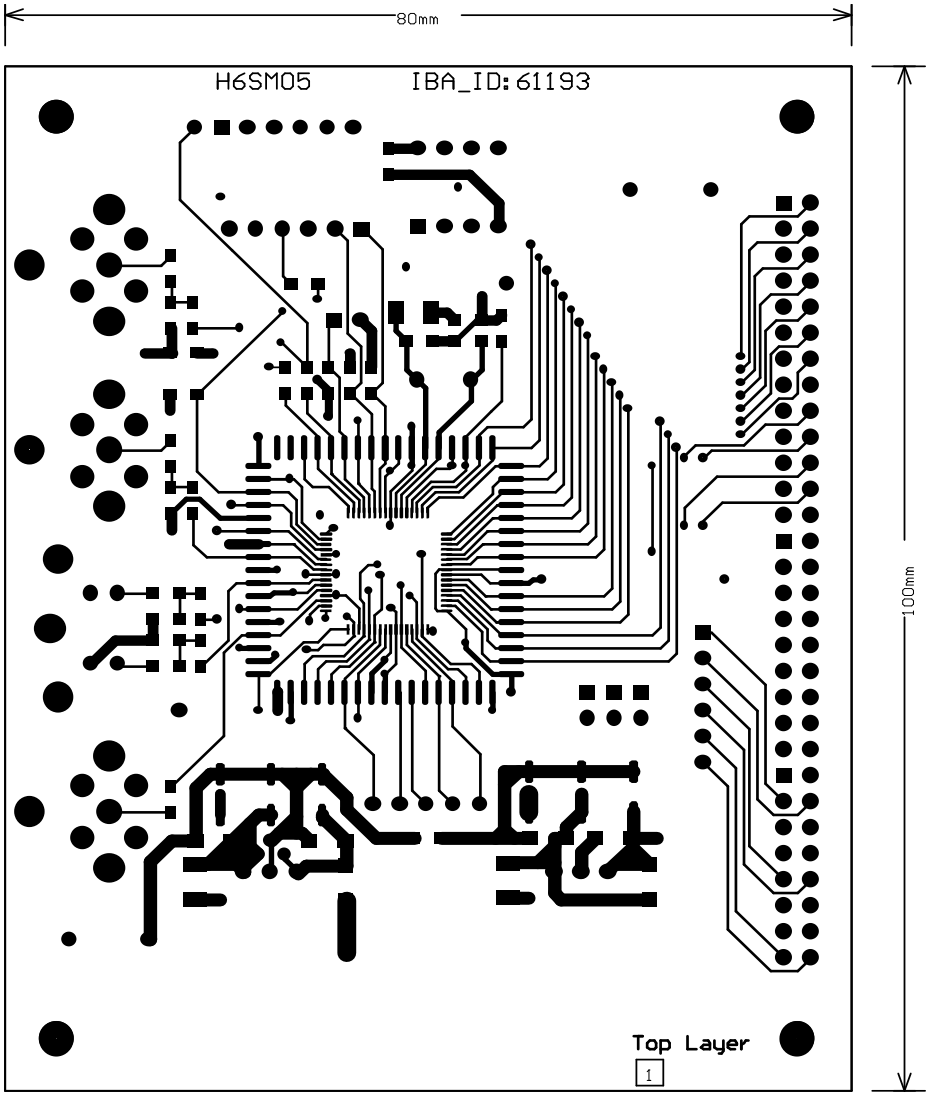


12.2 Layout

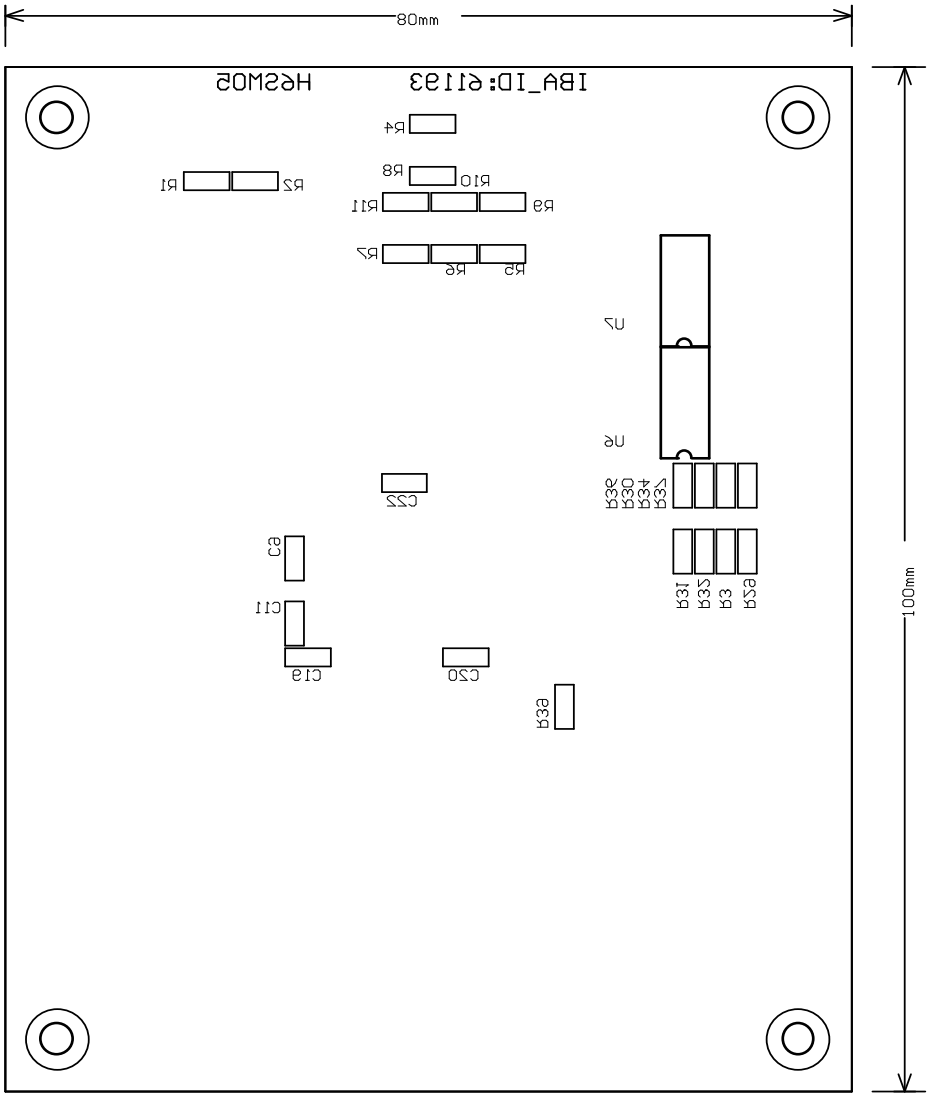
12.2.1 Top placement of DECMOD01



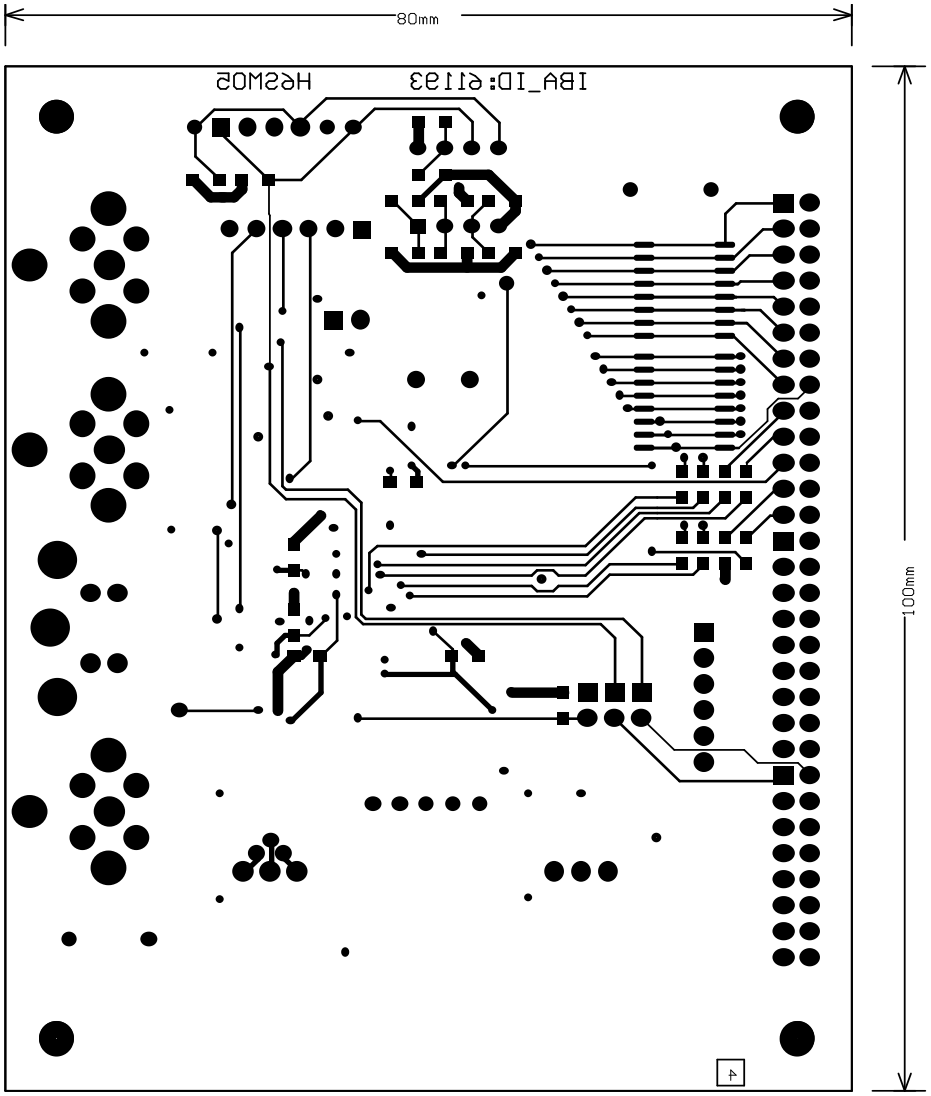
12.2.2 Routing of top layer of DECMOD01



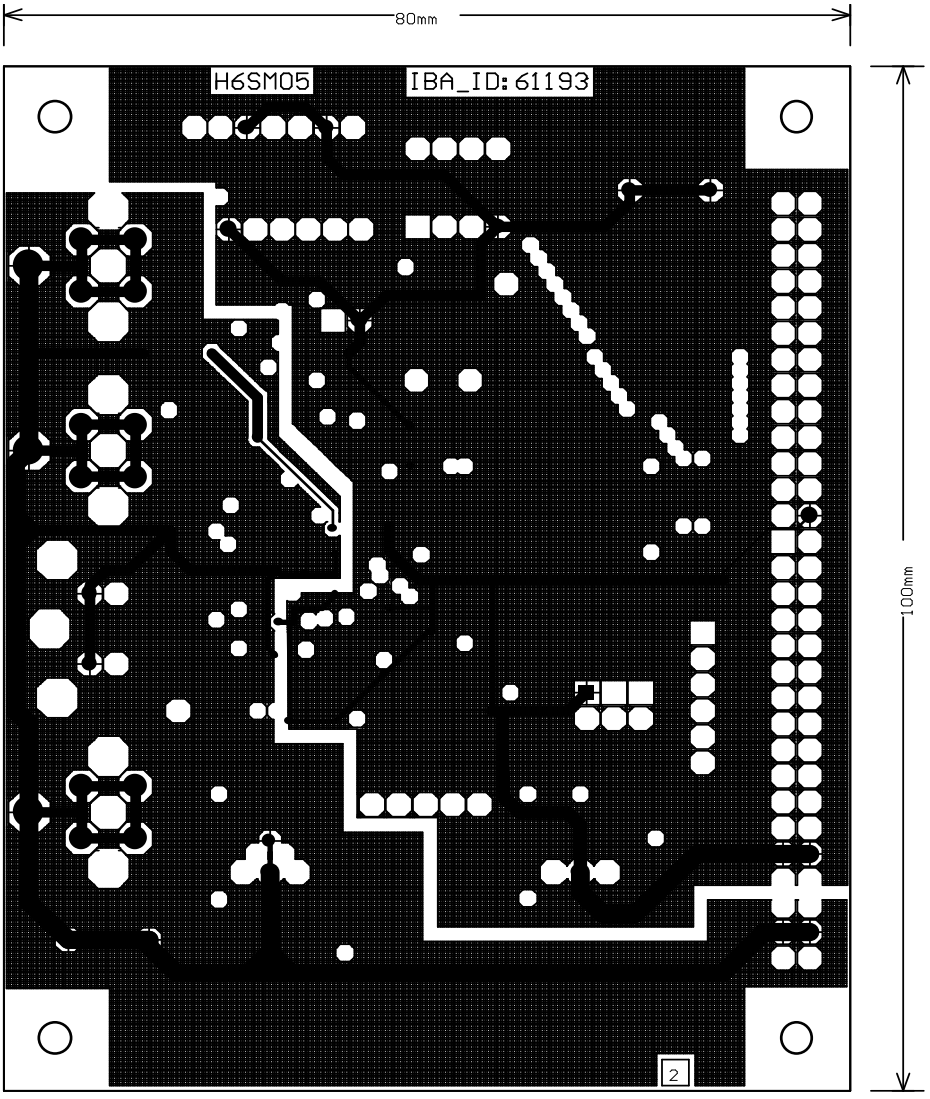
12.2.3 Bottom placement of DECMOD01



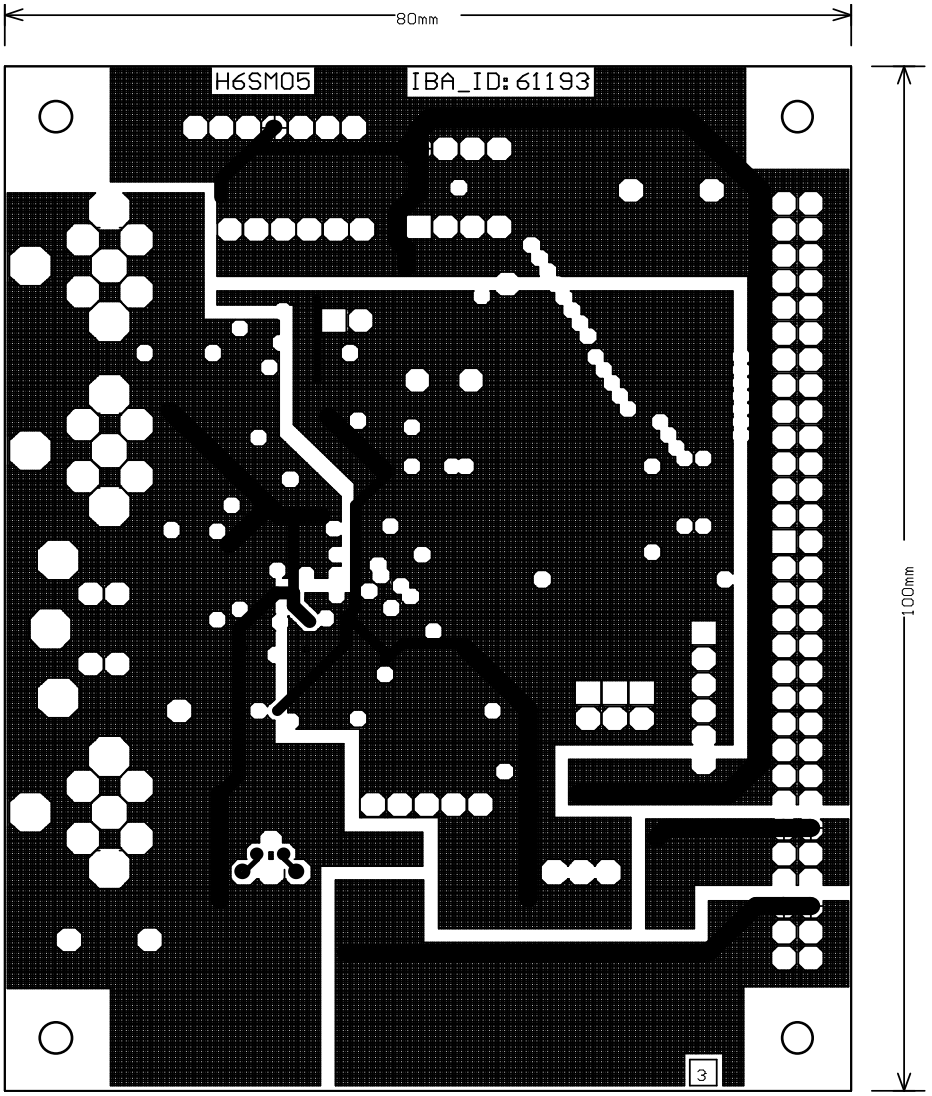
12.2.4 Routing of bottom layer of DECMOD01



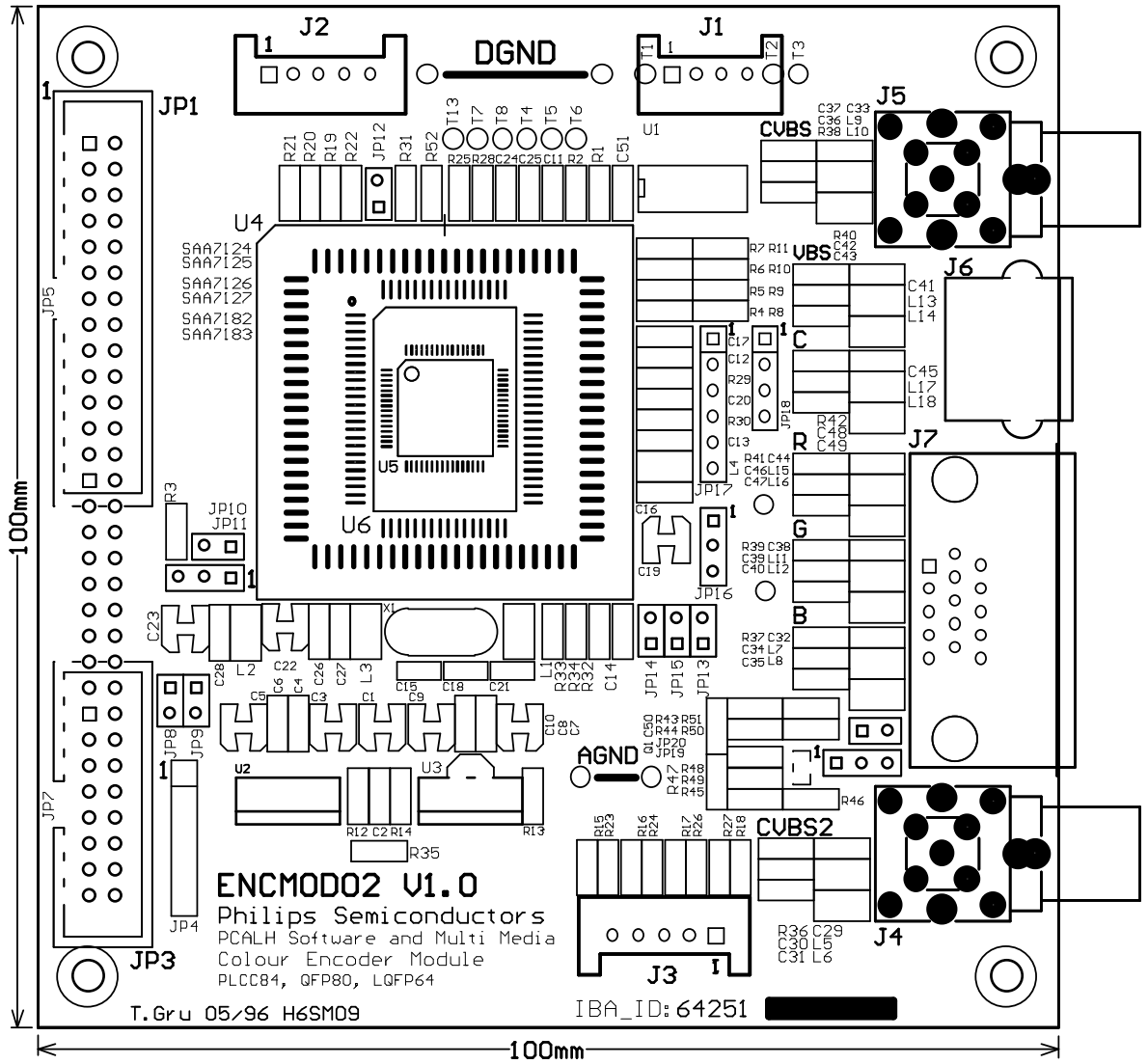
12.2.5 Routing of ground plane layer of DECMOD01



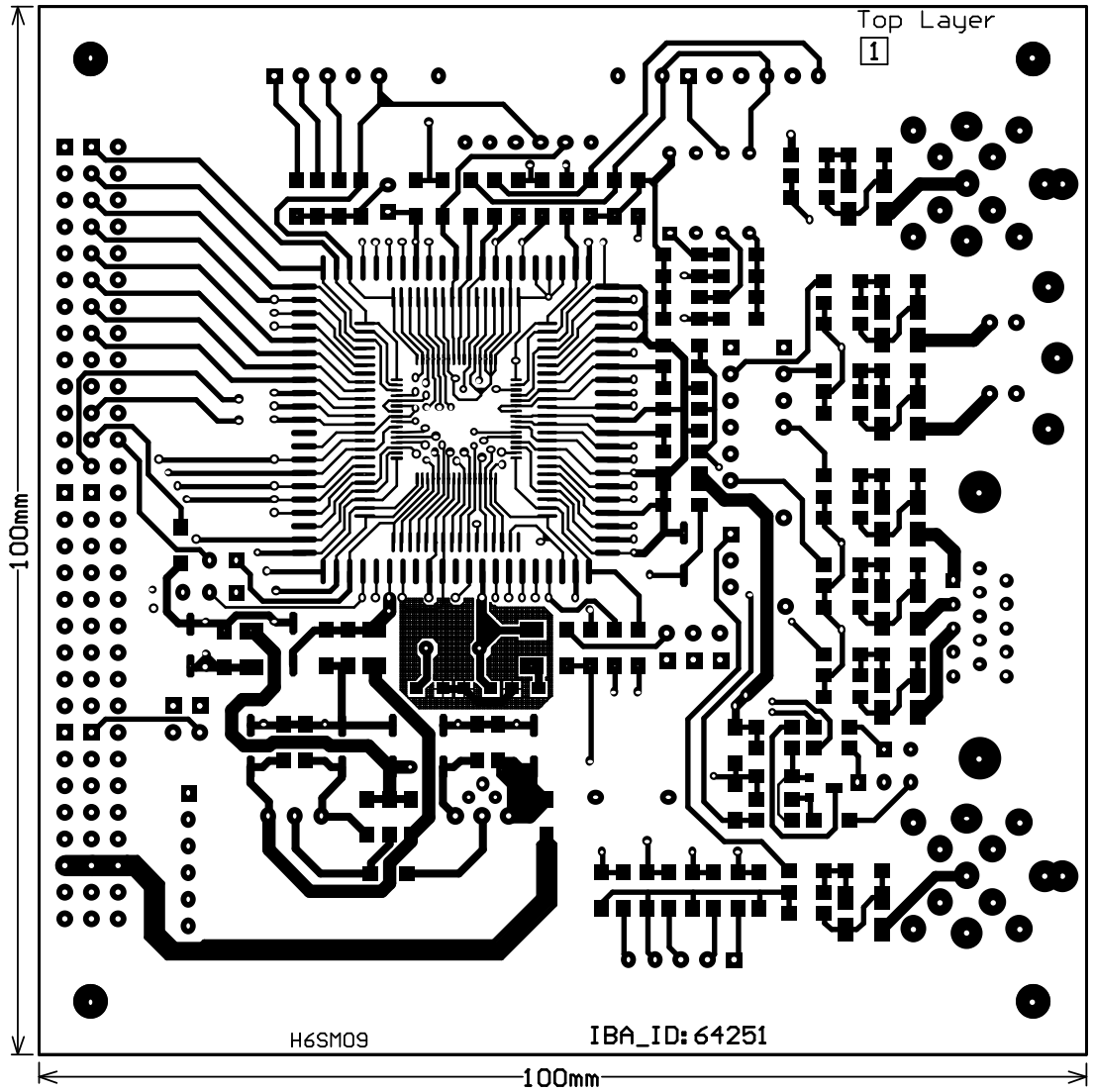
12.2.6 Routing of power supply layer of DECMOD01



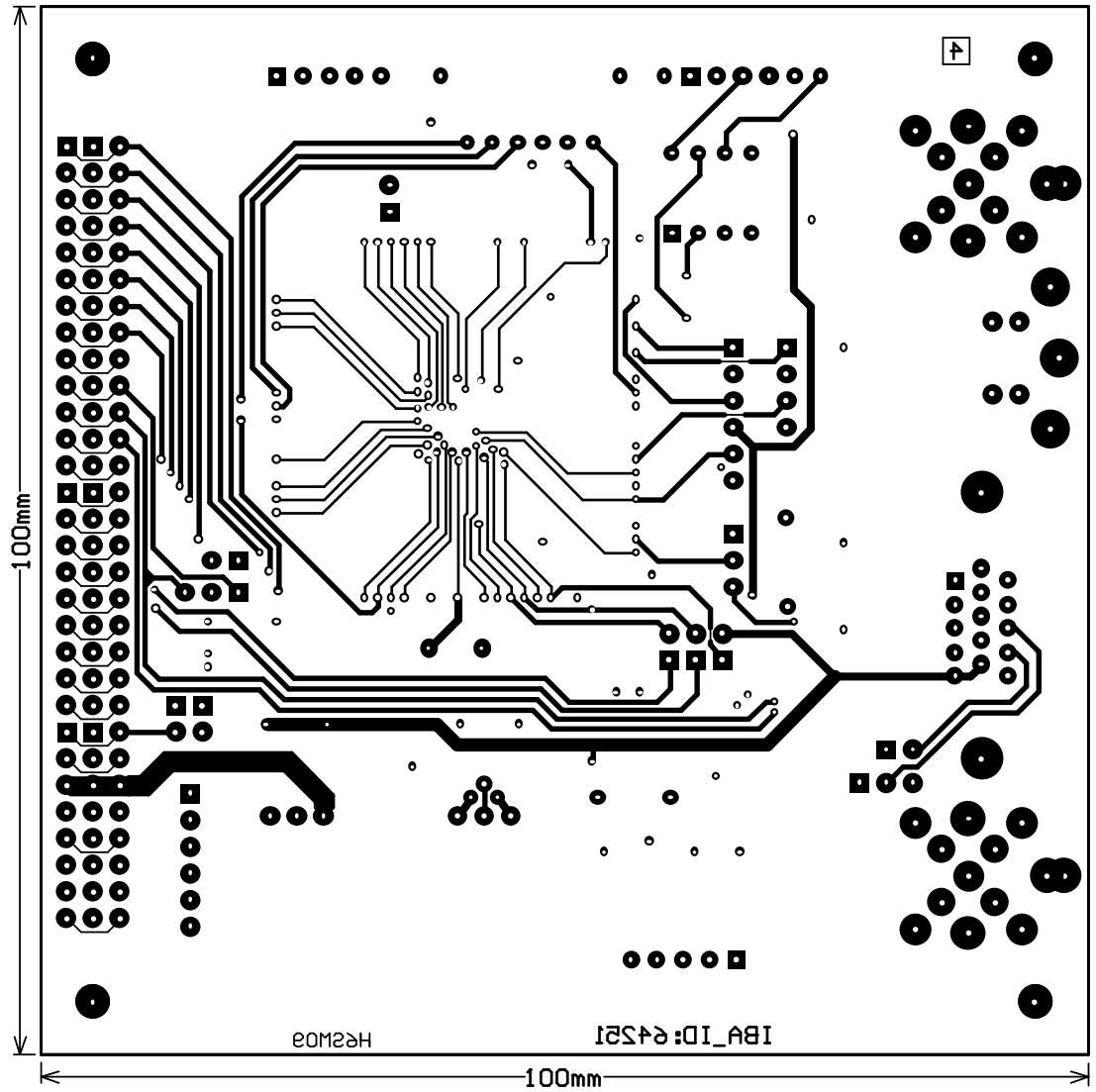
12.2.7 Top placement of ENCMOD02



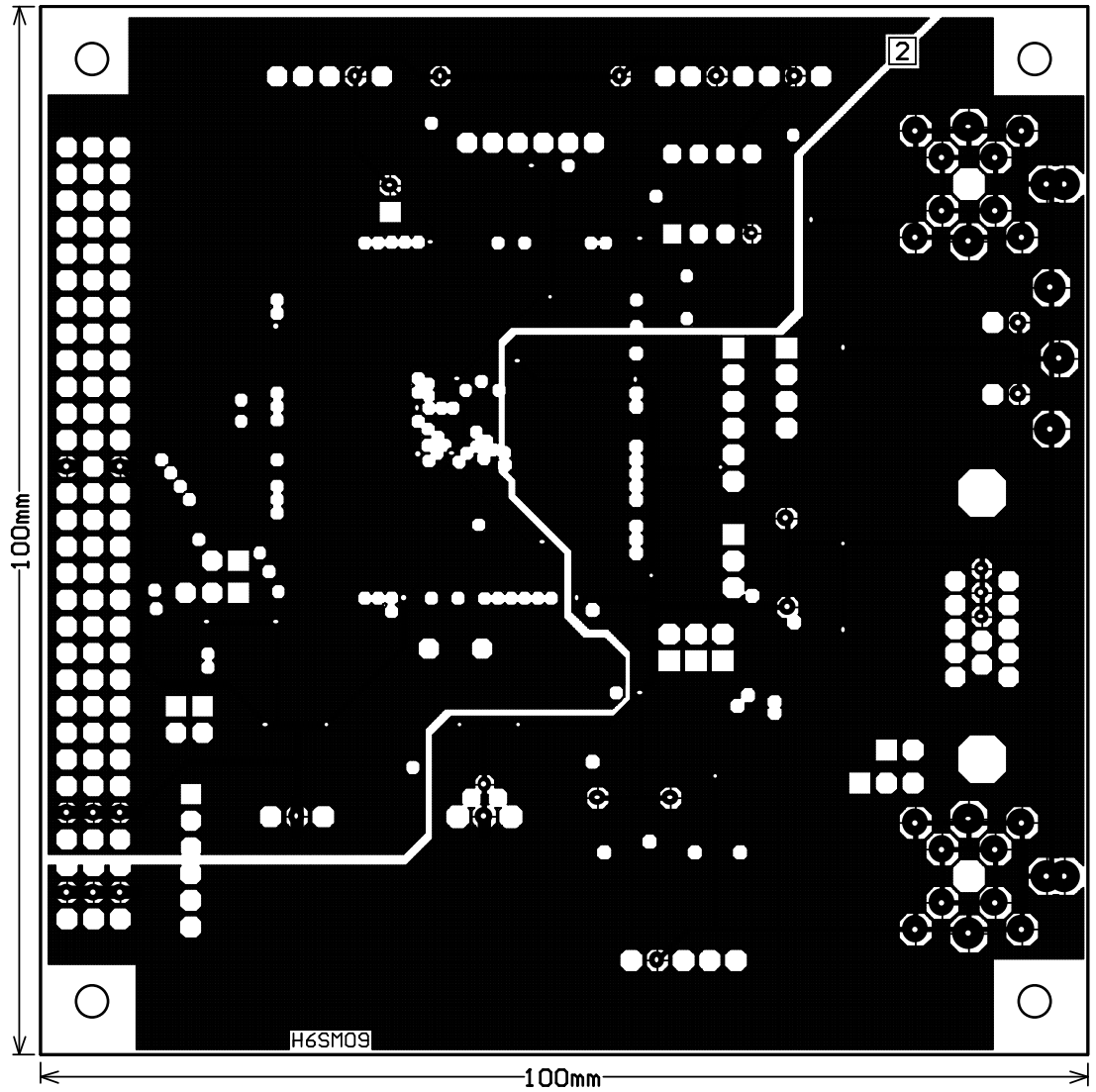
12.2.8 Routing of top layer of ENCMOD02



12.2.9 Routing of bottom layer of ENCMOD02



12.2.10 Routing of ground plane layer of ENCMOD02



12.2.11 Routing of power supply layer of ENCMOD02