ARMADILLO PRODUCT SPECIFICATIONS

08/24/82

* First started from LCP H/W specs.

8/29/82

* Continued update effort.

09/09/82

* Continued update effort.

09/10/82

* Continued update effort.

10/26/82

* Updated SRAM, ROM, C/M ROM, mapper, and CRU paragraphs.

10/27/82

* Continued update as of yesterday.

10/28/82

* Continued update as of yesterday.

10/29/82

* Continued update as of yesterday.

01/20/83

* Continued general update.

01/24/83

* Continued general update.

02/04/83

* Continued general update. Updated PAS Memory Map, also.

03/21/83

* Continued general update.

05/25/83

* Added Command Port Connector pin outs.

06/29/83

* Added Command Port Capacitance maximum loading.

07/06/83

* Added Command Port power limitations.

SECTION 1

SCOPE

This document describes the functional, environmental, mechanical, quality, and documentation requirements for the TI ARMADILLO Personal Computer.

SECTION 2

APPLICABLE DOCUMENTS

* FCC DOCKET 20780, PART 15, SUBPARTS H AND I
* MIL STD 461A; 462 METHODS CS01, CS02, CS06, RS01, RS02, RS03
* NATIONAL SAFE TRANSIT PRESHIPMENT TEST PROCEDURE
* GRAS 10237
* MIL STD 810B
* UL STD 114
* CSA STD C22.2-154
* TEC 380
* FILE MANAGEMENT SPECIFICATION
* LCP Mechanical Drawing Package DWG #0000000
* 9995 DATA SHEETS
* 9918A DATA SHEETS
* SOUND GENERATOR, SN94624
* Keyboard Specification DWG# 00000xx

SECTION 3

FUNCTIONAL HARDWARE DESCRIPTION

3.1 99/4A SOFTWARE COMPATIBILITY

Hardware shall be included to insure that most 99/4A Software will run on the ARMADILLO. Software excluded shall be that base which directly accesses the internal CRU (Keyboard or Joystick) of the 99/4A.

It shall not be a condition that BASIC programs execute at the same speed on the ARMADILLO as they do on the 99/4A, but games shall closely approximate the 99/4A speed. Software switching shall be included to remove these restrictions when desirable.

3.2 TRANSFORMER LOCATION

The transformer shall be located external from the ARMADILLO, and shall conform to the "RAT-IN-THE-SNAKE" approach.

3.3 POWER SUPPLY LOCATION

The Power Supply shall be located inside of the ARMADILLO. It shall supply both +5V and -5V and no +12V as a goal. Currents shall be established by the Electrical Design Team upon design completion.

3.4 DESIGN RULES

General design guidelines are set forth in the Equipment Group's TTL DESIGNER'S GUIDE.

3.5 DESIGN VERIFICATION

Propagation delays on each of the first QUAL units shall be carefully measured and compared against calculated design values. Any negative deviations shall be explored until completely understood. These shall drive any design changes necessary.

A thermal profile shall be generated to identify and eleminate hot spots.

3.6 TESTABILITY COMMENTS

Signature Analysis shall be designed in to the ARMADILLO as the primary means for both factory and field testing of digital circuits. The PCC shall define other test philosophies as needed for testing of the transformer, power supply, audio, and video.

3.7 TEST PLAN

A test plan shall be written after design and debug so as to include test hooks determined necessary or handy during that time. Piece part test plans shall be included in this effort.

3.8 PARTS SELECTION

Where practical, parts currently existing in the CPG Drawing System shall be used. Any new devices requiring QUAL shall be delivered to QA as quickly as samples are in hand to insure adequate QRA response time.

Parts requiring hand stuffing (those that cannot go through the washer are by definition hand stuffed) shall be held to a minimum.

3.9 RFI DESIGN CONSIDERATIONS

Good Grounding techniques shall be used through out to insure low RFI radiation from this source.

Connectors for the Power Supply, Keyboard, and any external peripheral device shall be grounded and filtered as may be required.

The entire system shall be enclosed in a conductive enclosure to futher reduce RFI if preliminary RFI scans indicate this to be required.

3.10 ROM CHECK BYTES

A two byte CRC shall be included in the last two byte locations of every ROM and GROM in the system. These bytes shall be used in system level diagnostics as well as in the initial device testing; thus, test programs may be made device independant.

3.11 CPU

The CPU shall be a TMS9995 deravitive uP operating at 10.7386 MHz. It shall have no internal RAM, and the CRU Flags (including the Mid Bit Flag) will respond in the new TMS9995 CRU space.

3.12 RAM

An internal 2Kx8 SRAM shall be provided, and shall be connected directly to the Data and Address bus of the CPU.

The SRAM shall respond to one of two locations depending upon the state of the CRU Configuration Bit (CRUS). The Power-Up default base address is >8000, and the alternate base address is >F000. See the CRU Memory Configuration Bit paragraph for more details.

3.13 ROM

A pair of ROMs shall be provided for system use. The first shall be connected directly to the TMS9995 Data and Address buses, and shall be called "ROM0". ROM0 shall be based at LAS >0000 if the CRU Configuration Bit is HIGH, and disabled if that bit is LOW. ROM0 shall operate on a 2 clock cycke per BYTE period, be organized as 8K x 8 array, and be either psuedo or fully static.

The second ROM ("ROM1") shall be located in the PAS, and shall be based at >FFA000. It shall cycle on a 3 clock cycle per

BYTE period as its address shall come from the Mapper.

ROM1 shall be a 32K x 8 organization, and shall be divided into three functional sections. The first is a 16K block based at >FFA000, and the second and third are 8K blocks in the DSR ROM space (>FF4000).

ROM1 may operate as either a psuedo static or fully static ROM.

3.14 COMMAND MODULE ROM CONTROL

The Command Module ROM shall respond at a base of >FF6000.

3.15 MEMORY MAPPER

A Memory Mapper shall be included on the ARMADILLO to map the 16-Bit Logical Address Space (LAS) into a 24-Bit Physical Address Space (PAS).

3.15.1 Organization. The following is a list of Memory Mapper Characteristics.

* The mapper shall be organized around sixteen (16) 27-Bit Base Registers to map the 16 9995 4K BYTE segments into the PAS. The 16 Base Registers shall be selected by the four (4) Most Significant Bits of the 9995 Address Bus.

* The CRU Address shall be passed unmodified by the Mapper.

* The Memory Mapper logic shall provide a three (3) Clock cycle per Byte time, and shall hide the first from the outside world (PAS) by suppressing MEMEN* for the first of the three Clock cycles.

* MEMEN* shall be suppressed from the PAS for all LAS mapped devices. Where practical, the devices in the LAS shall access in two (2) Clock cycles.

* The 16 Base Register array shall be auto loaded from one of eight 64 Byte blocks based at the zero end in the internal SRAM (regardless of where that RAM is based). If the CRU Configuration Bit is HIGH, a MOVB to LAS >8810 shall initiate the transfer. If that bit is LOW,

the mapper will respond at >F870. The Power-Up bit condition shall be HIGH.

* The MSB (Bit 00) of the MSBY of a Mapper Register shall serve as a WRITE Protect Bit. A violation of this feature shall provide an Interrupt, and no WRITE shall occur.

* Bit 01 in a Mapper Register shall provide an Execute Protect. Execution of code in an Execute Protected LAS 4K block shall produce an Interrupt, and the execution shall be allowed to take place if not pipelined in the TMS9995.

* Bit 02 in a Mapper Register shall provide READ protection. If a violation of this protect occurs, an Interrupt shall be generated. The READ operation shall be allowed to normally occur.

* A Mapper generated interrupt shall be cleared by a Status READ of the Mapper response location. The BYTE read shall have the status of the three violation bits formatted just as the protect bit locations were in the Mapper RAM.

* The Byte storred in the LAS >8810 (CRUS=1) or LAS>F870 (CRUS=0) shall determine the operation as is shown in the table in the following text.

* The mapper shall modify the TMS9995 DBIN* and WE* timing to conform to that of the TMS9900 to facilitate interfacing to 99/4 peripherals.

Byte Value	Function
0000 xxx0	Save Base Reg File in SRAM
0000 xxx1	Load Base Reg File from SRAM

xxx is the number of 64 BYTE areas from the base of the SRAM (>40 increments).

3.15.2 MAPPER Definition in SRAM. The MAPPER area in the internal 2K Byte SRAM shall be as follows.

>8000 64 BYTE, 0 base >803F
>8040 64 BYTE, 1 base Area >807F
>8080 64 BYTE, 2 base Area >80BF
>80C0 64 BYTE, 3 base Area >80FF
>8100 64 BYTE, 4 base Area >813F
>8140 64 BYTE, 5 base Area >817F
>8180 64 BYTE, 6 base Area >81BF
>81C0 64 BYTE, 7 base Area >81FF

3.15.3 Mapper Area Format. The Mapper area in SRAM shall be formatted as follows for the base area. The successive areas

shall be formatted identically, but it shall be displaced some integral number of >40 into the SRAM.

Address	Function
>000	MSBY, REG 0
>001	NMSBY, REG 0
>002	NLSBY, REG 0
>003	LSBY, REG 0
>004	MSBY, REG 1
>005	NMSBY, REG 1
>006	NLSBY, REG 1
>007	LLSBY, RG 1
....	....
>03C	MSBY, REG 15
>03D	NMSBY, REG 15
>03E	NLSBY, REG 15
>03F	LSBY, REG 15

3.15.4 Protect bit Format. The format for the Protect bits shall be as follows in the MSBY of the Mapper register. A HIGH Level shall be used to enable the protect feature.

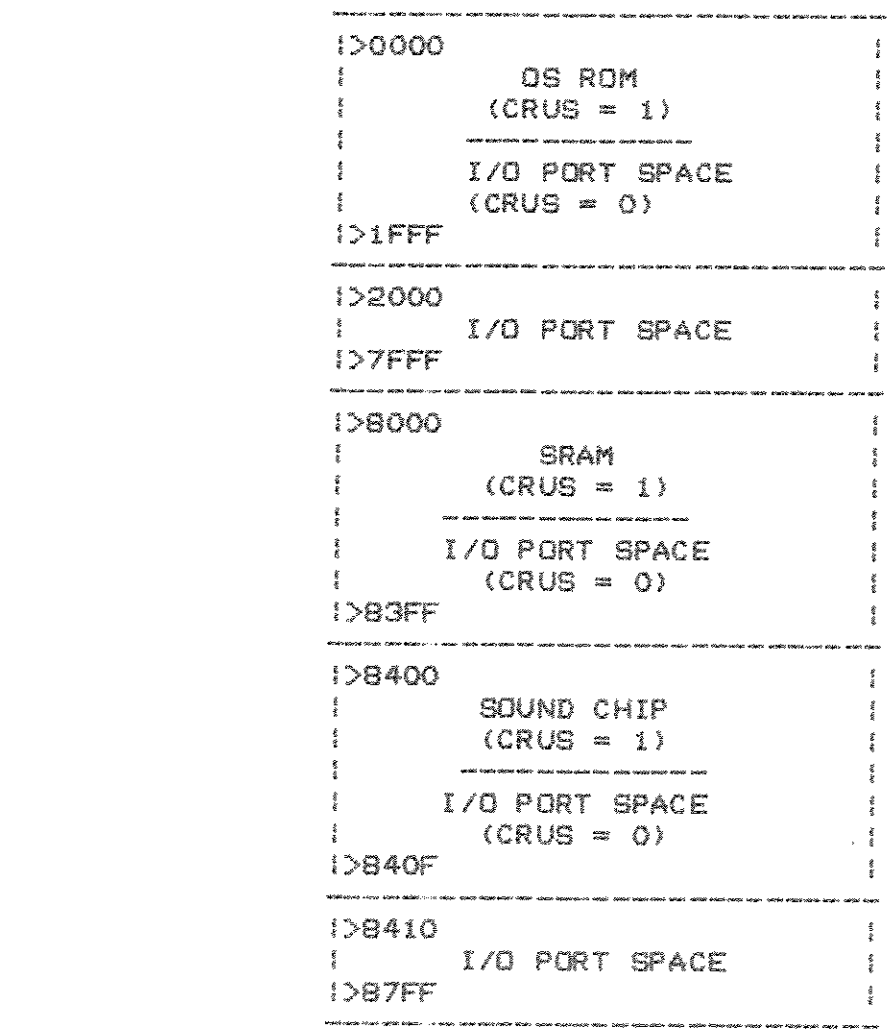
WXR0 0000

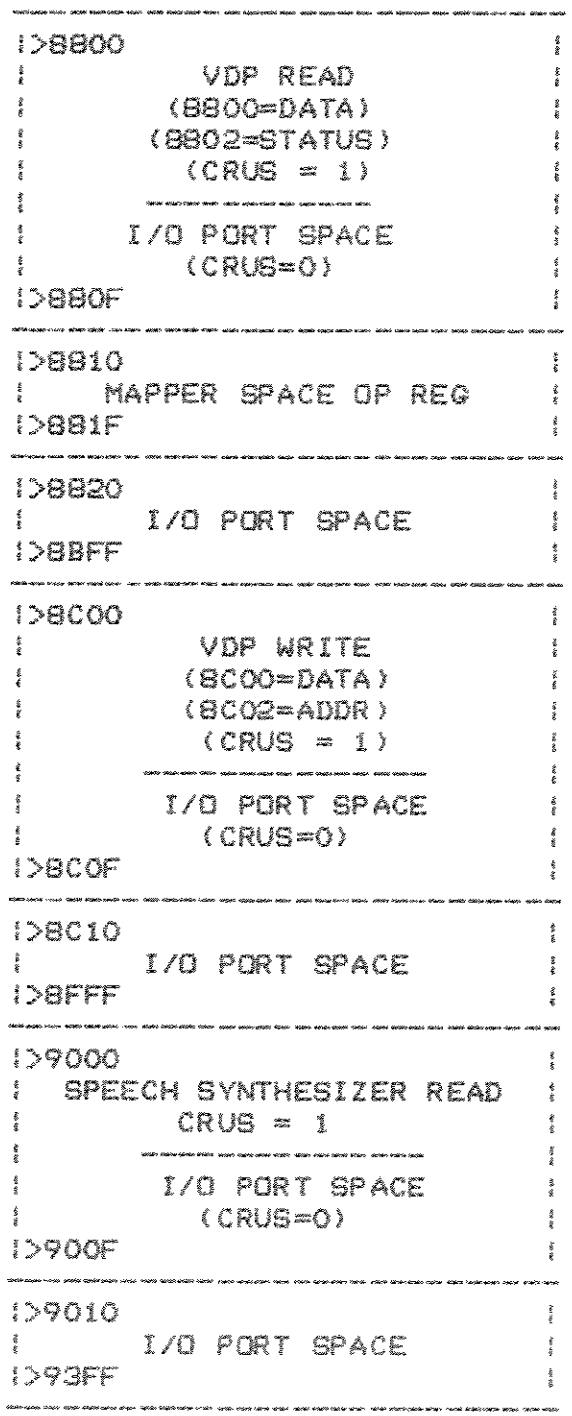
where W = WRITE Protected, X = Execute Protected,
and R = READ Protected.

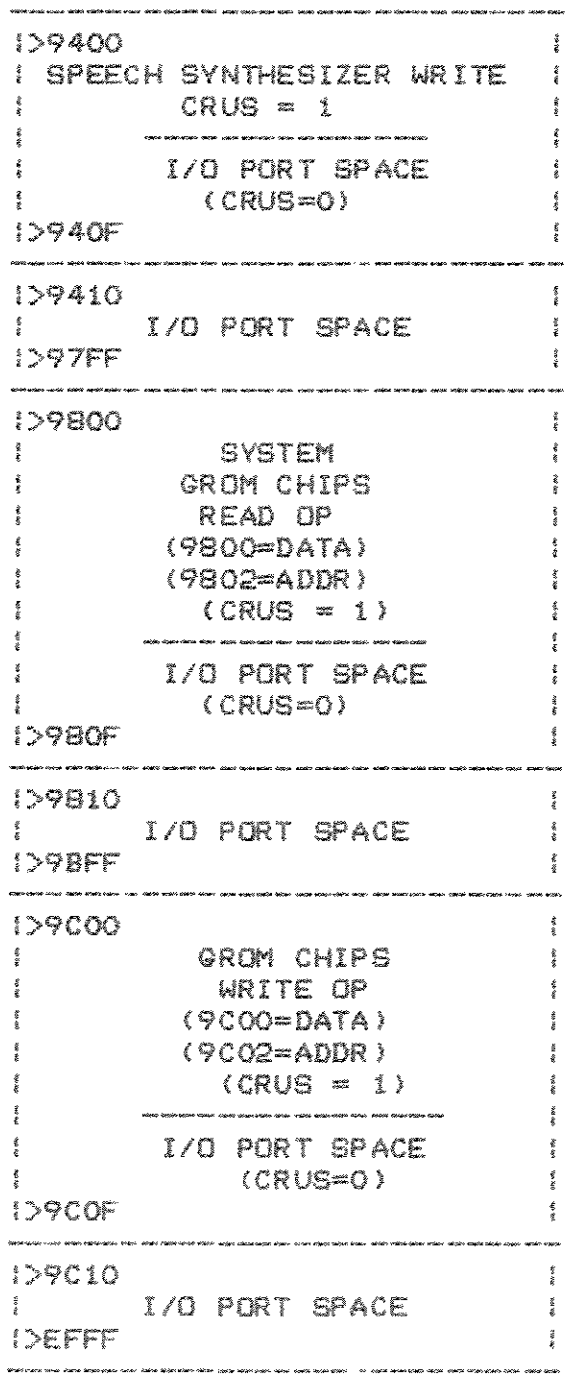
Any multiplicity of these bits may be ON in any LAS block.

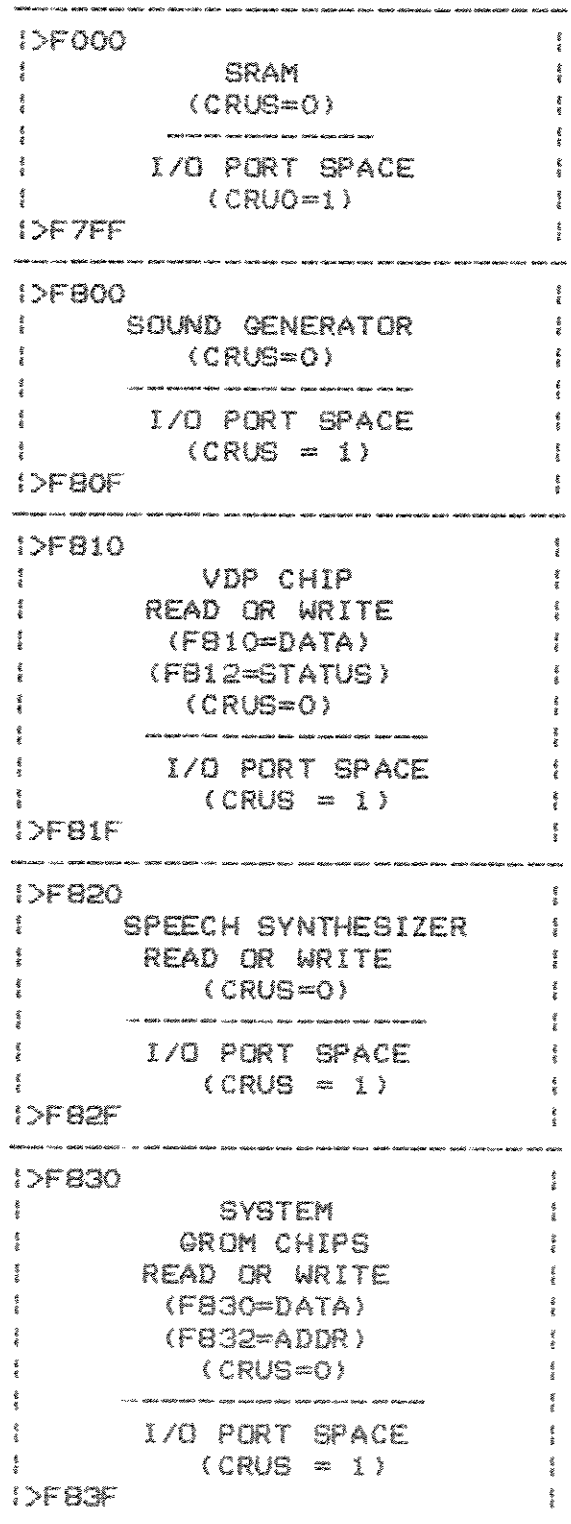
3.16 LOGICAL MEMORY MAP

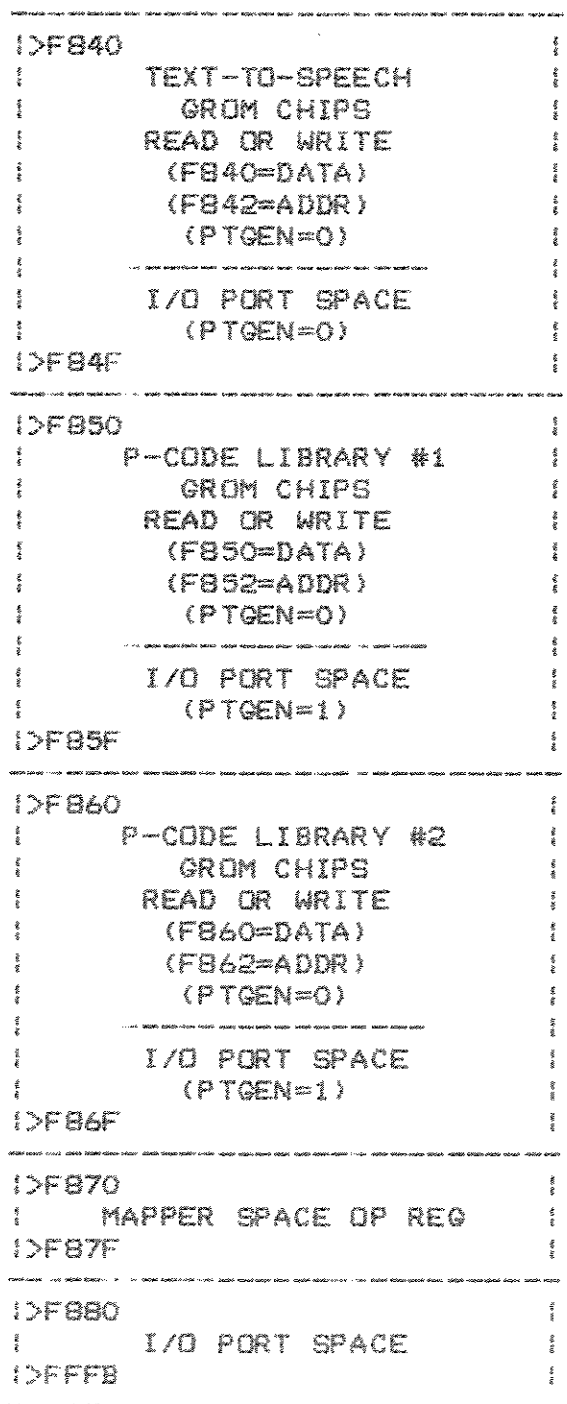
The following Memory Map shows the internal orgainzation of the Logical Address Space (LAS) of the ARMADILLO.

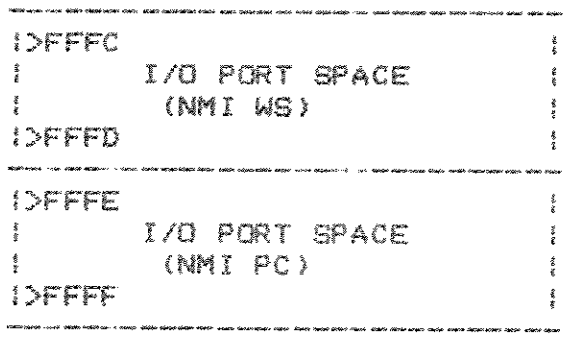



>8800
VDP READ
(8800=DATA)
(8802=STATUS)
(CRUS = 1)
I/O PORT SPACE
(CRUS=0)
>880F
>8810
MAPPER SPACE OP REG
>881F
>8820
I/O PORT SPACE
>8BFF
>8C00
VDP WRITE
(8C00=DATA)
(8C02=ADDR)
(CRUS = 1)
I/O PORT SPACE
(CRUS=0)
>8C0F
>8C10
I/O PORT SPACE
>8FFF
>9000
SPEECH SYNTHESIZER READ
CRUS = 1
I/O PORT SPACE
(CRUS=0)
>900F
>9010
I/O PORT SPACE
>93FF


>9400
SPEECH SYNTHESIZER WRITE
CRUS = 1
I/O PORT SPACE
(CRUS=0)
>940F
>9410
I/O PORT SPACE
>97FF
>9800
SYSTEM
GROM CHIPS
READ OP
(9800=DATA)
(9802=ADDR)
(CRUS = 1)
I/O PORT SPACE
(CRUS=0)
>980F
>9810
I/O PORT SPACE
>98FF
>9C00
GROM CHIPS
WRITE OP
(9C00=DATA)
(9C02=ADDR)
(CRUS = 1)
I/O PORT SPACE
(CRUS=0)
>9C0F
>9C10
I/O PORT SPACE
>EFFF

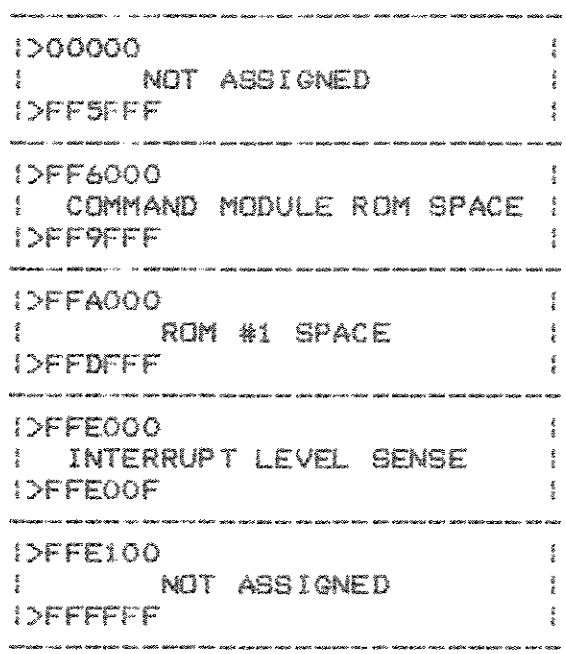

>F000
SRAM
(CRUS=0)
I/O PORT SPACE
(CRU0=1)
>F7FF
>F800
SOUND GENERATOR
(CRUS=0)
I/O PORT SPACE
(CRUS = 1)
>F80F
>F810
VDP CHIP
READ OR WRITE
(F810=DATA)
(F812=STATUS)
(CRUS=0)
I/O PORT SPACE
(CRUS = 1)
>F81F
>F820
SPEECH SYNTHESIZER
READ OR WRITE
(CRUS=0)
I/O PORT SPACE
(CRUS = 1)
>F82F
>F830
SYSTEM
GROM CHIPS
READ OR WRITE
(F830=DATA)
(F832=ADDR)
(CRUS=0)
I/O PORT SPACE
(CRUS = 1)
>F83F


>F840
TEXT-TO-SPEECH
GROM CHIPS
READ OR WRITE
(F840=DATA)
(F842=ADDR)
(PTGEN=0)
I/O PORT SPACE
(PTGEN=0)
>F84F
>F850
P-CODE LIBRARY #1
GROM CHIPS
READ OR WRITE
(F850=DATA)
(F852=ADDR)
(PTGEN=0)
I/O PORT SPACE
(PTGEN=1)
>F85F
>F860
P-CODE LIBRARY #2
GROM CHIPS
READ OR WRITE
(F860=DATA)
(F862=ADDR)
(PTGEN=0)
I/O PORT SPACE
(PTGEN=1)
>F86F
>F870
MAPPER SPACE OP REG
>F87F
>F880
I/O PORT SPACE
>FFFB


>FFFC
I/O PORT SPACE
(NMI WS)
>FFFD
>FFFE
I/O PORT SPACE
(NMI PC)
>FFFF

3.17 PHYSICAL ADDRESS MEMORY MAP

The following Memory Map shows the organization of the ARMADILLO Physical Address Space (PAS).



3.18 ONBOARD 64K BYTE DRAM

A 64K onboard DRAM shall be included. It shall be based at >00000 in the PAS.

3.19 INTERNAL DATA BUS CONTROL

The control of the Internal Data Bus shall be such that when a given device is mapped out of one LAS area into another LAS area, and another device is not put into the vacated space, that space shall be available through the I/O Port.

3.20 GROM BUS AND CONTROL BUFFERING

The GROM chips shall be isolated from significant load drive requirements, and all signals to the GROMs shall be driven or pulled up such that GROM loading and logic levels are observed.

3.21 COMMAND MODULE RESET

A definite System RESET shall be generated when a Command Module is plugged in without loading any power supply with a large capacitive load. The RESET shall be generated when the module is plugged in, but not when the module is removed. In addition, there shall be no waiting time between successive PLUG INs to insure that a RESET is generated.

3.22 MASTER OSCILLATOR

A 10.7386 MHz master oscillator shall be used to feed the TMS9995 and the 9118A VDP chip. The VDP shall be fed with as nearly symmetrical clock as is practical.

A means of adjusting the clock frequency to center band color shall be provided.

3.23 VDP CONNECTION

The VDP shall be mappable to one of two locations depending upon the state of the two CRU Configuration Bits. The Power Up default address shall be >8800 for a READ operation and >8C00 for a WRITE operation. The alternate address shall be F810 for both READ and WRITE operations. For more information, see the paragraph on the CRU Configuration Bits.

3.24 SOUND GENERATOR CONNECTION

The Sound Chip shall be logically connected such that it may be WRITTEN to only. The chip shall not be selectable for a READ operation.

The Power Up default address of the Sound Chip shall be >8400. It shall respond at >F800 as an alternate base. See the CRU Configuration Bit paragraph for more information. A "1"

indicates 99/4, and a "0" the Armadillo.

3.25 ON BOARD CRU

An on board CRU shall be included to comprehend interrupts, the cassette interface, the keyboard interface, and the joystick interface. This CRU shall be based at >0000 with the most significant 9 bits being decoded.

3.25.1 CRU Configuration Bit Definition. The CRU Configuration Bit shall be used to relocate the internal Memory mapped devices as shown in the Memory Map for the Logical Address Space (LAS).

3.25.2 RESET Bit. A SET BIT operation at a CRU Base of >2702 shall cause a Hardware RESET to occur.

3.25.3 CRU Bit Definition.

Disp	9901 Pin	LCP Function
1	INT1*	External Interrupt
2	INT2*	VDP Interrupt
3	INT3*	not used
4	INT4*	not assigned
5	INT5*	If LOW, an Expansion Box is connected.
6	INT6*	Joystick Fire Button
7/1F	INT7*/P15	Keyboard Row Sense (Bottom Row)
8/1E	INT8*/P14	Keyboard Row Sense
9/1D	INT9*/P13	Keyboard Row Sense
A/1C	INT10*/P12	Keyboard Row Sense (Top Row)
B/1B	INT11*/P11	Input from Cassette (MAG IN)
C/1A	INT12*/P10	Armadillo ID Bit (tied LOW, 99/4A tied HIGH)
D/19	INT13*/P9	Output to Cassette (MAG OUT)
E/18	INT14*/P8	Audio Gate
F/17	INT15*/P7	Speed Control Bit, 1=SLOW
10	P0	Encoded Keyboard Column Drive LSB
11	P1	Encoded Keyboard Column Drive
12	P2	Encoded Keyboard Column Drive
13	P3	Encoded Keyboard Column Drive MSB
14	P4	CRU Configuration Bit (CRUS)
15	P5	P-Code /Text-to-Speech GROM Library Enable Bit, 0=Enabled (PTGEN)
16	P6	Cassette Motor Control

3.26 KEYBOARD

Provisions for a 56 position Keyboard shall be made. It shall be organized in a 4 row, 14 column configuration, and there shall be no alternate action switches in the array. The Alpha Lock function shall be implemented in Software.

3.26.1 Keyboard Interface. A CRU based interface shall be included to drive 14 columns, and sense 4 rows. Scanning shall be accomplished with a 4-bit CRU Output which shall be decoded at the Keyboard to obtain drive for 14 columns. A 4-bit CRU Input shall be used to sense the four Keyboard rows.

The remaining 2 drive decodes from the 4-bit CRU Output lines shall be used in the Joystick sense.

3.26.2 Keyboard CRU Bit Definition.

Bit Disp	9901 Function	LCP Function
10	P0	Encoded Column Drive LSB
11	P1	Encoded Column Drive
12	P2	Encoded Column Drive
13	P3	Encoded Column Drive MSB
07	INT7*/P15	Row Sense LSB (Bottom Row)
08	INT8*/P14	Row Sense
09	INT9*/P13	Row Sense
0A	INT10*/P14	Row Sense MSB (Top Row)

3.27 JOYSTICK INTERFACE

The Joystick shall interface directly with the Keyboard logic to obtain a drive line for each Joystick, and four sense lines for the four directions. A separate CRU Input line shall be used to sense the FIRE Button. It shall be possible to use the Joystick Port for bidirectional I/O with the considerations noted in paragraphs for "Software Considerations".

3.27.1 Joystick CRU Bit Definition.

Bit Disp	9901 Function	LCP Function	
10	P0	Encoded Keyboard Drive LSB	⎫
11	P1	Encoded Keyboard Drive	⎬ 1110 #1
12	P2	Encoded Keyboard Drive	⎬ 1111 #2
13	P3	Encoded Keyboard Drive MSB	⎭
07	INT7*/P15	Joystick UP Sense	
08	INT8*/P14	Joystick LEFT Sense	
09	INT9*/P13	Joystick RIGHT Sense	
0A	INT10*/P12	Joystick DOWN Sense	
06	INT6*	FIRE Button Sense	

3.28 CASSETTE INTERFACE

A single Cassette interface that is compatible with existing tapes shall be included. Included shall be a READ control, a WRITE control, and a motor control. See the paragraph on CRU Bit definitions for more information.

The cassette interface shall be augmented with an Audio Gate, and there shall be no separate Audio In connector. Audio In will be available through the MAG IN jack (as it is on the 99/4A).

The MAG IN and MAG OUT signals for the recorder shall be available through minature (3.5 mm) audio jacks. The Cassete Motor Control signal shall be available through a sub-miniature (2.5 mm) audio jack.

3.29 HEXBUS INTERFACE

ADD LATER

3.30 SECOND DSR SPACE

ADD LATER

3.31 COMMAND PORT DEFINITION

The 99/8 Command Module Port shall closely resemble that of the 99/4QI, except that a 16K BYTE primary address space shall be supported.

3.31.1 Command Module Memory Capabilities. The Command Module shall support both GROM memories as well as Primary Memory space.

3.31.1.1 GROM Support. The Command Module Port shall support a total of four 5-chip GROM Libraries. There shall be no decode included in the console for unique library chip selects, and it shall be up to the user to provide this logic on the PCB that is to plug into the Command Module Port.

* Library 0 shall be that library normally associated with the base system, and shall be accessed at a displacement of >0 from the GROM base addresses described in the Logical Address Memory Map paragraph.

* Library 1 shall be accessed at a displacement of >4 from the GROM base addresses described in the Logical Address Memory Map paragraph.

* Library 2 shall be accessed at a displacement of >8 from the GROM base addresses described in the Logical Address Memory Map paragraph.

* Library 3 shall be accessed at a displacement of >C from the GROM base addresses described in the Logical Address Memory Map paragraph.

3.31.1.2 Command Module Primary Memory. A 16K BYTE Primary Address shall be supported, and it shall be accessed contiguously in the Physical Address Space based at >FF6000. Pseudo Static (Edge Triggered) ROMs shall function correctly when connected to this port.

3.31.1.3 Capacitance Loading. No more than 250 pF of capacitance loading shall be presented to any of the Command Module Bus signals.

3.31.1.4 Data Bus Drive Current. A minimum Source current of 200 uA at 2.4V shall be provided by any device driving either the Data Bus or the GROM READY status signal. That device shall also be capable of providing a minimum Sink Current of 1.0 mA at .4V.

3.31.2 Power Provisions. The Command Module Port shall make available to the Command Module no more than 335 ma of +5V current, and no more than 160 ma of -5V current. These levels comprehend GROM Libraries.

3.31.3 Command Module Port Pin Definition.

Pin #	Function	Pin #	Function
1	Command Mod Reset	19	+5V @ 335 ma Max
2	Logic Ground	20	Address Bus Bit 08
3	Data Bus Bit 7	21	Active LOW GROM CS
4	Address Bus Bit 02	22	Address Bus Bit 07
5	Data Bus Bit 6	23	Address Bus Bit 14
6		24	Address Bus Bit 03
7	Data Bus Bit 5	25	PDBIN, Data Bus Dir
8	Address Bus Bit 15	26	Address Bus Bit 06
9	Data Bus Bit 4	27	GROM Clock
10	Address Bus Bit 13	28	Address Bus Bit 05
11	Data Bus Bit 3	29	-5V @ 160 ma Max
12	Address Bus Bit 12	30	Address Bus Bit 04
13	Data Bus Bit 2	31	GROM READY Statis
14	Address Bus Bit 11	32	PWE*, Memory WRITE ENA
15	Data Bus Bit 1	33	Logic Ground
16	Address Bus Bit 10	34	Active LOW 16K Memory CS
17	Data Bus Bit 0	35	Logic Ground
18	Address Bus Bit 09	36	Logic Ground

3.32 SOFTWARE CONSIDERATIONS

The following is a list of Software requirements that must be obeyed when programming the Armadillo.

3.32.1 Power-Up Software. Power-Up software shall include SBO operations to provide active pull-up on internal CRU control bits. These bits are displaced from >0000 by >14, >15, and >17. Additionally, a CRU bit at >0400 shall be set to ONE to obtain Expansion Box operation for the ARMADILLO. Peripherals that must function at more than one clock speed or on different clock cycle counts shall use these locations for configuration. If we use our heads on this now, we will not screw to the wall the next crew that messes with this system!

3.32.2 Memory Mapped Device Access. The access of any byte oriented memory mapped device (VDP, Sound Chip, GROM chip) shall be performed in the BYTE mode; i.e., with MOVB instructions.

3.32.3 GROM Control. Hardware shall be included such that GROM Chip timing shall not be violated.

3.32.3.1 GROM Initialization. A single DATA READ from the GROM chips is required to initialize the chips for proper operation. A READ operation must be performed to insure that an Address WRITE goes to the proper byte in the Address Counter within the GROM chips. NOTICE ALSO THAT THIS MEANS A DUMMY READ FROM ALL GROM LIBRARIES!

3.32.4 GROM Accesses. Hardware shall be provided to limit GROM accesses such that there is at least a 5.6 us dead time between successive accesses. It is acceptable for programs to access at CPU speed; Hardware will take the CPU "NOT READY" if the 5.6 us dead time has not expired.

3.32.5 VDP Accesses. Hardware shall be provided to limit VDP accesses such that there is at least an 8 us dead time between successive accesses. It is acceptable for programs to access at CPU speed; Hardware will take the CPU "NOT READY" if the 8 us dead time has not expired. There shall be no differentiation made between VDP RAM and VDP REGISTER operations for dead time control.

3.32.6 Future Communications Through the Joystick Port. It will be necessary to keep an image of the 9901 configuration when the four sense lines (UP, DOWN, RIGHT, LEFT) are configured to be OUTPUTs. The only way to configure to be INPUTs again is to do a S/W RESET of the 9901. Since the Keyboard is not "Split" as it is in the 99/4, it will be necessary to devise some strange protocol to use this port for communications as the keyboard is the only operator interface (of course, there is the Power Switch as well as the External Interrupt).

3.33 I/O PORT

A buffered I/O Port shall be included to provide interface with the outside world through a 50-pin connector.

3.33.1 Data Path. This shall be a TTL driven line that connects to no MOS in the LCP. I/O Port pin assignments for the Data Bus are given in the I/O Port Pin Definition paragraph.

3.33.2 Address and Status/Control Signals. The Address and Status/Control interface to the outside world shall be as fully buffered as is practical and still meet cost goals. It shall be acceptable to feed the GROM Port with these buffered signals unless that signal feeds a GROM chip (A14 and BDIN both feed GROM chips).

3.33.3 Pin Definition.

Pin #	Function	Pin #	Function
1	UR5	26	UR5
2	RESET*	27	GND
3	EXTINT*	28	HOLD*
4	A5	29	A10
5	A4	30	A11
6	A12	31	A3
7	PDBIN	32	READY
8	LOAD*	33	GND
9	A13	34	A8
10	A7	35	A14
11	A15/COUT	36	A9
12	CRUCLK*	37	GND
13	PH3*	38	GND
14	PWE*	39	GND
15	A6	40	A2
16	A0	41	A1
17	PMEMEN*	42	GND
18	CRUIN	43	RDBENA*
19	D4	44	D7
20	D0	45	D6
21	D2	46	D5
22	D1	47	D3
23	SCLK	48	GND
24	IAQ/HDA	49	AUDIO IN
25	MSAST*	50	GND

SECTION 4

SYSTEM LEVEL DIAGNOSTICS

4.1 DIAGNOSTIC PHILOSOPHY

There shall be three basic levels of diagnostics to assist in both establishing the integrity of the machine as well as in the repair of the machine.

4.2 USER ORIENTED DIAGNOSTICS

This level of diagnostics is to be simple enough to allow the user to establish the integrity of the machine. It shall include, but not be limited to, such features as Keyboard to Display, Keyboard to Printer option, ROM CRC generation and check, system GROM CRC generation and check, and a full maintence RAM check. This Software shall be contained in a Command Module.

4.3 POWER-UP DIAGNOSTICS

Power up diagnostics shall be run at both power up and Reset. They shall include, but not be limited to, ROM CRC check, System GROM CRC check, and RAM check with a checker board pattern of >55, >AA, >55, >AA, etc. pattern spread through all of the existing RAM in the Mainframe. The Workspace shall be in the internal TMS9995 RAM at this time. This Software shall be contained in the DSR ROM.

4.4 MAINTENCE DIAGNOSTICS

Maintence diagnostics shall be tailored to Signature Analysis where practical, and shall also include scope sync loops. This paragraph will be detailed at the time when PCB design and debug work has been completed, and test hook locations have been established. This Software shall be contained in a Command Module.

4.4.1 RAM Testing. RAM testing shall be performed with, but not limited to, the following tests.

* Alternating 1's and 0's,
* Alternating 0's and 1's,
* Walking 1's,
* Walking 0's,
* Random bit pattern, non repeating on powers of 2,
* Bootstrap program execution/check.

4.4.2 ROM Testing. ROM testing shall be limited to generating and checking the CRC stored in the last two bytes of the ROM invloved.

4.4.3 GROM Testing. GROM tests at the system level shall be preformed just as the ROM tests were. Command Module Port testing shall be an option as these modules may have been manufactured at a date prior to the CRC requirement.

4.4.4 CPU Testing. A short test to generate a small data base using most 9995 instructions and then checked against the data base stored in the Boot ROM shall be performed.

4.4.5 VDP and Monitor Testing. Due to the abnormally long access times of the VDP chip, RAM testing shall be limited to a 55, AA, 55, AA, etc. bit pattern. Upon completion of this test, the standard power up screen shall be displayed.

4.4.6 Sound Testing. Sound chip testing shall be performed by programming several distinctively different sounds at several distinctively different intensities. The intent of this level of testing is to determine relative levels rather than ablolute values.

4.4.7 Keyboard Testing. The standard "RAKE" test shall be performed on the Keyboard. Testing shall go from left to right starting with the upper most keys, and continuing in a decending rows.

4.4.8 Outboard Device Testing. Where practical, diagnostic programs for any defined peripheral shall be contained in the DSR ROM for that peripheral.

SECTION 5

PRODUCTION ELECTRICAL TEST PLAN

5.1 COMPONENT LEVEL TESTING

All components shall be tested prior to being inserted into PCBs. PEP III parts will be used where available.

5.2 PCB BARE ETCH

All PCBs will be Bare Etch tested for Opens and Shorts.

5.3 ASSEMBLED PCB TESTING

All PCBs will be tested for Shorts and Opens where possible. In event that there are more points to be tested on the PCB than there are lines available in the test equipment, points for Opens testing shall be judiciously chosen. In addition the PCBs will be functionally tested at the board level.

5.4 FUNDAMENTAL TEST PHILOSOPHY

Signature Analysis shall be designed in to facilitate low TS&R times and low CND situations by providing field test instructions that are the same as those for the factory.

5.5 BURN IN

Burn In plans will be formed on the basis of information gained from Expansion Box experience. A 96 hr plan will be used regardless of whether Boards or Assembled Units are burned in.

5.5.1 Burn In Control. The UNITs in Burn In shall be linked via the Joystick Port to a host machine which will provide functional

test result data.

5.5.2 Power Cycling. The UNITs on Burn In shall be Power Cycled to improve reliability. The period shall be established experimentally.

5.6 RUN IN

Assuming BOARD Burn In, assembled units shall be run for a period of 4 hours at room temperature while running system level diagnostics and communicating with a host machine for data base checking. Neither operator intervention nor power cycling shall be required during Run In.

The UUT shall be linked via Joystick Port to a host machine which shall provide input data and shall check the data base generated by the UUT.

SECTION 6

ENVIRONMENTAL REQUIREMENTS

6.1 TEMPERATURE

6.1.1 Storage. The storage temperature range shall be from -40 deg C to +70 deg C.

6.1.2 Operating. The operating temperature range shall be from +10 deg C to +40 deg C.

6.2 HUMIDITY

6.2.1 Storage. The maximum storage relative humidity shall be 95% at +50 deg C.

6.2.2 Operating. The maximum operating relative humidity shall be 85% at +35 deg C.

6.3 ALTITUDE

6.3.1 Storage. The storage altitude range shall be from sea level to 40,000 ft.

6.3.2 Operating. The operating altitude range shall be from sea level to 15,000 ft.

6.4 VIBRATION

6.4.1 Operating. Sinusoidal vibrations of 0.8g 5--205 Hz for 30 minutes, applied along each of 3 mutually perpendicular axes for one hour.

SECTION 7

QUALIFICATION

7.1 GENERAL

QRA shall provide any special test requirements ASAP, and shall agree with the PCC on a QUAL plan prior to receiving any QUAL units. All preliminary PCB specs, theories of operation, etc. shall be given to QRA for consideration in the test plan if the information is available at the time that QRA can use it.

7.2 UNIT REQUIREMENTS

7.2.1 Type of Units Required for QUAL. The units presented for QUAL shall be production run units, and not custom units built only for QUAL.

7.2.2 Number of Units Required For QUAL. The number of units presented for QUAL shall be a minimum of 60 units.

7.3 SCHEDULE

TBD upon reciept of the QUAL Plan.

7.4 PACKING

TBD upon reciept of the QUAL Plan.

7.5 ENVIRONMENTAL

TBD upon reciept of the QUAL Plan.

7.6 STORAGE

7.6.1 High Temperature Storage. QRAS 10237 PARA 11.I- +70 deg C; 1000 hours storage at +70 deg C, RH less than or equal to 20%. Power up at room temperature after 168, 500, and 1000 hours.

7.6.2 Low Temperature Storage. QRAS 10237 Para 11.J -40 deg C; 1000 hour storage at -40 deg C, RH less than or equal to 60%. Power up after 168, 500, and 1000 hours.

7.6.3 High Humidity Storage. QRAS 10237 Para 11.K; 360 hour storage at 50 deg C, RH = 95% +/-2%. Verify operation after room temperature stabilization at 168, and 360 hours.

7.7 ELECTROMAGNETIC SUSCEPTIBILITY

MIL STD 461, 462 shall be run to verify the immunity of the 99/4 to both conducted and radiated susceptibility.

7.7.1 Conducted Susceptibility. CS01, CS02, CS06.

7.7.2 Radiated Susceptibility. RS01, RS02, RS03

7.8 INTERMITTANT OPERATION

QRAS 10237 Para 11.H; Power cycle one hour ON, one hour OFF for 1000 cycles at 25 deg C. Use three subgroups of two units: operate at 105 VAC, 117 VAC, and 130 VAC respectively.

7.9 TEMPERATURE

7.9.1 Operating. The operating temperature range shall be tested from +10 deg C to +40 deg C.

7.10 OPERATING HUMIDITY

GRAS 10237 Para 11.L: operate for 168 hours at 35 deg C, RH = 85% +/-2%.

7.11 ALTITUDE

7.11.1 Storage. The storage altitude range shall be from sea level to 40,000 ft.

7.11.2 Operating. The operating altitude range shall be from sea level to 15,000 ft.

7.12 SHOCK

7.12.1 Transit Drop In Shipping Carton. A packaged unit shall be dropped from a height of one meter on to a concrete floor as follows: one side, bottom, two corners, and two edges of carton.

7.12.2 Loose Cargo Bounce in Shipping Container. MIL-STD-810B Method 514.2, Procedure XI; para 4.6.12.2.1, 2, 3, 4 except limited to .1 inch double amplitude sinusoidal vibration and 24 Hz shall be used.

7.12.3 Drop Shock, Unpacked. Six inch drop from all sides with opposite side remaining on drop surface.

7.13 VIBRATION

7.13.1 Random Vibration in Shipping Container. MIL STD 810B, Table 514.1-V, Procedure X with 100 random vibration envelope modified as follows: 12 db/octave rise from 20-500 Hz and 24 db/octave fall from 500-20 Hz.

GRAS 10237 para 11.D; 30 minutes per plane.

7.13.2 Operating. GRAS, 10237, para 11.A, MIL STD 810B, Method 514-1, Procedure 7 per para 4.5.1.3, Test Curve AY.

7.14 OPERATING TEMPERATURE CYCLING

GRAS 10237 Para 11.G except temperature shall be +5 deg C to +48 deg C.

Five cycles from +5 deg C to +48 deg C; one hour at temperature extremes, and one hour between temperature excursions at ambient. PiQUALIFICATION)

7.14.1 UL. The ARMADILLO shall be UL qualified as the primary target. UL Std 114 shall be used.

7.14.2 CSA. The ARMADILLO shall be CSA qualified to CSA Std C22.2-154.

7.14.3 VDE. The ARMADILLO shall be qualified to VDE Std 380.

7.14.4 JIS. The ARMADILLO shall be qualified to JIS Std .

7.15 STATIC DISCHARGE

The LCP shall withstand a static discharge of 20KV to any part of the exterior surface.

7.16 EMI SUSCEPTIBILITY

7.17 FCC QUALIFICATION

The unit shall comply with FCC Docket #20780, Part 15, Subparts H and I.

7.18 INTERMITTENT OPERATION

All goals related to operating time shall be calculated on a 50% duty cycle.

SECTION 8

RELIABILITY

8.1 MTBF GOAL

The MTBF shall be in excess of 20,000 hours.

8.2 PRODUCT ACCEPTANCE GOALS

A 3083 Product Acceptance of 1.3 shall be used.

8.3 PACK VERIFICATION GOALS

A failure rate of .5% after burn in based on a sample size of 24 per lot shall be used for Pack Verification.

SECTION 9

MAINTAINABILITY

9.1 SERVICE GOALS

A MTTR of 15 minutes shall be used.

9.2 PHYSICAL SERVICE FEATURES

To aid in servicing, a single Main Logic PCB with designated test points shall be utilized utilized.

9.3 REPAIR CENTER SUPPORT PLAN

The PCC is to support the Repair Center with both documentation as well as training seminars.

9.3.1 TS&R Techniques To Be Used. The PCC shall provide test programs either on disk or in EGROM Command modules to facilitate fault verification and isolation.

9.3.1.1 Signature Analysis. Signature Analysis generators shall be provided by the PCC to generate the test patterns necessary for the use of Signature Analysis.

9.3.1.2 Scope Sync Loops. Short test programs shall be furnished by the PCC to sync a scope while exercising a given block of logic. These programs shall be determined during initial PCB debug, and shall be added to as need permits. The PCC shall support this effort as is needed.

9.3.2 Training By PCC Personnel. The PCC shall provide both PCB Specifications as well as a detailed PCB Theory of operation. A training seminar shall be taught by the PCC, and if the need exists, the session shall be video taped.

9.3.3 Documentation To Be Furnished. The PCC shall provide the following documentation:

* A full set of schematics of each PCB in the system,
* A set of specifications for each PCB in the system,
* A detailed theory of operation for each PCB in the system,
* A video tape of the training sessions if deemed necessary. The content of these tapes whall be driven by the first seminars.

9.3.4 Equipment Required.

* 50MHz Oscilloscope or faster.
* HP 5004A Signature Analyser or equivalent.

SECTION 10

PHYSICAL REQUIREMENTS

10.1 OUTSIDE DIMENSIONS GOALS

10.1.1 Console Dimensions. The Console dimensional goals are 17"W x 7"H x 10"D. GANDRE, FIX IT!

10.2 WEIGHT GOALS

10.2.1 Console Weight. The weight goal of the Console shall be 10 pounds. GANDRE, FIX IT!

10.3 AC POWER REQUIREMENTS

The AC input power shall be no greater than 150 Watts.

10.4 CASE MATERIALS

GANDRE, FIX IT!

10.5 PCB CONFIGURATION

The Main Logic Board area allocation shall be 10"x15", and connector locations shall allow two degrees in which to reduce PCB size.

The Power Supply PCB area allocation shall be 5"x7".

SECTION 11

PACKING

Packing and wrapping shall pass the Shock and Vibration tests as called out in these sections of the Specifications.

SECTION 12

COST REDUCTION PATHS

12.1 GENERAL

Any piecepart changes for cost reduction shall be approved by QRA Engineering.

12.2 LEADLESS CHIP CARRIERS

Leadless Chip Carriers shall be investigated for increased circuit density necessary to combine PCBs.

12.3 CUSTOM LOGIC/GATE ARRAYS

Both Custom Logic and Gate Arrays shall be investigated to futher reduce package count. All design shall comprehend this possibility where practical.

12.4 CHIP COMPONENT MOUNTING

Chip component mounting shall be explored for use on all of the LCP PCBs, and used where cost effective.

SECTION 13

FCC/PCC INTERFACE

13.1 TRAINING

The PCC shall provide both PCB Specifications as well as a detailed PCB Theory of operation. A training seminar shall be taught by the PCC, and if the need exists, the session shall be video taped.

13.1.1 Documentation To Be Furnished. The PCC shall provide the following documentation:

* A full set of schematics of each PCB in the system,
* A set of specifications for each PCB in the system,
* A detailed theory of operation for each PCB in the system,
* A video tape of the training sessions if deemed necessary.

13.2 PRODUCT HAND OFF

The product hand off from the PCC to the FCC shall be performed where applicable, to the CALD "Design-To-Production Product Phaseover of 12/27/76.

SECTION 14

UNIT IDENTIFICATION REQUIREMENTS

14.1 FCC IDENTIFICATION

The system nameplate shall have the assigned FCC ID number and the following note:

"Certified to comply with Class B limits, part 15 of FCC rules. See instructions if interference to Radio reception is suspected".

14.2 UL/CSA IDENTIFICATION

The System nameplate shall have the UL/CSA symbols as well as the appropriate listing numbers.

14.3 SERIALIZATION AND DATE CODING

Serialization and date coding shall occur on both the Mainframe and its plug in cards.

SECTION 15

DOCUMENTATION

15.1 USER'S MANUAL

Every LCP computer will be shipped with an OPERATOR'S MANUAL which includes service and warranty information.

15.2 HARDWARE FUNCTIONAL DESCRIPTION

A Hardware Functional Description manual shall be available at an additional cost. This manual shall detail system hardware well enough that new hardware may be designed for the system by personnel not directly associated with the LCP program.

In addition, any programming constraints shall be detailed to inform personnel not directly associated with the LCP who may wish to do programming (DSRs for new peripherals, etc).

15.3 SITE CODING

The site of manufacture shall be identified on the label.