AL4V8M440 Data Sheet

Version 1.0

Preliminary Version

Amendments

04.26.2004 Preliminary Version

AL4V8M440 8MBits FIFO Field Memory

Contents:

1.0 Description

The AL4V8M440 8Mbits (1,024k x 8-bit) FIFO memory provides completely independent 8bit input and output ports that can operate at a maximum speed of 80 MHz. The built-in address and pointer control circuits provide a very easy-to-use memory interface that greatly reduces design time and effort. Manufactured using state-of-the-art embedded high density memory cell array, the AL4V8M440 uses high performance process technologies with extended controller functions (write mask, read skip.. etc.), allowing easy operation of non-linearity and regional read/write FIFO for PIP, Digital TV, security system and video camera applications. Expanding AL4V8M440 data bus width is possible by using multiple AL4V8M440 chips in parallel. To get better design flexibility, the polarities of the AL4V8M440 control signals are selectable. The read and write control signals, such as Read/Write Enable, Input/Output Enable.., can be either active low or high by pulling /PLRTY signal to high or low respectively.

Available as a 44-pin TSOP (II), the small footprint allows product designers to keep real estate to a minimum.

2.0 Features

- 8Mbits (1,024k x 8 bits) organization FIFO
- Independent 8bit read/write port operations (different read/write data rates acceptable)
- Maximum Read/write cycle time: 80Mhz and 50Mhz (2 speed grades)
- Input Enable (write mask) / Output Enable (data skipping) control
- Selectable control signal polarity
- Self refresh
- 5V signals input tolerance
- 3.3V ± 10% power supply
- Standard 44-pin TSOP (II) package

3.0 Applications

- Multimedia systems
- Video capture or editing systems for NTSC/PAL or SVGA resolution
- Security systems
- Scan rate converters
- PIP (Picture-In-Picture) video display
- TBC (Time Base Correction)
- Frame synchronizer
- Digital video camera
- Hard disk cache memory
- Buffer for communication systems

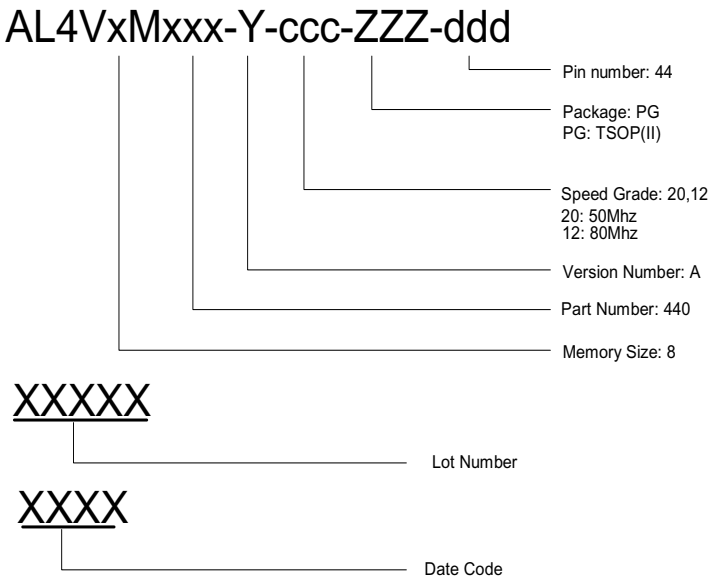
* 80MHz High-Speed version
- DTV/HDTV video stream buffer

4.0 Ordering Information

The AL4V8M440 has two speed grades, AL4V8M440-20 and AL4V8M440-12, which can operate at frequencies of 50MHz and 80MHz respectively. Both speed grades are powered by 3.3V and are available in a 44-pin standard TSOP-II package.

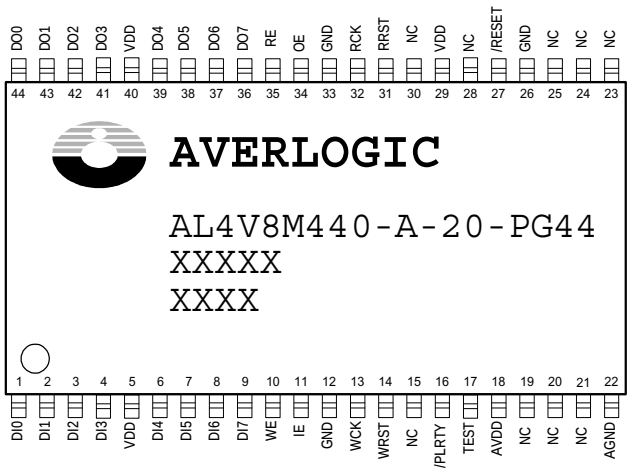
Part number	Package	Power Supply	Status
AL4V8M440-20/12 (50/80MHz)	PG44: 44-pin plastic TSOP(II)	+3.3V±10%	Sample 2004

4.1 Marking Information



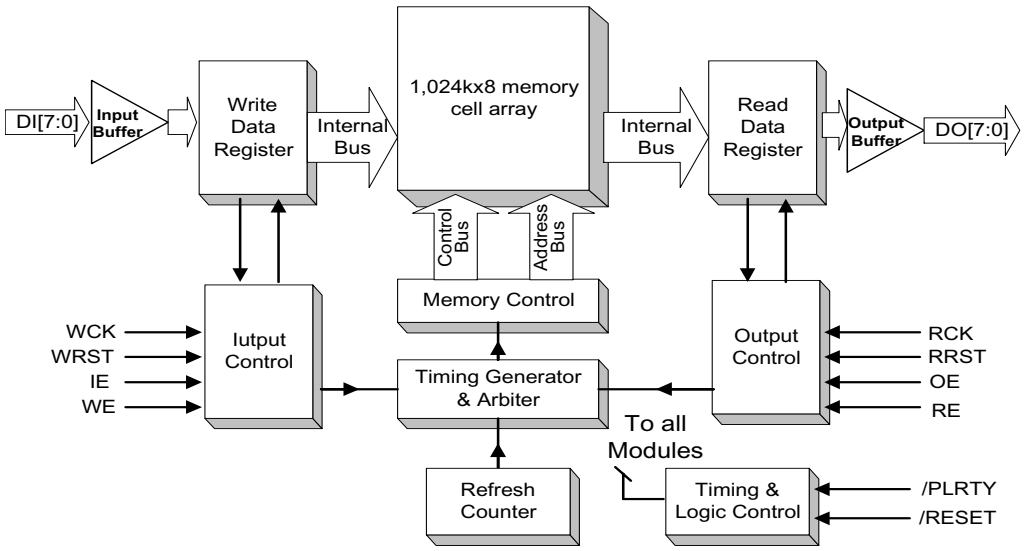
5.0 Pin-out Diagram

The AL4V8M440 pin-out diagram is following.



AL4V8M440-20/12 TSOP (II) pinout diagram (Top view)

6.0 Block Diagram



AL4V8M440 Block Diagram

The internal structure of AL4V8M440 consists of an Input/Output buffers, Write Data Registers, Read Data Registers and main 1,024k x8 memory cell array and the state-of-the-art logic design that takes care of addressing and controlling the read/write data.

7.0 Pin Definition and Description

The pin definitions and descriptions are as follows:

Write Bus Signals

Pin name	Pin number	I/O type	Description
DI[7:0]	9,8,7,6,4,3,2,1	I	The DI pins input 8bits of data. Data input is synchronized with the WCK clock. Data is acquired at the rising edge of WCK clock.
WE	10	I	WE is an input signal that controls the 8bit input data write and write pointer operation.
IE	11	I	IE is an input signal that controls the enabling/ disabling of the 8bit data input pins. The internal write address pointer is always incremented at rising edge of WCK by enabling WE regardless of the IE level.
WCK	13	I	WCK is the write clock input pin. The write data input is synchronized with this clock.
WRST	14	I	The WRST is an input signal that resets the write address pointer to 0.

*Note: For the polarity definition of all write control signals (WE, IE and WRST), please refer to /PLRTY pin definition and "Memory Operation" section for details.

Read Bus Signals

Pin name	Pin number	I/O type	Description
DO[7:0]	36,37,38,39,41, 42,43,44	O	The DO pins output 8bit of data. Data output is synchronized with the RCK clock. Data is output at the rising edge of the RCK clock.
RE	35	I	RE is an input signal that controls the 8bit output data read and read pointer operation.
OE	34	I	OE is an input signal that controls the enabling/ disabling of the 8bit data output pins. The internal read address pointer is always incremented at rising edge of RCK by enabling RE regardless of the OE level.
RCK	32	I	RCK is the read clock input pin. The read data output is synchronized with this clock.
RRST	31	I	The RRST is an input signal that resets the read address pointer to 0.

*Note: For the polarity definition of all read control signals (RE, OE and RRST), please refer to /PLRTY pin definition and "Memory Operation" section for details.

Power/Ground Signals

Pin name	Pin number	I/O type	Description
V_{DD}	5, 29, 40	-	3.3V ± 10%.
GND	12, 26, 33	-	Ground.
AV_{DD}	18	-	Dedicated power pin for the internal oscillator. 3.3V ± 10%.
AGND	22	-	Dedicated ground pin for the internal oscillator.

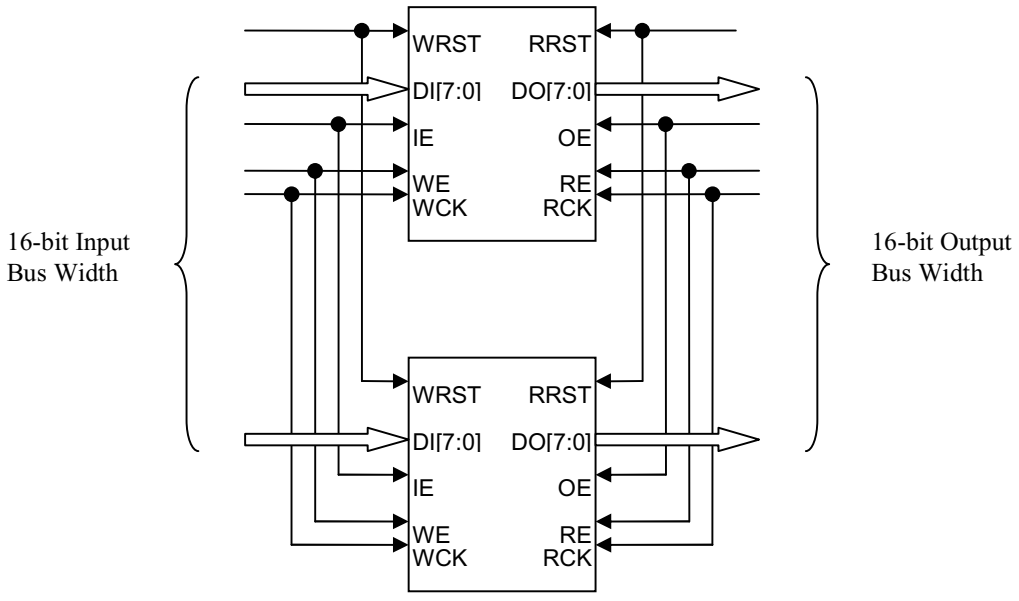
Miscellaneous Signals

Pin name	Pin number	I/O type	Description
/RESET	27	I	The global reset pin /RESET will automatically initialize chip logic and clear the window mode registers to 0. See Application note for the recommendation circuit of the global reset signal. Please refer to the Application Notes.

/PLRTY	16	I	Select active polarity of the control signals including WE, RE, WRST, RRST, IE and OE, totally 6 signals /PLRTY = V_{DD}, active low. /PLRTY = GND, active high. Note: During memory operation, the pin must be permanently connected to V_{DD} or GND. The pin has internal Pull-High as default active low, if /PLRTY has no connection. If /PLRTY level is changed during memory operation, memory data is not guaranteed.
TEST	17	I	For testing purpose only. Connect to Ground.
NC	15, 19, 20, 21, 23~25, 28, 30	-	No connect or connect to Ground

8.0 Multiple Devices Bus Expansion

The AL4V8M440 FIFO memory can be applied to very wide range of media applications. A parallel connect of multiple AL4V8M440 FIFOs provides extra FIFO bus width.



AL4V8M440 Data Bus Width Expansion

9.0 Memory Operation

9.1 Power-On-Reset & Initialization

During the system power on, a 200μs negative pulse on the /RESET pin is required and will automatically initialize chip logic and reset window mode registers to default value "0". Apply a valid reset pulse to WRST and RRST after power-on-reset to reset read/write address pointer to zero.

9.2 WRST, RRST Reset Operation

The reset signal can be given at any time regardless of the WE, RE and OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation will not be executed until cycles are enabled again.

9.3 Control Signals Polarity Select

The AL4V8M440 provides the option for operating polarity on controlling signals. With this feature, the application design can benefit by matching up the operation polarity between AL4V8M440 and existing interfacing devices without additional glue logic. The operating polarity of control signals WE, RE, WRST, RRST, IE and OE are controlled by /PLRTY signal. When /PLRTY is pulled high all eight signals will be active low. When /PLRTY is pulled low all eight signals will be active high.

9.4 FIFO Write Operation

In the FIFO write operation, 8 bits of write data are input in synchronization with the WCK clock. The FIFO write operation is determined by WRST, WE, IE and WCK signals and the combination of these signals could produce different write result. The /PLRTY signal determines the activated polarity of these control signals. The following tables describe the WRITE functions under different operating polarities.

/PLRTY = VDD

WRST	WE	IE	WCK	Function
L	-	-	↑	Write reset. The write pointer is reset to zero.
H	L	L	↑	Normal Write operation.
H	L	H	↑	Write address pointer increases, but no new data will be written to memory. Old data is retained in memory. (Write mask function)
H	H	-	↑	Write operation stopped. Write address pointer is also stopped.

/PLRTY = GND

WRST	WE	IE	WCK	Function
H	-	-	↑	Write reset. The write pointer is reset to zero.
L	H	H	↑	Normal Write operation.
L	H	L	↑	Write address pointer increases, but no new data will be

				written to memory. Old data is retained in memory. (Write mask function)
L	L	-	↑	Write operation stopped. Write address pointer is also stopped.

9.5 FIFO Read Operation

In the FIFO read operation, 8 bits of read data are available in synchronization with the RCK clock. The access time is stipulated from the rising edge of the RCK clock. The FIFO read operation is determined by RRST, RE, OE and RCK signals, consequently the combination of these signals could produce varying read results. The /PLRTY signal could decide the activated polarity of these control signals. The following tables describe the READ functions under different operating polarities.

/PLRTY = VDD

RRST	RE	OE	RCK	Function
L	L	L	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
L	L	H	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
L	H	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.
L	H	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
H	L	L	↑	Normal Read operation.
H	L	H	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
H	H	L	↑	Read address pointer is stopped. Output data is held.
H	H	H	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

/PLRTY = GND

RRST	RE	OE	RCK	Function
H	H	H	↑	Read reset. The read pointer is reset to zero. Data in the address 0 is output.
H	H	L	↑	Read reset. The read pointer is reset to zero. Output is high impedance.
H	L	H	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and data in the address 0 is output after RE goes low.
H	L	L	↑	Read address pointer is stopped. Output data is held. Read address pointer will be reset to zero and output is high impedance after RE goes low.
L	H	H	↑	Normal Read operation.

L	H	L	↑	Read address pointer increases. Output is high impedance. (Data skipping function)
L	L	H	↑	Read address pointer is stopped. Output data is held.
L	L	L	↑	Read operation stopped. Read address pointer is stopped. Output is high impedance.

When the new data is read, the read address should be between 192 and 524,287 cycles after the write address pointer, otherwise the output for new data is not guarantee.

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter		Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

10.2 Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Low Level Input Voltage	0	-	0.3 V_{DD}	V

10.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		Min	Typ	Max	Unit
I_{DD}	Operating Current	-	52	62	mA
I_{DDS}	Standby Current	-	14	-	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current (No pull-up or pull-down)	-5	-	+5	µA
I_{LO}	Output Leakage Current (No pull-up or pull-down)	-5	-	+5	µA
R_L	Input Pull-up/Pull-down Resistance		50		KΩ

1. Tested with outputs disabled (I_{OUT} = 0)
2. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.

10.4 AC Characteristics

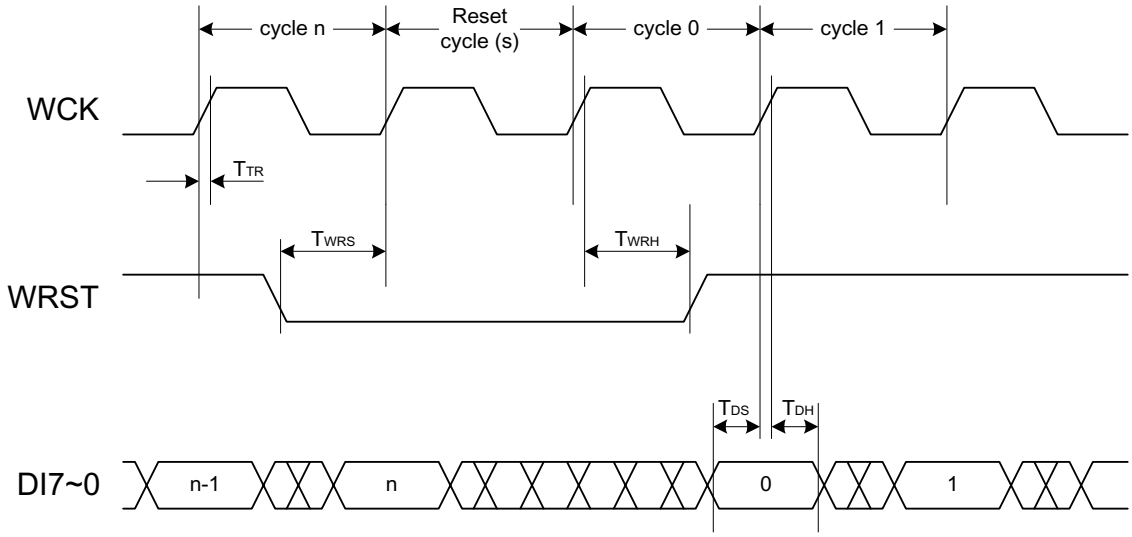
(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

Parameter		50MHz		80MHz		Unit
		Min	Max	Min	Max	
T_{WC}	WCK Cycle Time	20	-	12.5	-	ns
T_{WPH}	WCK High Pulse Width	7	-	5	-	ns
T_{WPL}	WCK Low Pulse Width	7	-	5	-	ns
T_{RC}	RCK Cycle Time	20	-	12.5	-	ns
T_{RPH}	RCK High Pulse Width	7	-	5	-	ns
T_{RPL}	RCK Low Pulse Width	7	-	5	-	ns
T_{AC}	Access Time	-	15	-	12	ns
T_{OH}	Output Hold Time	4	-	4	-	ns
T_{HZ}	Output High-Z Setup Time	3	15	4	-	ns
T_{LZ}	Output Low-Z Setup Time	3	15	5	-	ns
T_{WRS}	WRST Setup Time	5	-	4	-	ns
T_{WRH}	WRST Hold Time	2	-	5	-	ns
T_{RRS}	RRST Setup Time	5	-	4	-	ns
T_{RRH}	RRST Hold Time	2	-	5	-	ns
T_{DS}	Input Data Setup Time	5	-	4	-	ns
T_{DH}	Input Data Hold Time	2	-	5	-	ns
T_{WES}	WE Setup Time	5	-	4	-	ns
T_{WEH}	WE Hold Time	2	-	5	-	ns
T_{WPW}	WE Pulse Width	10	-	12	-	ns
T_{RES}	RE Setup Time	5	-	4	-	ns
T_{REH}	RE Hold Time	2	-	5	-	ns
T_{RPW}	RE Pulse Width	10	-	12	-	ns
T_{IES}	IE Setup Time	5	-	4	-	ns
T_{IEH}	IE Hold Time	2	-	5	-	ns
T_{IPW}	IE Pulse Width	10	-	12	-	ns
T_{OES}	OE Setup Time	5	-	5	-	ns
T_{OEH}	OE Hold Time	2	-	5	-	ns
T_{OPW}	OE Pulse Width	10	-	12	-	ns
T_{TR}	Transition Time	2	20	3	-	ns
C_I	Input Capacitance	-	7	-	7	pF

C_O	Output Capacitance	-	7	-	7	pF

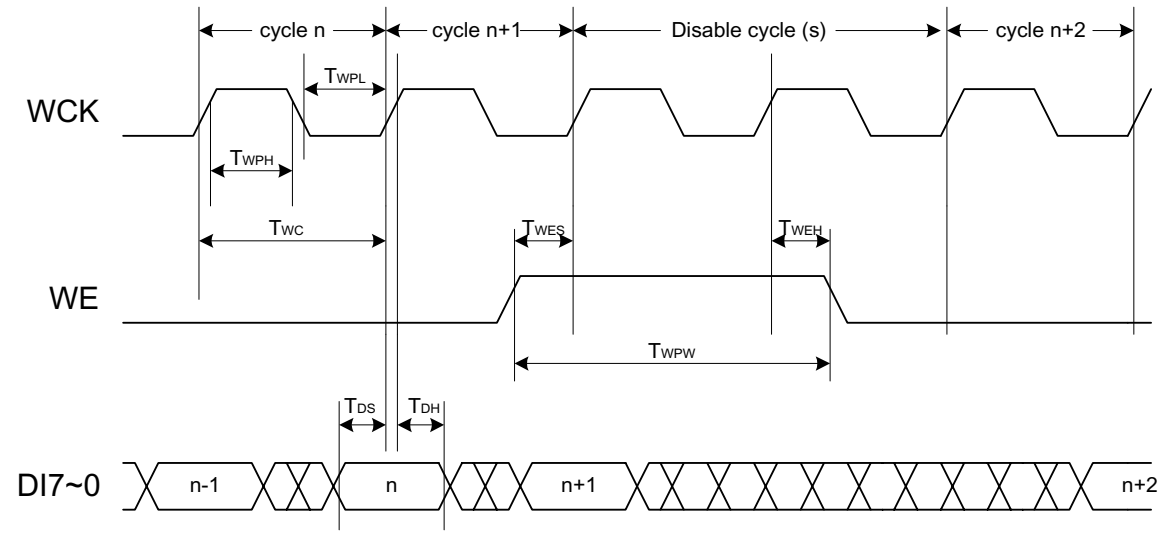
- The read address needs to be at least 192 cycles after the write address.

11.0 Timing Diagrams



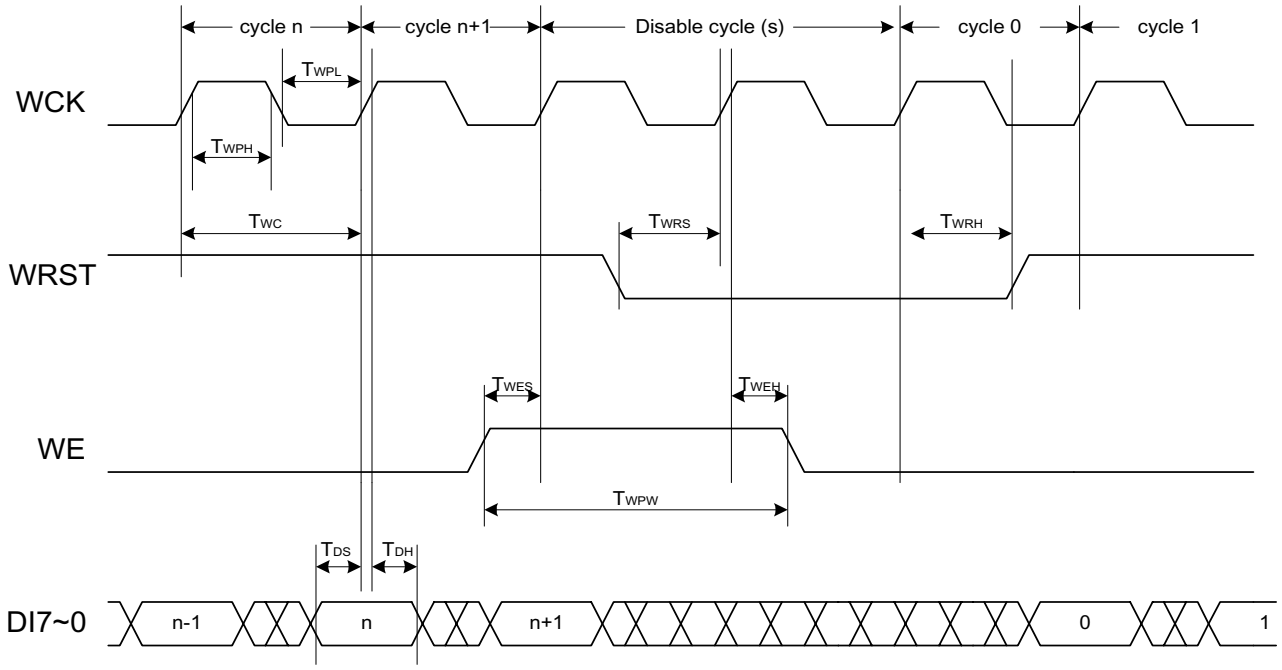
/PLRTY=VDD , WE= "L" , IE= "L"

Write Cycle Timing (Write Reset)



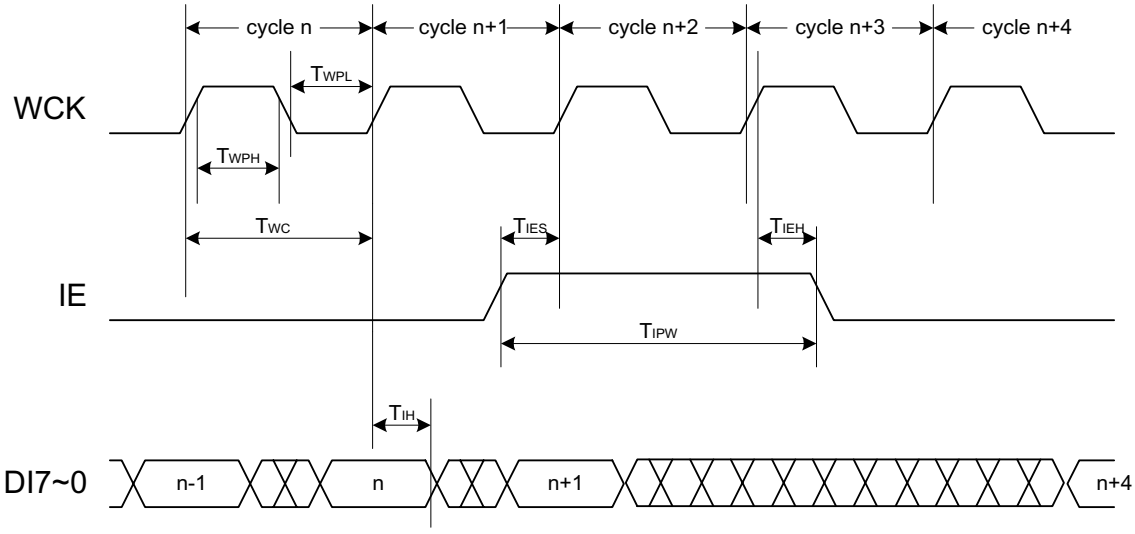
/PLRTY=VDD ,IE="L" ,WRST="H"

Write Cycle Timing (Write Enable)



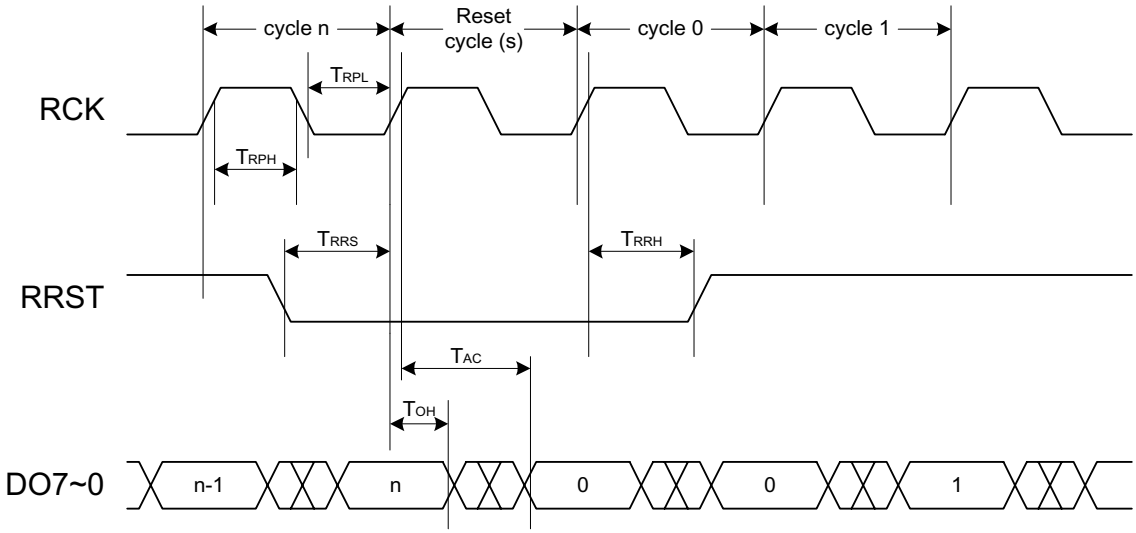
/PLRTY=VDD ,IE="L"

Write Cycle Timing (WE, WRST)



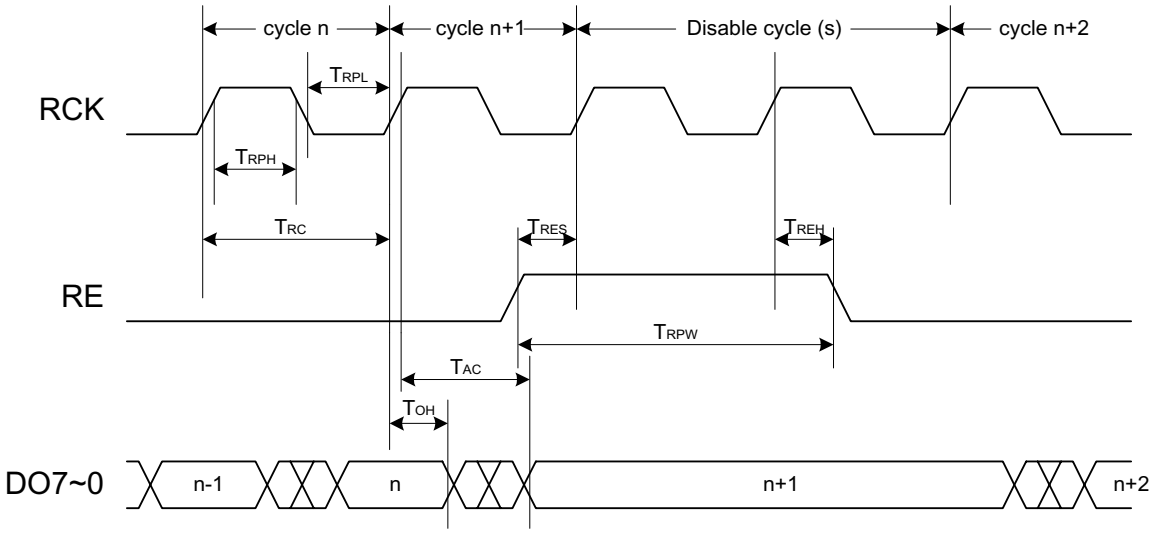
/PLRTY=VDD ,WE="L" ,WRST="H"

Write Cycle Timing (Input Enable)



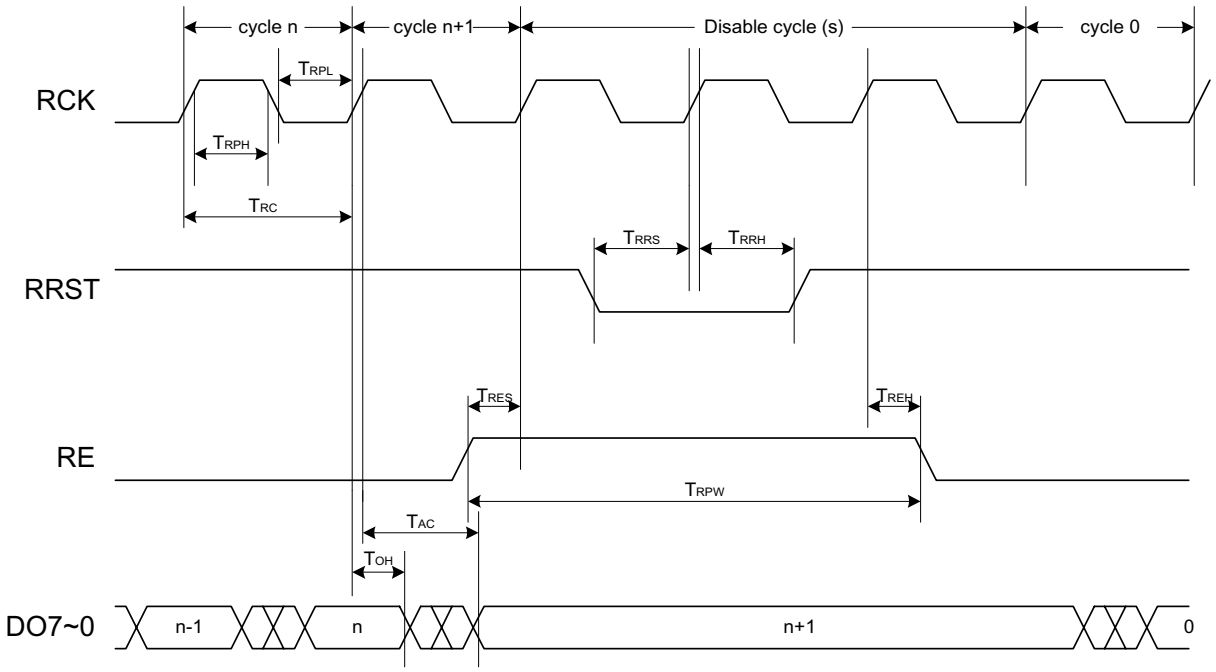
/PLRTY=VDD ,RE= "L" ,OE= "L"

Read Cycle Timing (Read Reset)



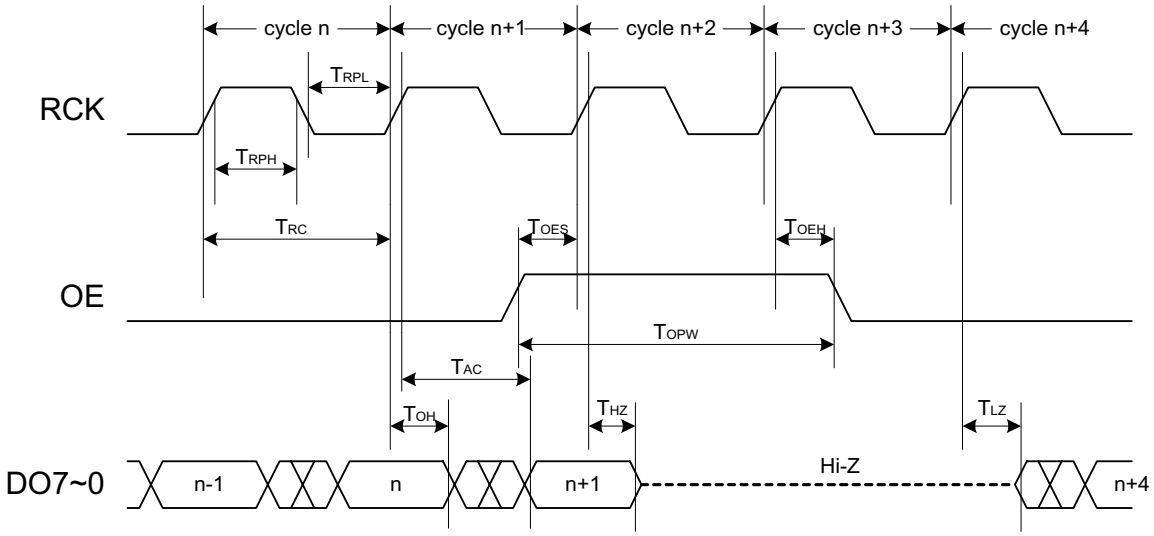
/PLRTY=VDD ,OE="L" ,RRST="H"

Read Cycle Timing (Read Enable)



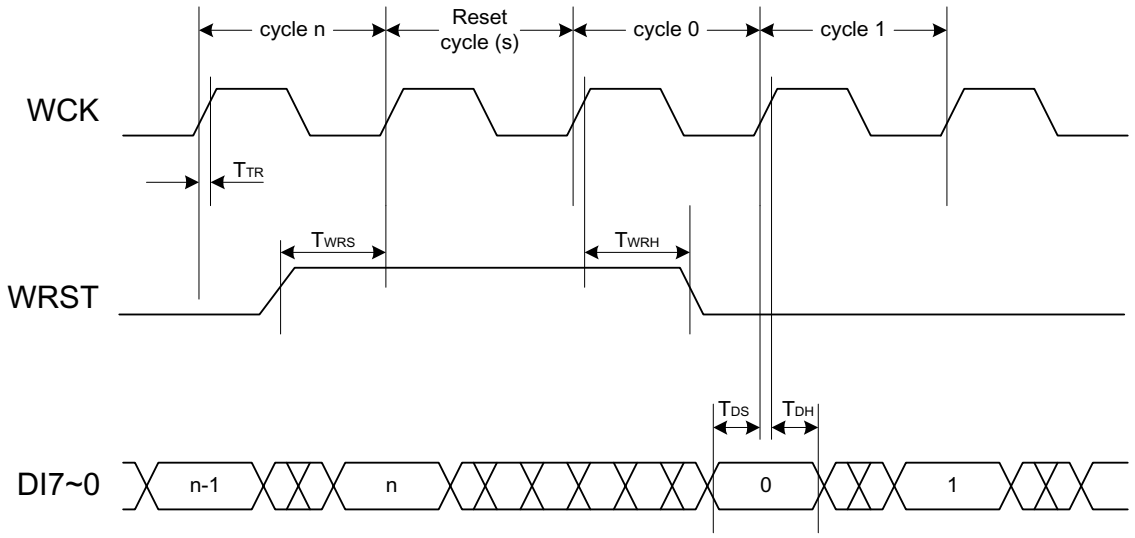
/PLRTY=VDD ,OE="L"

Read Cycle Timing (RE, RRST)



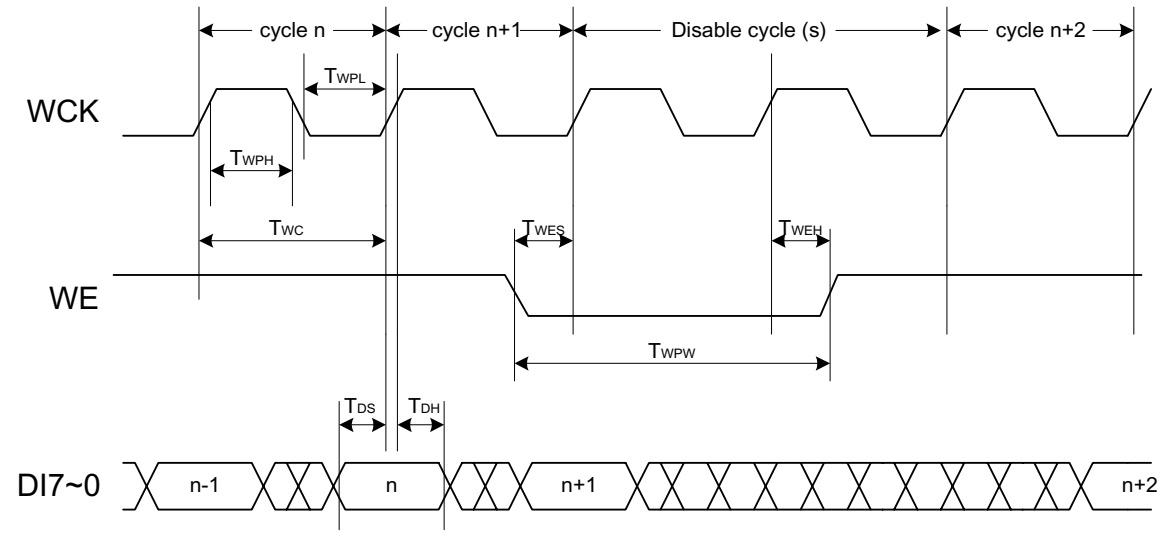
/PLRTY=VDD ,RE="L" ,RRST="H"

Read Cycle Timing (Output Enable)



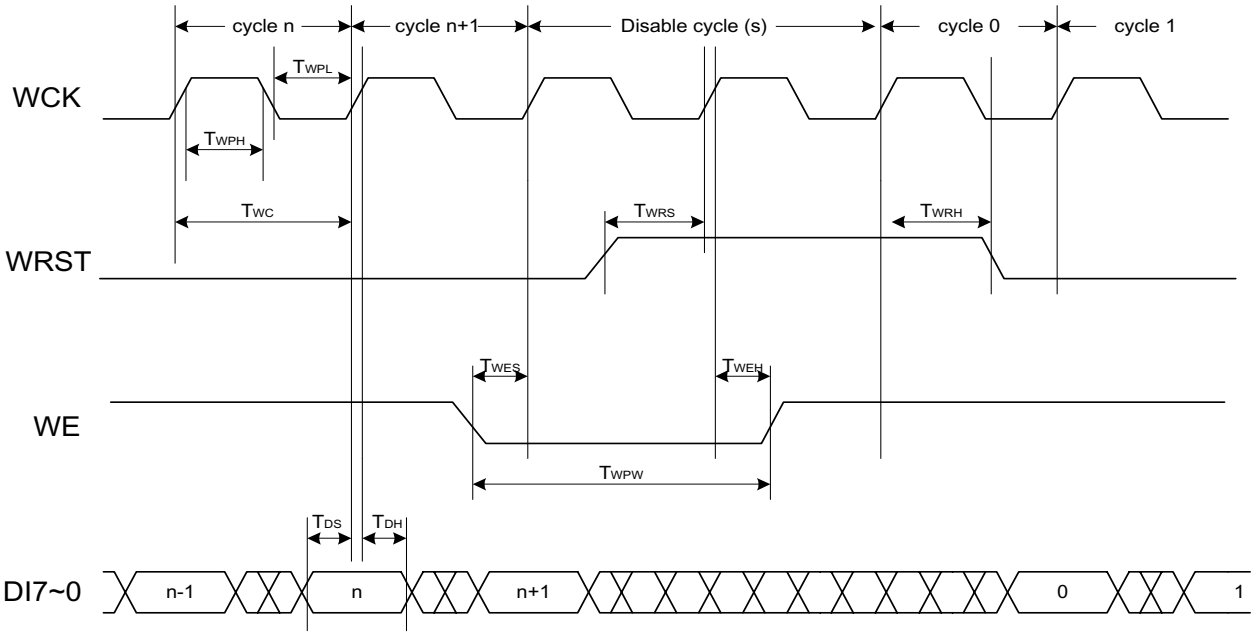
/PLRTY=GND , WE= "H" , IE= "H"

Write Cycle Timing (Write Reset)



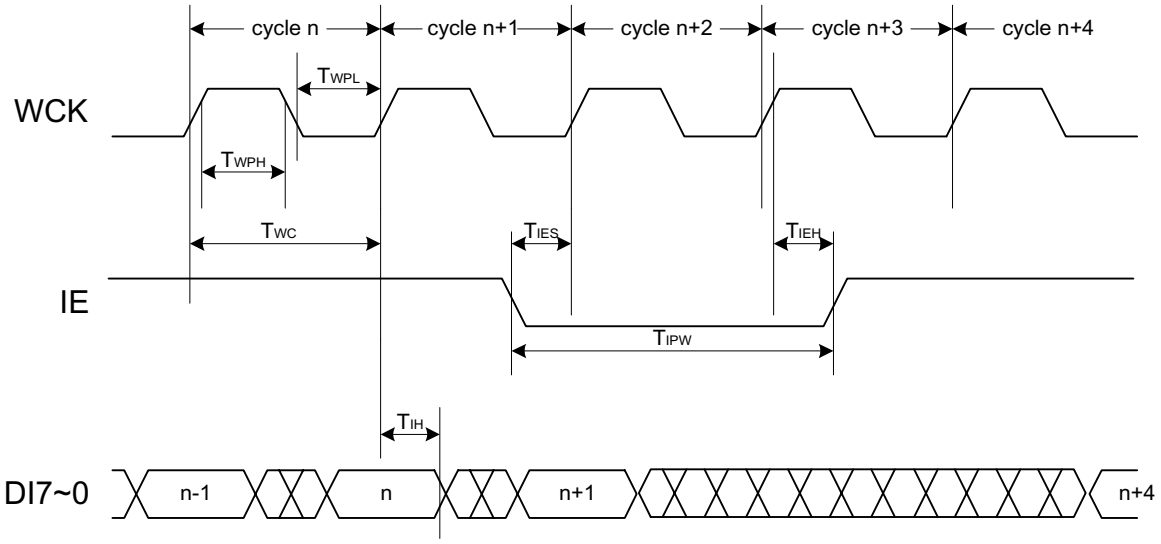
/PLRTY=GND ,IE="H" ,WRST="L"

Write Cycle Timing (Write Enable)



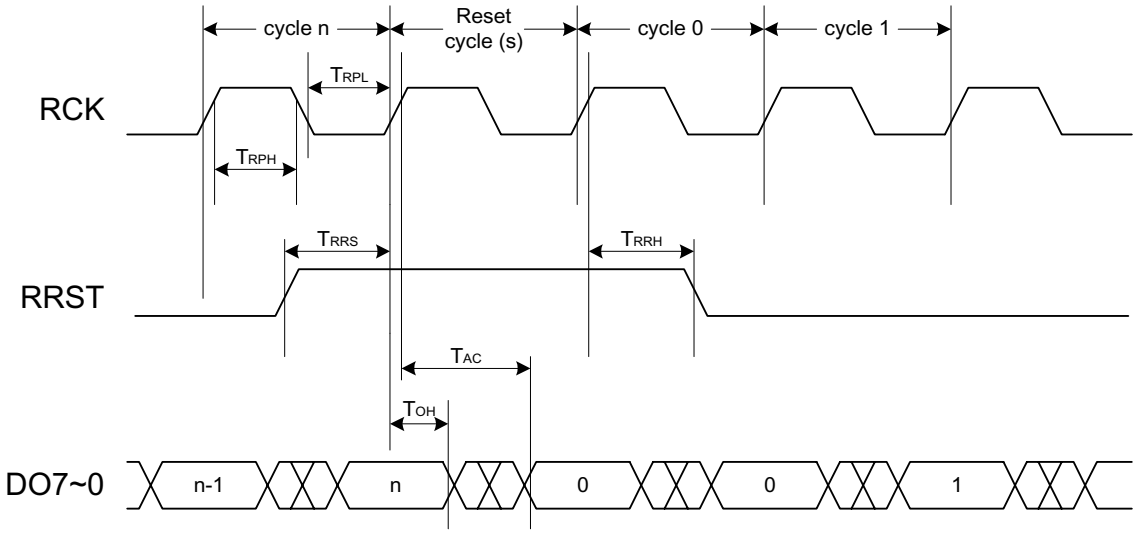
/PLRTY=GND ,IE="H"

Write Cycle Timing (WE, WRST)



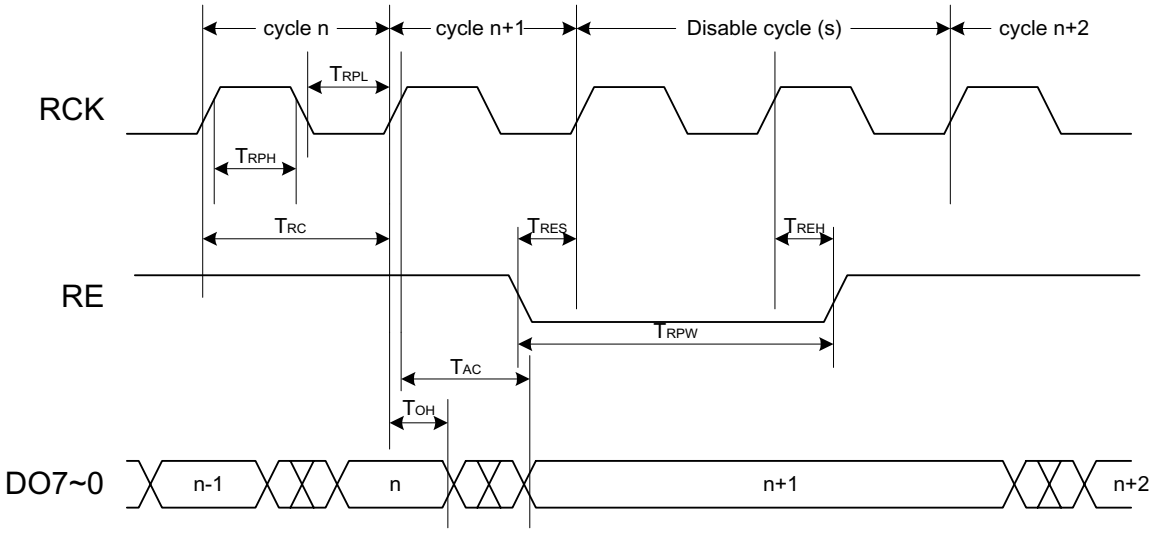
/PLRTY=GND ,WE="H" ,WRST="L"

Write Cycle Timing (Input Enable)



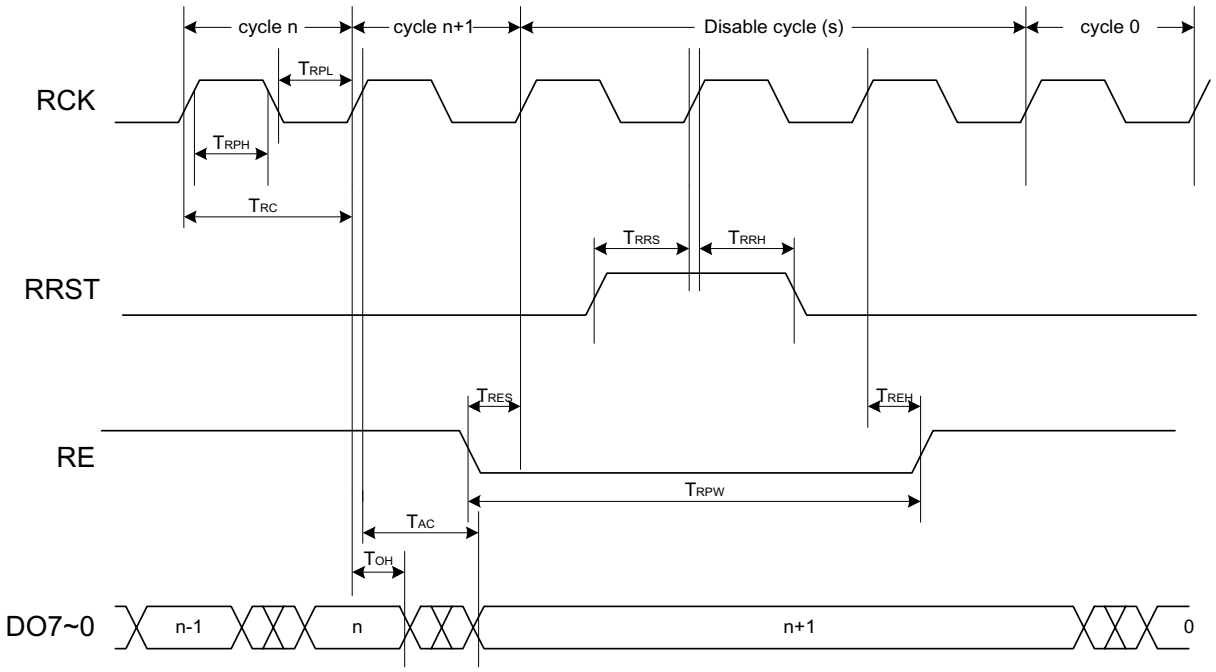
/PLRTY=GND ,RE= "H" ,OE= "H"

Read Cycle Timing (Read Reset)



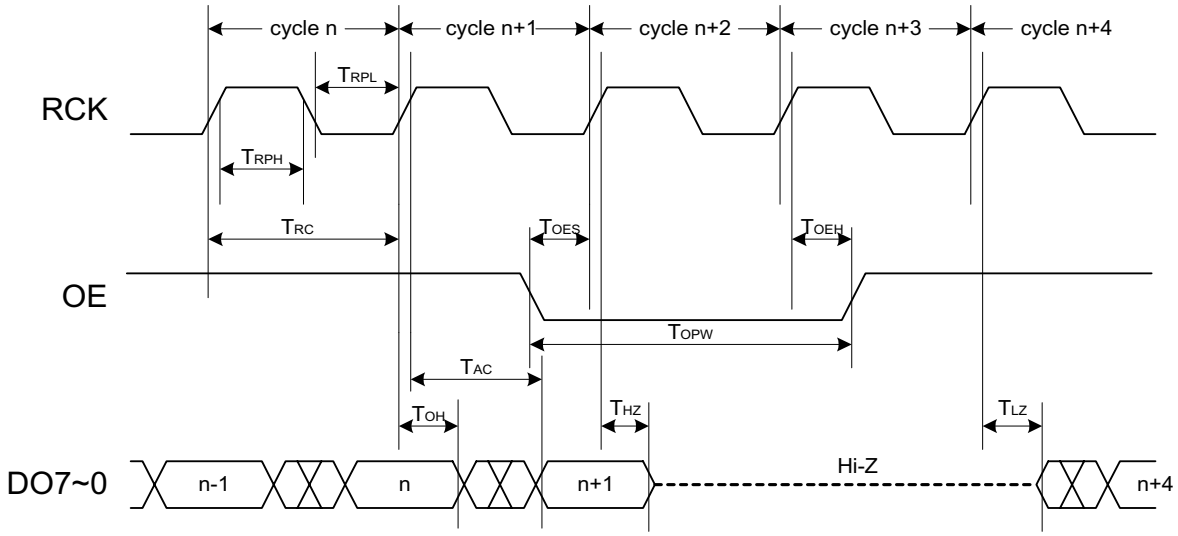
/PLRTY=GND ,OE="H" ,RRST="L"

Read Cycle Timing (Read Enable)



/PLRTY=GND ,OE="H"

Read Cycle Timing (RE, RRST)

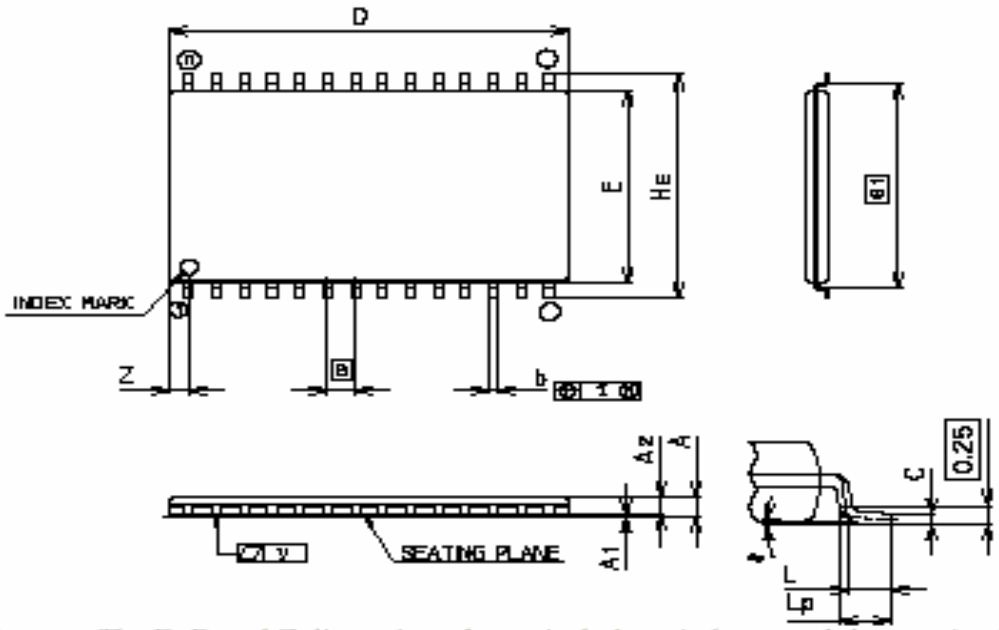


/PLRTY=GND ,RE="H" ,RRST="L"

Read Cycle Timing (Output Enable)

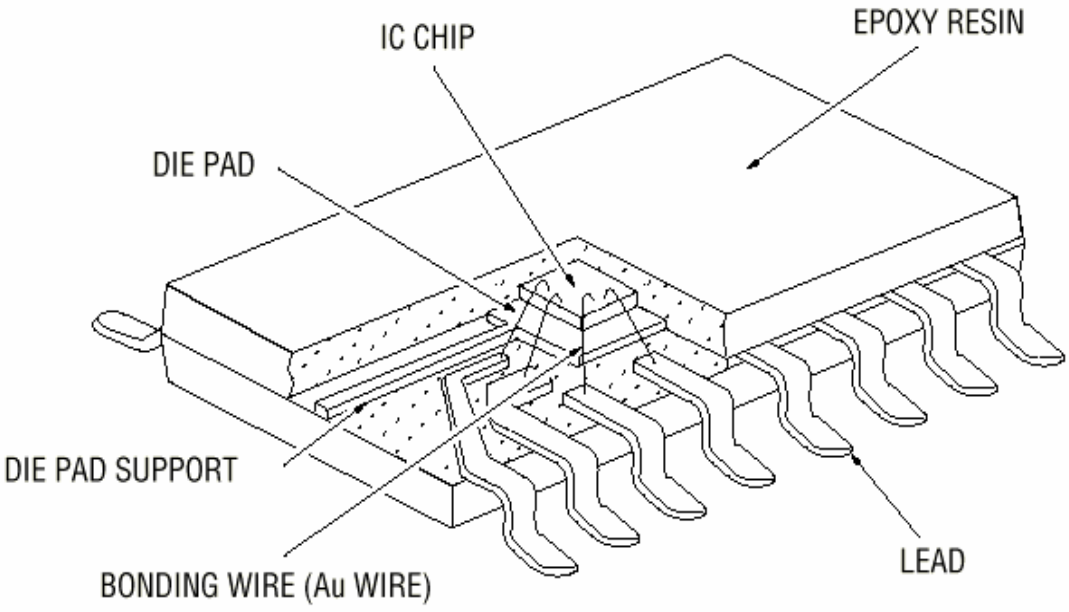
12.0 Mechanical Drawing – 44 PIN PLASTIC TSOP (II)

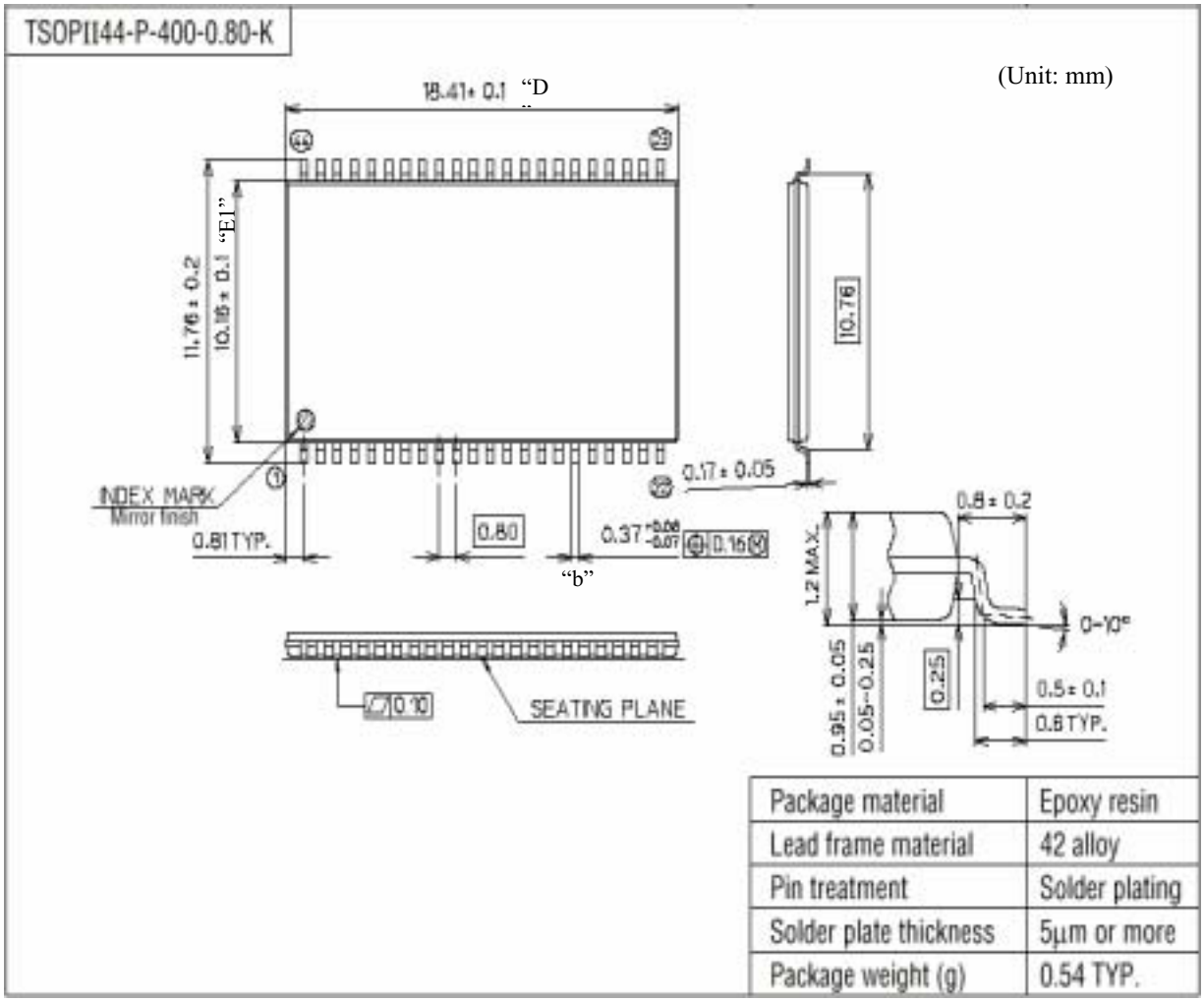
PLASTIC TSOP (Type II)



Note: The D, E, and Z dimensions do not include resin burrs and the remains from die pad support.

Package Structural Diagram





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5μm or more
Package weight (g)	0.54 TYP.

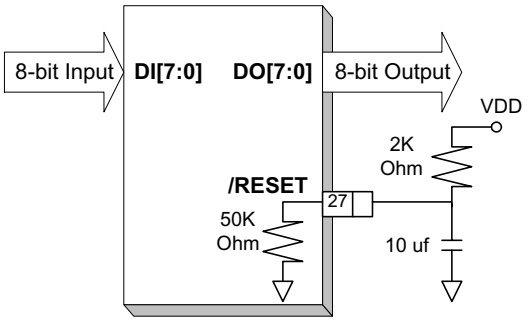
NOTE:

1. Controlling Dimension: Millimeters.
2. Dimension "D" does not include mold protrusion. Mold protrusion shall not exceed 0.15(0.006") per side. Dimension "E1" does not include interlead protrusion. Interlead protrusion shall not exceed 0.25(0.01") per side.
3. Dimension "b" does not include damar protrusions/intrusion. Allowable damar protrusion shall not cause the lead to be wider than the MAX "b" dimension by more than 0.13mm. Damar intrusion shall not cause the lead to be narrower than the MIN "b" dimension by more than 0.07mm.

13.0 Application Notes

13.1 Chip Global Reset Recommend Circuit

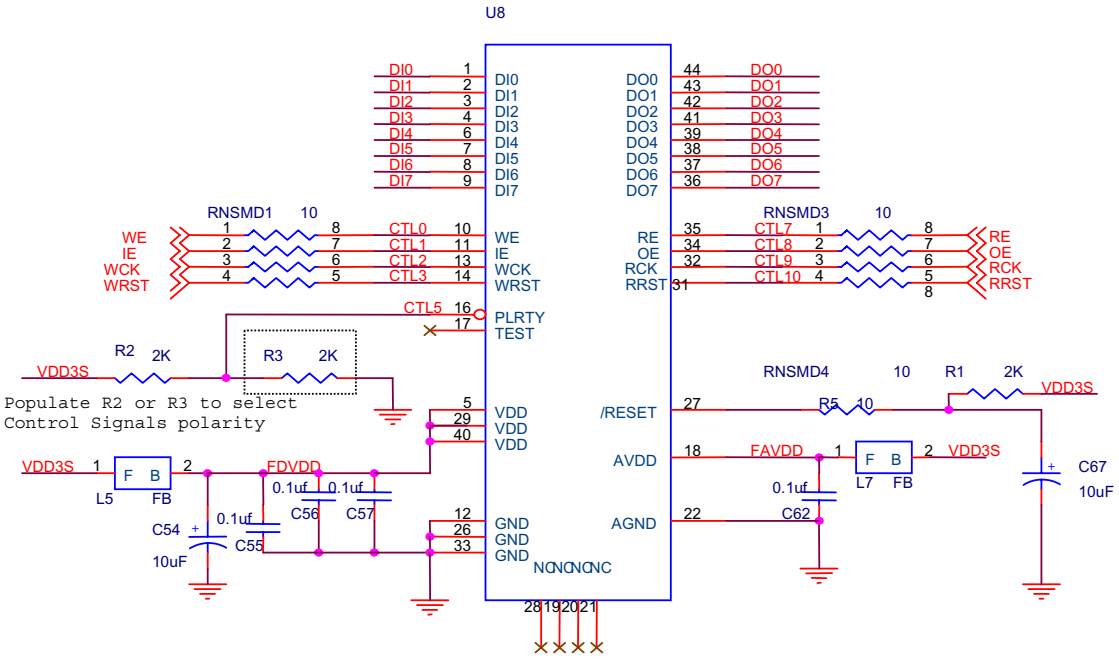
To ensure a proper reset pulse can be applied to /RESET pin (pin 27) to complete the power-on reset, the recommend reset circuit is to connect the AL4V8M440 /RESET pin (pin 27) to V_{DD} with a 2k Ω resistor and to Ground with a 10μf capacitor as follows.



AL4V8M440 Global Reset Circuit

It is also recommend adding buffers for the power-on reset circuit to increase the driving capability for any application with multiple AL4V8M440 chips.

13.2 The AL4V8M440 Reference Schematic



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