APPLICATION NOTE

High Performance Scaler SAA7140A(/B)

AN96053

Philips
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Abstract

This application note is intended to provide application support for the new Philips High Performance Scaler IC (HPS) SAA7140A(/B). It contains worked-out examples of application circuits for interfacing the HPS to the Video Input Processor SAA7111(/A) and the One Chip Frontend (OCF) SAA7110(A).

The SAA7111(/A) Video Input Processor converts the analog video input signal from the connector CVBS or S-Video to digital data, delivers the control signal and the line locked clock. The SAA7140A(/B) outputs the up- or down-scaled video picture. The VIP can easily be replaced by the OCF SAA7110(A).

This note gives a detailed description of the schematics and some hints how to design the PCB (printed circuit board) with mixed analogue and digital signal processing.

APPLICATION NOTE

High Performance Scaler SAA7140A(/B)

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Summary

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The SAA7111(/A) Video Input Processor converts the analog video input signal from the connector CVBS or S-Video to digital data, delivers the control signal and the line locked clock. The SAA7140A(/B) outputs the up- or down-scaled video picture. The VIP can easily be replaced by the OCF SAA7110(A).

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1. IC Description

1.1 HPS SAA7140A(/B)

The High Performance Scaler SAA7140A(/B) can scale pictures down to randomly-sized windows as well as horizontal zooming. Different processing and scaling functions can be switched either on two different video fields or from field to field to an new setup for video effects. The horizontal scaling is done by prefiltering and two-dimensional phase correct interpolation. Vertical scaling is implemented in a linear phase interpolation mode and for scaling smaller than half of the input size the accumulation mode calculate the high quality output picture. All the features are explained in the data sheet of the SAA7140A and SAA7140B. The SAA7140B operates in an 3 Volt environment. Some programming examples for different scaling are given later in this report.

The standard digital 16 bit YUV video input port of the HPS accepts all Philips 8 bit digital multistandard decoders, as the SAA7110(A) and the SAA7111(/A). A second port is the 16 bit bi-directional expansion port, supporting full duplex D1 and half duplex YUV data. These data are resynchronized to the horizontal and vertical reference signal and upsampled to 24 bit Y, U and V data. Brightness, saturation and contrast can be set via I2C bus. After the high performance scaling processing the data and its control signal are send to the output formatter. The data are configurable in various output formats in RGB or YUV representation. All controlsignal for easy interfacing to other circuits are output parallel to the data, the pixelqualifier indicates the valid data in the line and valid lines in the field. The output-clock can run synchronous to the scaler input clock, the transparent mode. If the data shall be transfered into a bus-system, the burst mode is recommended. In this mode the output-clock must be higher, the data are buffered in an internal fifo and read out in blocks to reduce the load at the bus.

1.2 VIP SAA7111(/A) (optional OCF SAA7110(A))

The video acquisition, the colour decoding and the clock generation is based on the SAA7111(/A) Video Input Processor. The decoder block performs luminance processing as well as chrominance processing for PAL B/G, NTSC-M and its substandards. The decoded luminance and colour difference signals (YUV) can be adjusted for brightness, contrast and colour saturation, the digital output levels can be programmed to comply with the CCIR-601 recommendation. The synchronization unit derives horizontal and vertical timing signals from the input signal.

The single 24.576 MHz quartz crystal oscillator is used as timing reference for the clock generation. The decoder drives the clock generator to obtain a sampling clock that is locked to the line frequency of the incoming video signal. The line-locked sampling clock ensures that always the orthogonal sampling raster can be maintained even with non-standard input signals coming from sources like a video recorder. The resulting clock frequency signal of 27 MHz and its reference signal is output for further use in the application.

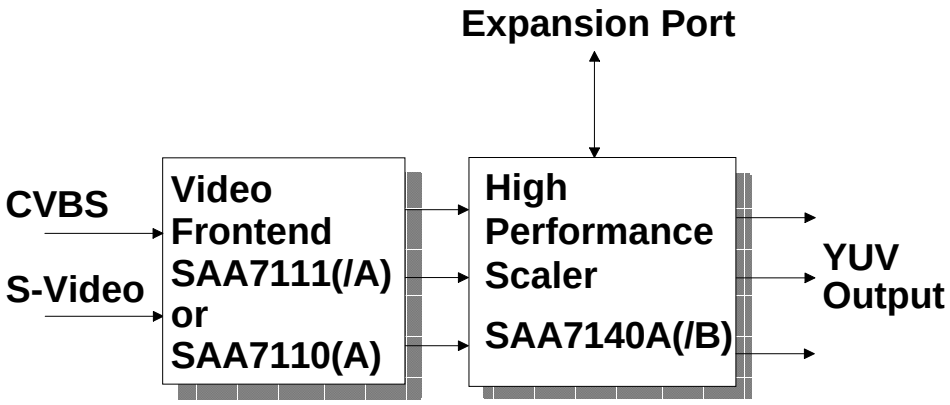
The SAA7111(/A) contains two 8 bit CMOS analogue to digital converters to digitize the incoming video input signals. The IC features two identical analogue preprocessing channels, source select switches allow to connect the converters to the desired analogue channel. The preprocessing channels perform automatic gain control, clamping and peak-white limiting of the input signal as well as lowpass filtering to prevent aliasing.

The frontend can optional be stuffed by the SAA7110(A) One Chip Frontend. The modification is documented in the schematics and the pin description of the datasheet.

2. Circuit Description

The analogue CVBS or S-Video signal is converted and decoded in the video frontend SAA7111(/A). The digital YUV output data in 4:2:2 format, the control signal HREF and VS are send to the HPS SAA7140A(/B). The output of the HPS is set to YUV 4:2:2 format in transparent mode. All control signal to the following applicationspecific circuit are delivered from the SAA7140A(/B).

Blockdiagram Video Frontend and Scaler:



3. Schematics

The video frontend schematics include all additional resistors to install the SAA7111(/A) as well as the SAA7110(A). To reduce high frequent ringing at the clock line, when this wire is very long, R9 may be replaced by 33R. The fourth analog input (pin 17) can optional be used.

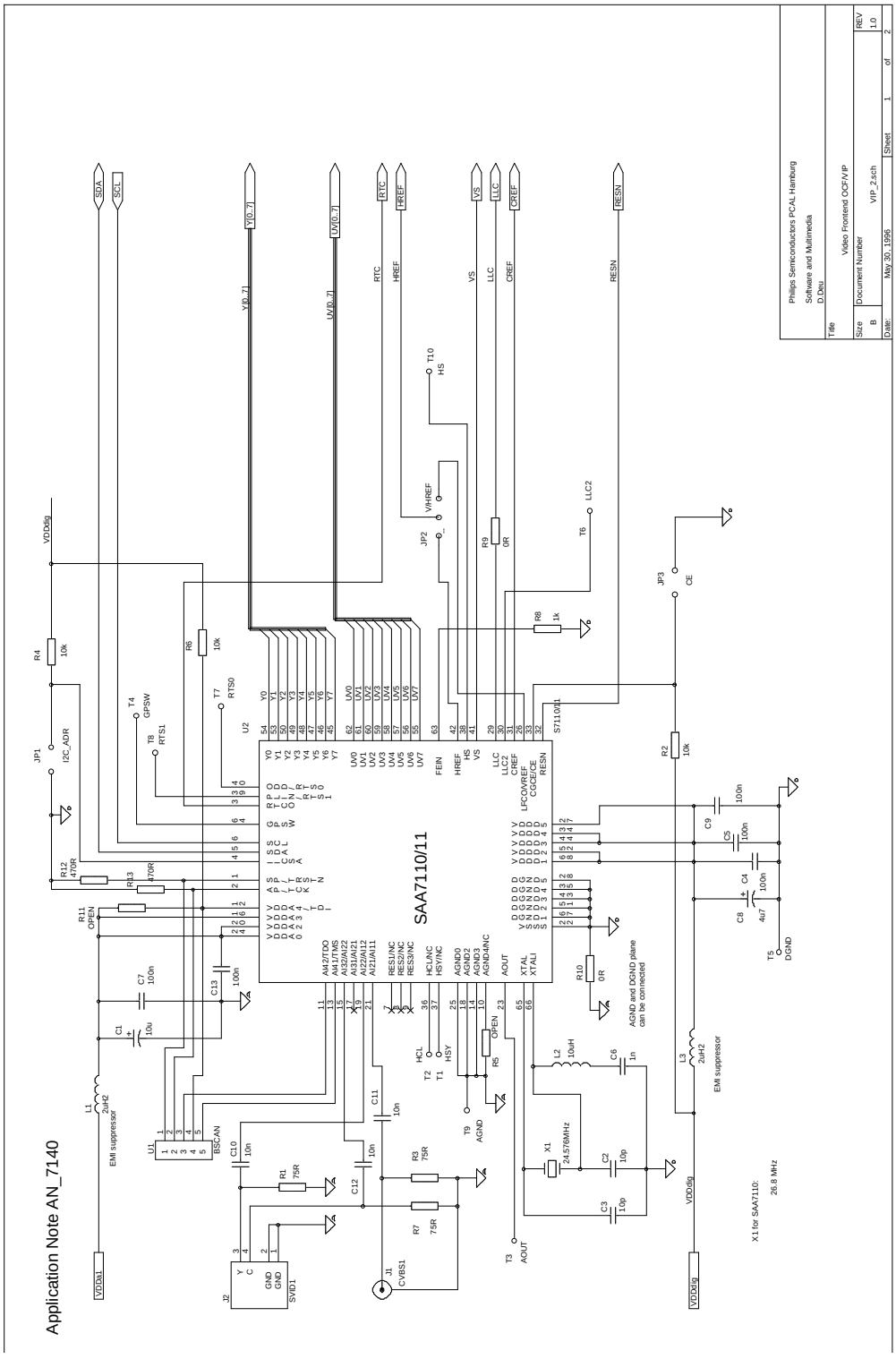
The power supply pins of the VIP and the HPS should be decoupled as close as possible to the pins of the IC. The separate analog and digital ground planes can be connected at the PCB by R10. The placement of this connection should be optimized at the final board for best signal/noise performance.

The signal port 0..3 at the HPS sheet is free programmable via I2C bus as input or output for general use.

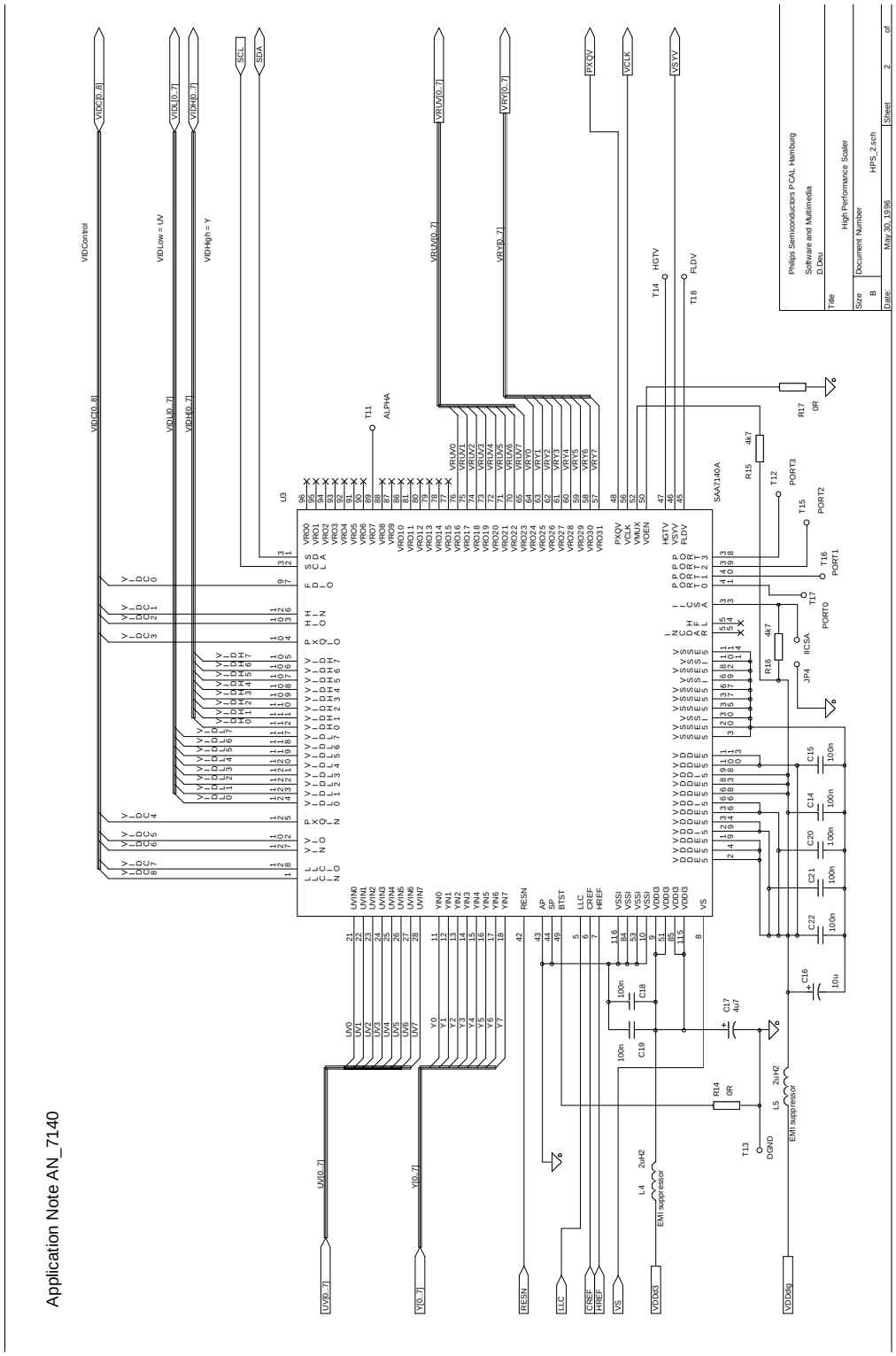
All EMI suppressors in the power supply line should have a very low resistance.

The SAA7140B is designed for a complete 3Volt system environment. All power supply pins must be connected to 3 Volt supply.

3.1 Schematics SAA7111(/A)



3.2 Schematics SAA7140A



4. Connector Description

4.1 Video Input Connectors

The analogue video input signal CVBS is fed to the colour decoder via the RCA Jack (Cync) connector J1. The determination is 75 Ohm.

The analogue S-Video input signal is connected to the Hosiden Y/C J2. The determinations for the luminance and chrominance channel are 75 Ohm.

4.2 Boundary Scan Connector U1

For test purposes the boundary scan pins of the SAA7111(/A) are connected.

Pin 1 TRSTN
Pin 2 TCK
Pin 3 TDO
Pin 4 TDI
Pin 5 TMS

5. I2C Bus default Setups

The listed tables will give some startup sets for the I2C bus programming of the SAA7140A(/B). The programming of the SAA7111(/A) is described in the data sheet.

TABLE 1 I2C bus setup SAA7140A(/B)

Subaddress	Bypass Frame Data	Zoom x2 1 Field Data	Scale 1/2 1 Field Data	Scale 1/4 1 Field Data	Scale 1/3 1 Field Data	Icon 1 Field Data
00	3C	3C	3C	3C	3C	3C
01	F0	F0	F2	F2	F2	F2
02	0	0	0	0	0	0
03	10	10	10	10	10	10
04	1D	1D	1D	1D	1D	1D
05	80	80	80	80	80	80
06	40	40	40	40	40	40
07	40	40	40	40	40	40
08	0	0	12	12	12	12
09	0	0	AF	AF	AF	AF
A	3	3	2	2	2	2
B	0	0	0	0	0	0
C	0	0	14	14	14	14
D	38	38	14	14	14	14
E	1	1	1	1	1	1
F	40	40	0	20	19	2F
10	40	40	1	2	1	6
11	0	0	2	0	2	0
12	0	0	2	0	2	0
13	0	0	10	10	10	10

TABLE 1 I2C bus setup SAA7140A(/B)

Subaddress	Bypass Frame Data	Zoom x2 1 Field Data	Scale 1/2 1 Field Data	Scale 1/4 1 Field Data	Scale 1/3 1 Field Data	Icon 1 Field Data
14	0	0	0	41	0	42
15	0	0	0	1	0	7
16	FF	FF	FF	2	FF	0
17	0	0	20	21	20	31
18	0	0	0	0	8	21
19	4	2	4	5	5	4
1A	0	0	0	0	9A	FC
1B	0	0	0	2	1	2
1C	0	0	0	0	0	0
1D	0	0	0	0	0	0
1E	0	0	0	0	0	0
1F	0	0	0	0	0	0
20	0	0	0	0	0	0
21	0	0	0	0	0	0
22	0	0	0	0	0	0
23	10	10	10	10	10	10
24	1D	1D	1D	1D	1D	1D
25	80	80	80	80	80	80
26	40	40	40	40	40	40
27	40	40	40	40	40	40
28	0	0	12	12	12	12
29	0	0	AF	AF	AF	AF
2A	3	3	2	2	2	2
2B	0	0	0	0	0	0
2C	0	0	14	14	14	14
2D	38	38	14	14	14	14
2E	1	1	1	1	1	1
2F	40	40	0	20	19	2F
30	40	40	1	2	1	6
31	0	0	2	0	2	0
32	0	0	2	0	2	0
33	0	0	10	10	10	10
34	0	0	0	41	0	42
35	0	0	0	1	0	7
36	FF	FF	FF	2	FF	0
37	0	0	20	21	20	31
38	0	0	0	0	8	21
39	4	2	4	5	5	4
3A	0	0	0	0	9A	FC
3B	0	0	0	2	1	2
3C	0	0	0	0	0	0
3D	0	0	0	0	0	0
3E	0	0	0	0	0	0
3F	0	0	0	0	0	0

With the bypass setup all signals are output without processing. The setup Zoom x 2 doubles the horizontal length of the picture, vertical is not processed. The setup Scale 1/2 reduces the horizontal length to 1/2 and does not process the vertical size because only one field is displayed. The setup Scale 1/4 reduces horizontal to 1/4 and vertical to 1/2. The setup Scale 1/3 generates a randomly sized image (approx. 1/3). The setup Icon scales down to a few pixel per line.

6. Control and Demo Software

Two Software packages are available to control the SAA7140A(/B) via I2C bus. The Application and Demo Software does automatic scaling in a given window. The DTV debugger software allows the expert access and manipulate any register of each I2C bus controlled device.

Both packages can operate in parallel if the debugger has been started first. This is very helpful to change the scaling by the application software and read the programmed data back from the SAA7140A(/B) through the debugger.

6.1 Application and Demo Software

The application and demo software with documentation is available on request.

6.2 DTV Debugger Software

The installation of the DTV Debugger Software is described in its own user manual (available on request).

Some setupfiles are added to this software package.