TEKTRONIX®

7B92
DUAL TIME BASE

CIRCUIT DESCRIPTION SUPPLEMENT

INSTRUCTION MANUAL

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NOTE

Refer to the 7B92 Operators Manual for specifications and complete operating information. Refer to the 7B92 Service Manual for maintenance, calibration, diagrams, and parts replacement information.

CIRCUIT DESCRIPTION

This manual supplement describes the circuitry used in the 7B92 Dual Time Base unit. The description begins with a discussion of the instrument, using the basic block diagram shown on Fig. 1. Next, each circuit is described in detail, using detailed block diagrams when appropriate, to show the relationship between the stages in each major circuit. Detailed schematics of each circuit are located in the Diagrams section at the back of the service manual; refer to these schematics throughout the following circuit description for specific electrical values and relationships.

BLOCK DIAGRAM

The basic block diagram in Fig. 1 shows the basic interconnections between the individual blocks; each block representing a major circuit within the instrument. The numbered diamond in each block refers to the circuit diagram (located at the rear of the service manual) which covers that specific part of the instrument.

Block Diagram Description

The Delaying Sweep Start Comparator is activated by the positive gate from the Main Trigger Generator. The output gate, coupled to the Delaying Sweep Generator, is the same duration as the delaying sweep. This gate is also coupled to the Aux Sweep Gate connector and to Display Mode Switching for Alternate Sweep operation.

The delaying sweep sawtooth signal is generated when the gate from the Delaying Sweep Start Comparator is applied to the Delaying Sweep Generator. The sawtooth duration is determined by the gate duration; the rate of change of the sawtooth is set by Ct and Rt, selected by the TIME/DIV OR DLY TIME switch. The delaying sweep sawtooth signal is coupled to the Horizontal Output Amplifier, the Delaying Sweep Stop Comparator, the Delay Pickoff circuits, and the Delaying Sweep Out connector.

One side of the Delaying Sweep Stop Comparator is driven by the delaying sweep sawtooth signal and the other side is set by the Delaying Sweep Length adjustment. When the sawtooth waveform passes through the setting of the Delaying Sweep Length adjustment the output of the comparator switches to a positive level.

The positive level from the Sweep Stop Comparator initiates the positive HOLDOFF gate. The duration of the HOLDOFF gate is variable, depending on the setting of the TIME/DIV switch. Holdoff timing capacitors are separate from sweep timing capacitors. HOLDOFF is longer for slower sweep rates. Output from the delaying sweep HOLDOFF is coupled to the Main Trigger Generator, the Delayed Trigger Generator, and the Holdoff out connector.

A sweep gate cannot be generated during the HOLDOFF interval. When the HOLDOFF falls, the trigger circuits are reset so that they are ready to receive a trigger signal.

The Lockout Amp processes mainframe logic signals (when operating the mainframe in the alternate or delaying Horizontal Modes) to provide a sweep disable pulse to the Main Trigger Generator.

The Horizontal Output Amplifier provides positioning and amplification of the sawtooth signals. Display Mode Switching works in conjunction with the Horizontal Output to provide NORMAL Sweep, INTEN, DLY'D Sweep and ALT Sweep Display Modes.

The Delay Pickoff circuits produce a delay gate when the delaying sawtooth signal passes through the LEVEL selected by the DELAY TIME MULT dial. The gate ends with the delaying sawtooth signal. The output gate is coupled to the Delayed Trigger Generator.

The Delayed Trigger Generator includes circuitry for selecting delayed sweep mode, delayed trigger mode, delayed trigger source, type of coupling, and the point on the trigger signal where sweep triggering occurs. When the Delayed Trigger LEVEL control is at the RUNS AFTER DLY TIME detent, the output sweep gate is generated as soon as the delay gate signal (from the Delay Pickoff circuits) is applied. When the Delayed Trigger LEVEL is in the DLY'D SWP TRIGGERABLE position, the output trigger is initiated by the next input trigger signal after the delay gate is applied. The delayed sweep trigger is terminated by the $\overline{\text{HOLDOFF}}$ signal. The trigger signal is coupled to the Delayed Sweep Start Comparator.

The Delayed Sweep Start Comparator is activated by the signal from the Delayed Trigger Generator. The output gate coupled to the Delayed Sweep Generator, is the same duration as the delayed sweep. The delayed sweep gate signal is also coupled to the Sweep Gate Generator.

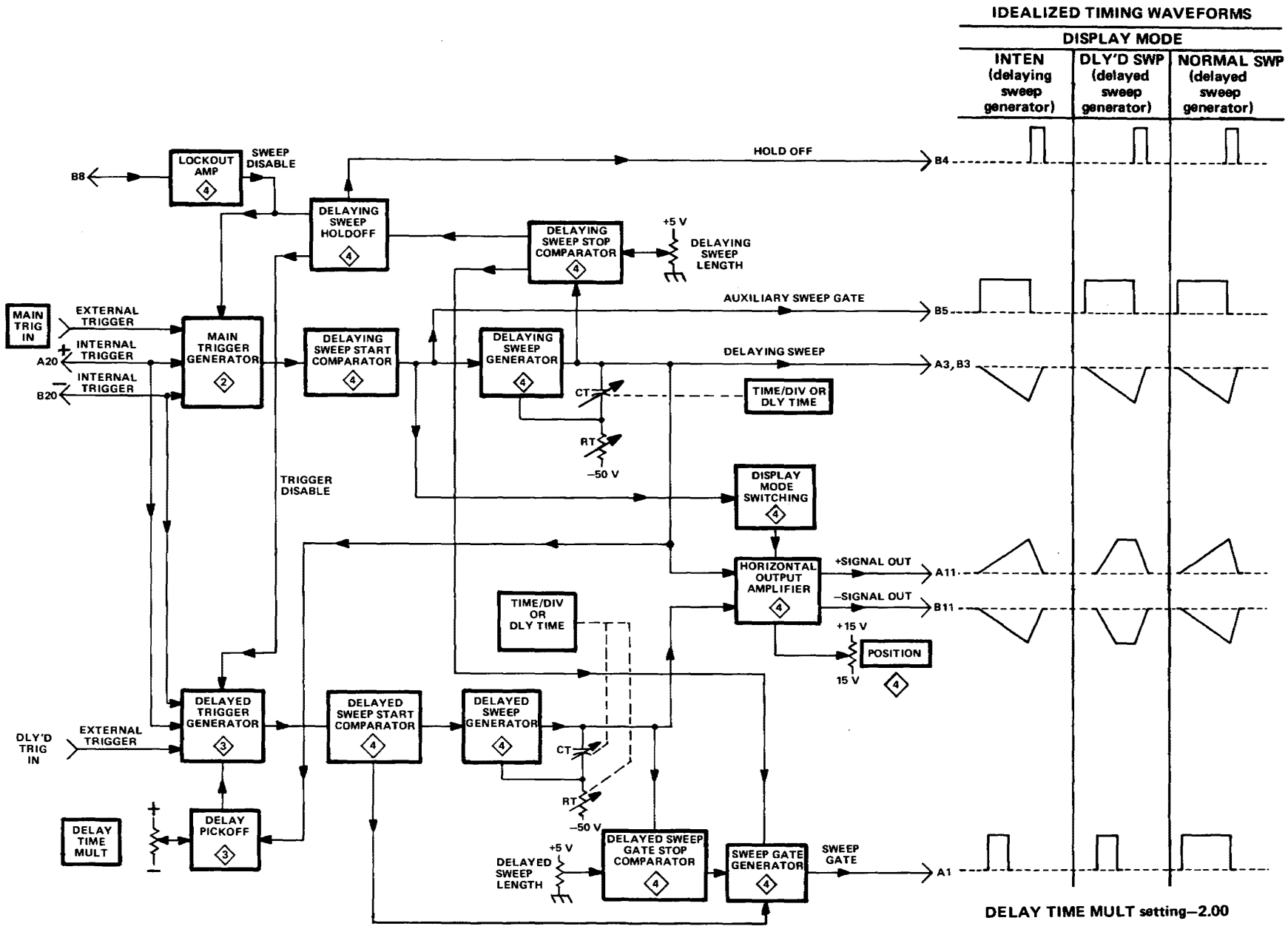


Fig. 1. 7B92 basic block diagram.

The delayed sweep sawtooth signal is developed by the Delayed Sweep Generator. The sawtooth is generated during the time that a gate is applied from the Delayed Sweep Start Comparator. Rate of change of the sawtooth is set by Ct and Rt, selected by the DLY'D TIME/DIV switch. The delayed sawtooth output is coupled to the Horizontal Output Amplifier and the Delayed Sweep Stop Comparator.

One side of the Delayed Sweep Gate Stop Comparator is driven by the delaying sweep sawtooth signal; the other side is set by the Delayed Sweep Length Adjustment. When the delayed sawtooth waveform passes through the voltage set by the Delayed Sweep Length Adjustment, the comparator switches to a positive level. This positive level is coupled to the Sweep Gate Generator.

The Sweep Gate Generator produces an unblanking pulse for the associated oscilloscope. The Sweep Gate pulse is initiated by the gate from the Delayed Sweep Start Comparator and terminated by the pulse from the Delaying Sweep Stop Comparator or Delayed Sweep Gate Stop Comparator (whichever occurs first).

CIRCUIT OPERATION

This section provides a detailed description of the electrical operation and relationship of the circuits in the 7B92. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits refer to the following textbooks.

Tektronix Circuit Concepts Books (order from your local Tektronix Field Office or representatives).

Horizontal Amplifier Circuits, Tektronix Part No. 062-1144-00.

Oscilloscope Trigger Circuits, Tektronix Part No. 062-1056-00.

Sweep Generator Circuits, Tektronix Part No. 062-1098-01.

Phillip Cutler, "Semiconductor Circuit Analysis", McGraw-Hill, New York, 1964.

Lloyd P. Hunter (Ed), "Handbook of Semiconductor Electronics", second edition, McGraw-Hill, New York, 1962.

Jacob Millman and Herbert Taub, "Pulse Digital and Switching Waveforms", McGraw-Hill, New York, 1965.

The following circuit analysis is written around the detailed block diagrams which are given for each major circuit. These detailed block diagrams give the names of the individual stages within major circuits and show how they are connected together to form the major circuit. The block diagrams also show the inputs and outputs for each circuit and the relationship of the front-panel controls to the individual stages. The circuit diagrams from which the detailed block diagrams are derived are shown in the Diagrams section at the rear of the service manual.

MAIN TRIGGER 2

The Main Trigger circuit block includes circuitry for selecting trigger signal source, type of coupling, trigger mode, and the point on the trigger signal where sweep triggering occurs. Also, regardless of the trigger signal shape or amplitude (within specification), the main trigger circuits provide a fast-rise uniform amplitude gate pulse to the Delaying Sweep Start Comparator. Termination of the gate pulse occurs at the rise of delaying sweep HOLDOFF. Figure 2 shows a detailed block diagram of the main Trigger circuits and the schematic is shown on diagram 2 at the rear of the service manual. Refer to diagram 1 at the rear of the service manual for front-panel switching detail.

Trigger Inputs

The Main Trigger circuit block accepts trigger signals from one of three sources; 1. An external signal applied to the MAIN TRIG IN connector. 2. An internal signal from the vertical plug-in unit installed in the oscilloscope system. 3. An internal signal from a sample of the line voltage applied to the oscilloscope system. Separate amplifiers and trigger level comparators are provided for each trigger input. The internal, external, and line trigger signals are coupled to Summing Amplifier and Slope Comparator U660 (see Fig. 2).

External Trigger Amplifier. When the MAIN TRIGGERING SOURCE switch is set to EXT or EXT ÷ 10, the triggering signal is obtained from an external signal applied to the MAIN TRIG IN connector. Both high-frequency and low-frequency inputs are provided to External Trigger Amplifier U620. Separate input paths allow each circuit to be compensated for the appropriate frequency range. Input paths are determined by high-pass and low-pass filters.

The high-frequency input is from the MAIN TRIG IN connector, through R55, to pins 14 and 3 of U620. A high-pass filter consisting of R55 and C59 (EXT SOURCE); or R55, C57, and R58 (EXT ÷ 10 SOURCE) accepts external trigger signals above approximately 80 MHz.

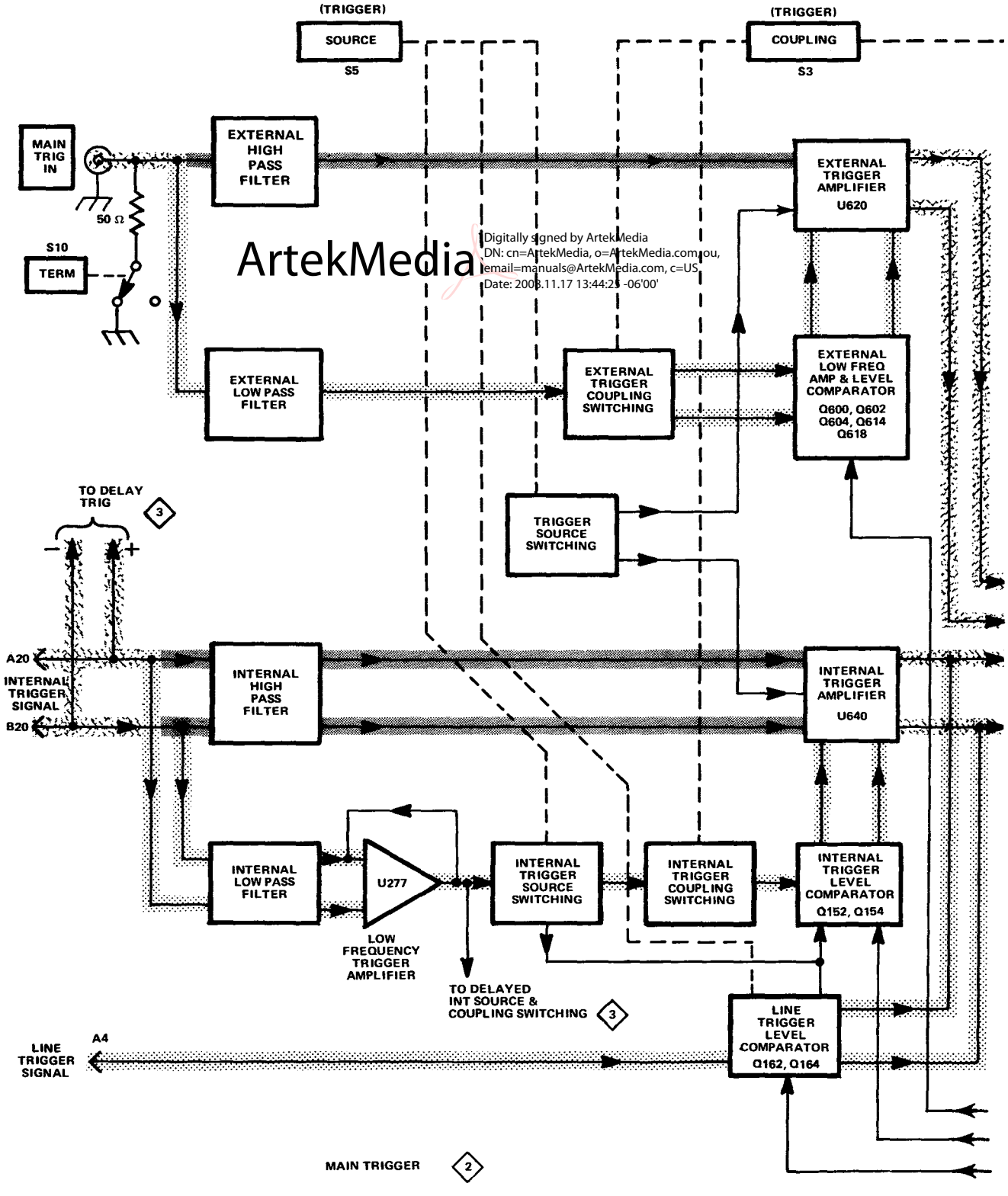


Fig. 2. Main Trigger detailed block diagram.

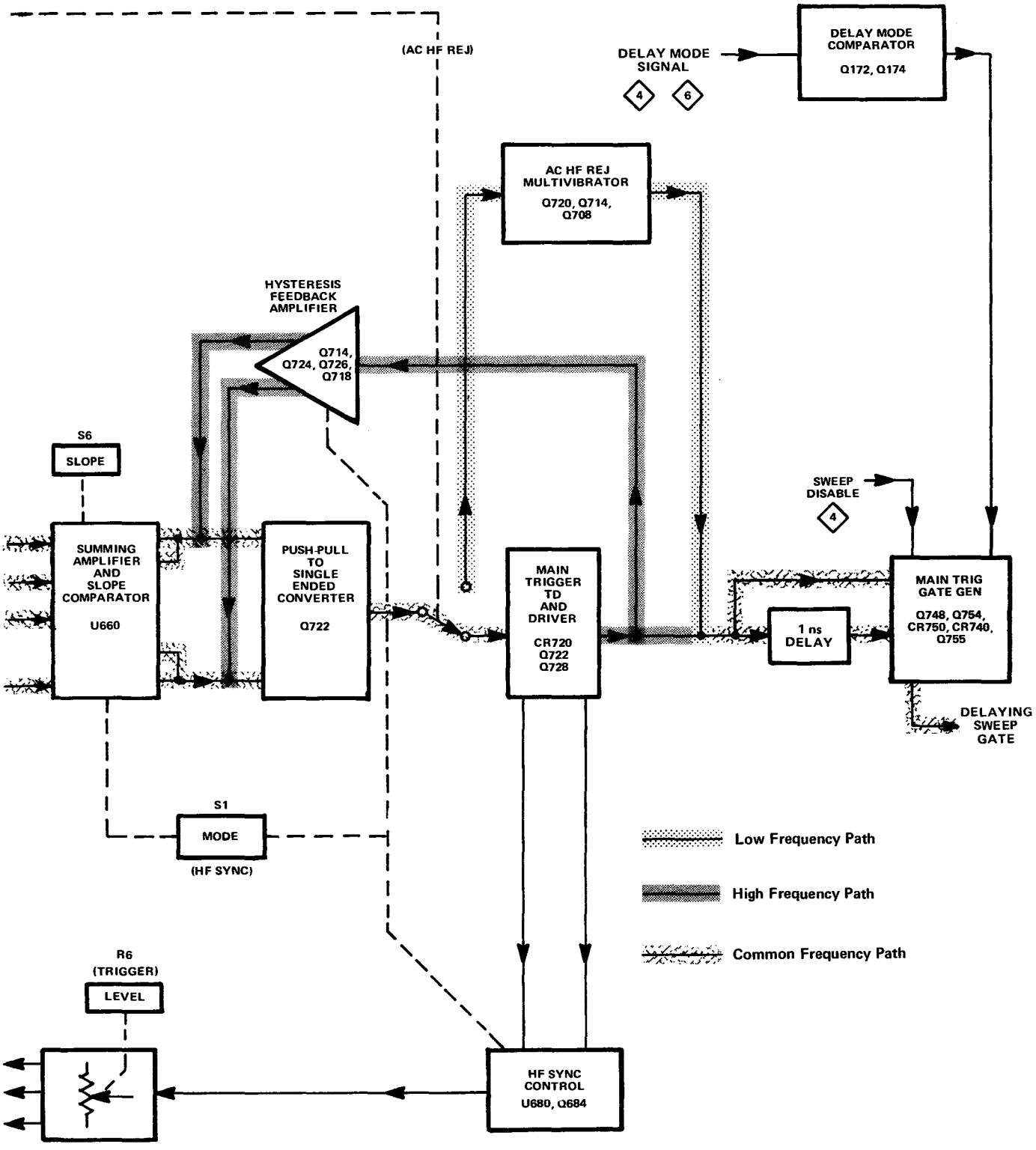

(AC HF REJ)
DELAY MODE SIGNAL
4
6
DELAY MODE COMPARATOR
Q172, Q174
AC HF REJ MULTIVIBRATOR
Q720, Q714, Q708
HYSTERESIS FEEDBACK AMPLIFIER
Q714, Q724, Q726, Q718
S6
SLOPE
SUMMING AMPLIFIER AND SLOPE COMPARATOR
U660
PUSH-PULL TO SINGLE ENDED CONVERTER
Q722
MAIN TRIGGER TD AND DRIVER
CR720 Q722 Q728
SWEEP DISABLE
4
1 ns DELAY
MAIN TRIG GATE GEN
Q748, Q754, CR750, CR740, Q755
DELAYING SWEEP GATE
S1
MODE
(HF SYNC)
R6
(TRIGGER)
LEVEL
HF SYNC CONTROL
U680, Q684
Low Frequency Path
High Frequency Path
Common Frequency Path

Fig. 2. (cont)

The low-frequency external input is through Q600, Q602, Q604, and Q618 into pins 2, 5, 12, and 15 of U620. A low-pass filter, consisting of R60 and stray capacitance, accepts external trigger signals below approximately 80 MHz.

Q600A is a source follower stage with constant current supplied through Q600B. Q602 and Q604 are connected as a differential comparator for the external trigger input. LEVEL control R6 sets the reference voltage for the comparator (trigger level) into the base of Q604. DC Ext Center, R603, varies the level at the emitters of Q602 and Q604 so that the sweep is triggered at the same point on the internal and external trigger signals. Q614 and Q618 provide preamplification of the low frequency signal after trigger level comparison. The low-frequency signal is coupled into pins 2, 5, 12, and 15 of U620.

External Trigger Coupling (AC, AC LF REJ, DC). When the MAIN TRIGGERING COUPLING switch is set to DC, C3 is shorted. The external trigger signal path is through R606, divider R607 and R608, and into source follower Q600A.

In AC LF REJ COUPLING, the trigger signal path through R606 etc., is opened and the external triggering path is coupled through compensating network C62, C63, and R63 into source follower Q600A. At frequencies below about 30 kilohertz, the signal path through C62 and C63 is blocked and the triggering signal is coupled through R3 to ground. In AC LF REJ, R65 and R3 provide the 1 MΩ input impedance.

In AC COUPLING, the DC, AC LF REJ, and AC HF REJ switches are canceled. The trigger signal path is through C3, R606, and R607 to source follower Q600A.

When the external trigger signal frequency is above approximately 80 MHz, all signals are AC coupled through C57 or C59 (high frequency path) to pins 3 and 14 of U620 regardless of COUPLING switch position. The low-frequency and dc components (depending upon COUPLING switch position) of the high-frequency trigger signal are coupled through the external low-frequency path into pins 2, 5, 12, and 15 of U620.

TERM Switch. The TERM switch (S10) selects 50 Ω or 1 MΩ input for both the high and low-frequency external inputs. The 50 Ω input consists of R50 in parallel with R52; and the 1 MΩ input consists of R56, R606, R607, and R608 in series.

Internal Trigger Amplifier. When the MAIN TRIGGERING SOURCE switch is set to INT, the triggering signal is obtained from the vertical plug-in unit installed in the oscilloscope system. The internal trigger signal is coupled to the 7B92 through interface connector pins A20 and B20. Both high-frequency and low-frequency inputs are provided to Internal Amplifier U640. Separate high and low frequency paths allow each circuit to be compensated for the appropriate frequency range. Input paths are determined by high-pass and low-pass filters.

The high-frequency internal trigger input is from interface connector pins A20 and B20 into pins 3 and 14 (push-pull) of Internal Amplifier U640. A high pass filter, consisting of C658 and R642 for the positive input and C654 and R637 for the negative input, accepts internal trigger signals above approximately 16 kHz. The high frequency push-pull signal is also coupled to the delayed trigger circuits.

The low-frequency internal trigger input is push-pull through R650 and R652 into U277, Q152, Q154, and pins 2 and 15 of Internal Amplifier U640. Internal DC Center Adjustment, R647, sets the quiescent level of U277 so that the sweep is triggered at the same point on the internal trigger signal in both the AC and DC COUPLING switch positions. The output of operational amplifier U277 is coupled to the delayed trigger circuits and to the internal level comparator. The LEVEL control (R6) sets the reference voltage for internal level comparator Q152 and Q154. The output of the comparator is coupled to pins 2 and 15 of Internal Amplifier U640.

Internal Trigger Coupling. In the DC position of the MAIN TRIGGERING COUPLING switch, the internal trigger signal is coupled through DC offset Zener VR1 to the input of the Internal Level Comparator (Q152, Q154). In AC COUPLING the triggering signal is coupled through C150 to the level comparator. In AC LF REJ, both the ac and dc low-frequency paths are opened, thus blocking the low-frequency internal triggering signal.

Line Trigger Amplifier. When the MAIN TRIGGERING SOURCE switch is set to LINE, the triggering signal is obtained from a sample of the line voltage applied to the oscilloscope system. The line triggering signal is coupled through interface connector pin A4 to the input of the Line Trigger Level Comparator (Q162, Q164). The LEVEL control (R6) sets the reference level of the comparator. The output is coupled to pins 13 and 4 of Summing Amplifier and Slope Comparator U660.

Source Switching. The source switching circuits determine whether the Summing Amplifier and Slope comparator (U660) receives the trigger signal from the Internal, External, or Line Amplifiers.

When the MAIN TRIGGERING SOURCE switch is set to EXT ÷ 10, +15 volts is coupled through R630 and CR631, thus forward biasing CR631. Pin 6 of U620 is a diode drop higher than pin 11, which produces an output at pins 7 and 10. Relay K10 is in its non-energized state with both sides of the relay at ground. Relay K600 is energized with one side at 15 volts and the other side at ground. Therefore, the high-frequency path is coupled through C57 and divider network R57 and R58. The low-frequency path is through divider network R608, and R65-R606-R607. Pins 6 and 11 of U620 are coupled to pins 11 and 6 of U640, respectively. Therefore, when External Amplifier U620 is on, Internal Amplifier U640 is off and vice versa.

When the MAIN TRIGGERING SOURCE switch is set to EXT, the EXT ÷ 10 switch is canceled. The EXT switch applies 15 volts to R630, which forward biases CR631. U620 is turned on in the manner described in the preceeding paragraph (EXT ÷ 10 SOURCE). The 15 volts applied by the EXT switch energizes K10 and turns off K600. The high-frequency path is through C59; the low-frequency path is through divider network R65-R606 and R607-R608.

In the INT MAIN TRIGGERING SOURCE, the EXT, EXT ÷ 10, and LINE switches are canceled. The ground potential at the EXT switch turns off relay K10 and reverse biases CR631. Pin 6 of U620 is low with respect to pin 11, which causes an output at pins 8 and 9 into the +5 volt supply. When pin 6 of U620 is low with respect to pin 11, pin 6 of U640 is high with respect to pin 11. This results in an output at pins 7 and 10 of Internal Amplifier U640.

When the MAIN TRIGGERING SOURCE switch is set to LINE, +5 volts is applied directly to pin 11 of Internal Amplifier U640. Pin 6 of U640 is low with respect to pin 11. Therefore, both the internal and external amplifiers have outputs into the +5 volt supply through pins 8 and 9. When the LINE switch is selected, a −15 volts supplies emitter current for the Line Level Comparator (Q162, Q164). The line trigger signal is coupled into pins 4 and 13 of Summing Amplifier and Slope Comparator U660.

Summing Amplifier and Slope Comparator

The internal, external, and line signals are summed into Summing Amplifier and Slope Comparator U660. The trigger signal coupled from U660 to the Push-Pull to Single-Ended Converter is determined by the Source Switching circuits as previously described.

When pin 6 of U660 is high with respect to pin 11, the output is at pins 7 and 10. With the SLOPE switch (S6) set to −, pin 6 is a diode drop higher than pin 11. Therefore, in the − SLOPE, the push-pull output is at pins 7 and 10.

When pin 6 of U660 is low with respect to pin 11, the output is at pins 8 and 9. With the SLOPE switch (S6) set to the +, the 15 volt supply is tied to ground through R660 and R271. Pin 6 is pulled low with respect to the level at pin 11 (the voltage level at pin 11 is set by VR600). Therefore, in the + SLOPE, the push-pull output is at pins 8 and 9.

Trigger Generator

The Push-Pull to Single-Ended Amplifier (Q722) changes the push-pull output of U660 to a single-ended signal at Trigger Driver tunnel diode CR720. Quiescent current for CR720 is supplied by Q728. A feedback loop (consisting of Q714, Q724 and Q718, Q726) is driven push-pull from CR720 to the output of Summing Amplifier U660. The feedback loop acts as a hysteresis reducing network for Trigger Driver tunnel diode CR720. The hysteresis reducing network allows CR720 to trigger on low amplitude trigger signals. Trigger Level Sensitivity adjustment, R730, varies the current feedback into Q722.

HF SYNC Operation. In the HF SYNC MAIN TRIGGERING MODE the cathode of CR271 is grounded. This sets the level at pin 6 of U660 low with respect to pin 11. This forces a positive slope output at pins 8 and 9 of U660. The ground level is also coupled to the base of Q684. Q684 turns on and CR684 is forward biased, which connects U680 into a feedback loop. The ground level, initiated by the HF SYNC switch, pulls down on the emitters of Q724 and Q726, which supplies more current for Q722. The additional current through Q722 turns on CR720 in a free-running mode. The LEVEL control (R6) adjusts the effective frequency of the free-running tunnel diode (CR720) to synchronize with the subharmonic of the triggering signal frequency. Feedback amplifier U680 offsets the trigger LEVEL voltage to maintain a balance of push-pull current output from Trigger Summing Amplifier and Slope Comparator U660.

AC HF REJ. In AC HF REJ COUPLING the Trigger Driver Tunnel Diode, Hysteresis Feedback Amplifier, and HF SYNC Control circuits are disabled by removing the ground potential from current source Q728. A ground potential, initiated by the AC HF REJ switch, supplies emitter current for a Schmitt mulitvibrator (Q608, Q604). In AC HF REJ, collector current for the Push-Pull to Single-Ended Converter (Q722 is through L714 and R714. The push-pull trigger signal is coupled through Q722 and a low-pass filter network (C710, R711, C712, and R712) to gate the Schmitt multivibrator. The output of the multivibrator is through source follower Q702 into the Sweep Gate Generator.

Sweep Gate Generator

The Sweep Gate Generator produces a positive-going gate pulse to enable the main sweep generator. During main

sweep HOLDOFF the sweep disable pulse at pin C is high. This level is seen at the emitter of source follower Q755. The high level saturates Q754 and Q748. The saturated condition of Q754 and Q748 takes the current from tunnel diodes CR740 and CR750, which keeps them in the low state. At the end of HOLDOFF, the level at pin C drops to the low state. The low level is seen at the emitters of Q754 and Q748. Both transistors turn off, which allows the current to flow through CR740 and CR750, thereby arming both tunnel diodes. Upon the initiation of a trigger pulse, Q744 turns on, which supplies additional current and switches CR740 to its high state. One nanosecond later, the trigger signal is seen at the anode of the Sweep Gate tunnel diode CR750. CR750 turns on, and a sweep gate is coupled to the Main Sweep Generator. Trigger jitter is reduced by arming CR750 before the arrival of a trigger signal. At the end of sweep, the level at pin C rises to its high state. The high level is seen at the emitters and therefore the bases of Q754 and Q748. Q748 and Q754 saturate, taking the current from CR740 and CR750, which switches them to the low state.

Delay Mode Comparator

The Delay Mode Comparator (Q172, Q174) is functional only when the 7B92 is operating as a delayed sweep unit in the B Horizontal compartment of an oscilloscope with two horizontal compartments. When the 7B92 is operating in the Independent or Triggerable After Delay modes (as determined by the Delaying Sweep unit in the A Horizontal compartment), Q172 is on and Q174 is off. Therefore, the circuit has no effect on the Main Trigger circuits. When the 7B92 is operating in the Runs After Delay Time Mode (as determined by the Delaying Sweep unit in the A Horizontal compartment), a high level is seen at the base of Q172. Q172 turns off and Q174 turns on. Q174 supplies sufficient current to switch CR740 and CR750 to the high state in the absence of a sweep disable pulse at pin C.

DELAY PICKOFF AND DELAYED TRIGGER

The Delayed Trigger circuit block includes circuitry for selecting trigger signal source, type of coupling, trigger mode, and the point on the trigger signal where sweep triggering occurs. Also, regardless of the trigger signal shape or amplitude (within specification), the delayed trigger circuits provide a fast-rise, uniform amplitude gate pulse to the delayed sweep comparator. Termination of the gate pulse occurs at the rise of sweep holdoff. Fig. 3 shows a detailed block diagram of the Trigger circuits and the schematic is shown on diagram 3 at the rear of the service manual. Refer to diagram 1 at the rear of the service manual for front-panel switching detail.

Trigger Inputs

The Delayed Trigger circuit block accepts trigger signals from an external signal applied to the DLY'D TRIG IN connector or an internal signal from the vertical plug-in unit installed in the oscilloscope system. Separate amplifiers and trigger level comparators are provided for each trigger input. The internal and external trigger signals are coupled to Summing Amplifier and Slope Comparator U860 (see Fig. 3).

External Trigger Amplifier. When the Delayed Triggering SOURCE switch is set to EXT, the triggering signal is obtained from an external signal applied to the DLY'D TRIG IN connector. Both high-frequency and low-frequency inputs are provided to External Trigger Amplifier U820. Separate input paths allow each circuit to be optimized over the appropriate frequency range. Input paths are determined by high-pass and low-pass filters.

The high-frequency input is from the DLY'D TRIG IN connector, through R86, to pin 14 of U820. A high-pass filter consisting of R86 and C86 accepts external trigger signals above approximately 80 MHz.

The low-frequency external input is through Q800, Q802, Q804, Q814, and Q818 into pins 2, 5, 12, and 15 of U820. A low-pass filter, consisting of R71 and stray capacitance, accepts external trigger signals below approximately 80 MHz.

Q800A is a source follower stage with constant current supplied through Q800B. Q802 and Q804 are connected as a differential level comparator for the external trigger input. The LEVEL control R4, sets the reference voltage for the comparator (trigger level) into the base of Q804. DC Ext Center, R802, varies the level at the emitters of Q802 and Q804 so that the sweep is triggered at the same point on the internal and external trigger signals. Q814 and Q818 provide preamplification of the low frequency signal after trigger level comparision. The low-frequency signal is coupled into pins 2, 5, 12, and 15 of U820.

External Trigger Coupling. When the Delayed Triggering COUPLING switch is set to DC, the external trigger signal path is through R71, R73, R75, and R76 into Source Follower Q800A. In AC COUPLING, the DC switch is opened. The AC path is through R71, R78, C78, and C79 into Source Follower Q800A.

When the external trigger signal frequency is above approximately 80 MHz, all signals are AC coupled through C86 (high frequency path) to pins 3 and 14 of U820, regardless of COUPLING switch position. The low-frequency and DC components (depending upon COU-

PLING switch position) of the high-frequency trigger signal are coupled through the external low-frequency path into pins 2, 5, 12, and 15 of U820.

TERM Switch. The TERM switch selects 50 Ω or 1 MΩ input for both the high and low-frequency external inputs. The 50 Ω input consists of R81 in parallel with R82; the 1 MΩ input consists of R73, R75, R76, and R807 in series.

Internal Trigger Amplifier. When the Delayed Triggering SOURCE switch is set to INT, the triggering signal is obtained from the vertical plug-in unit installed in the oscilloscope system. The internal trigger signal is coupled to the 7B92 through interface connector pins A20 and B20. Both high-frequency and low-frequency inputs are provided to Internal Amplifier U840. Separate high and low frequency paths allow each circuit to be compensated for the appropriate frequency range. Input paths are determined by high-pass and low-pass filters.

The high-frequency internal trigger input is from interface connector pins A20 and B20 into pins 3 and 14 (push-pull) of Internal Amplifier U840. A high pass filter, consisting of C848 and R841 for the positive input and C838 and R836 for the negative input, accepts internal trigger signals above approximately 16 kHz.

The low-frequency internal trigger input is from the Main Trigger Internal Low Pass Filter and Low Frequency Trigger amplifier, through the Delayed Trigger Source and Coupling circuits, and into the Internal Level Comparator. The LEVEL control (R4) sets the reference voltage for internal level comparator Q182 and Q184. The output of the comparator is coupled to pins 2 and 15 of Internal Amplifier U840.

Internal Trigger Coupling. In the DC position of the Delayed Triggering COUPLING switch, the internal trigger signal is coupled through DC offset Zener VR 2 to the input of the Internal Level Comparator (Q182, Q184). In AC COUPLING, the triggering signal is coupled through C9 to the level comparator.

When the Delayed Triggering SOURCE switch (S11) is set to EXT, +5 volts is coupled to R821, which forward biases CR824. Pin 6 of U820 is a diode drop higher than pin 11, which produces an output at pins 7 and 10. Pins 6 and 11 of U820 are coupled to pins 11 and 6 of U840 respectively. Therefore, when External Amplifier U820 is on, Internal Amplifier U840 is off, and vice versa.

When the Delayed Triggering SOURCE switch is set to INT, the low-frequency internal trigger signal is coupled from the Main Trigger circuits to the Delayed Trigger Source and Coupling circuits. Also, R821 is tied to ground, which sets pin 6 of U820 negative with respect to pin 11. Therefore, the output of U820 is at pins 8 and 9 into the +5 volt supply. CR827 is reversed biased, which makes pin 6 of Internal Amplifier U840 high with respect to pin 11. Thus, the output of U840 is at pins 7 and 10 into pins 13 and 4 of U860.

Summing Amplifier and Slope Comparator

The internal and external signals are summed into Summing Amplifier and Slope Comparator U860. The trigger signal, coupled from U860 to the Push-Pull to Single-Ended Converter, is determined by the Source Switching circuits.

When pin 6 of U860 is low with respect to pin 11, the output is at pins 8 and 9. With the SLOPE Switch (S4) set to +, pin 6 is a diode drop lower than pin 11. Therefore, in the + SLOPE, the push-pull output is at pins 8 and 9.

When pin 6 of U860 is positive with respect to pin 11, the output is at pins 7 and 10. With the SLOPE switch (S4) set to −, +15 volts supplies the current to turn on Q188. The collector of Q188 pulls down the anode of CR861. Pin 11 is pulled low with respect to pin 6. Therefore, in the − SLOPE, the push-pull output is at pins 7 and 10.

Trigger Generator

The Push-Pull to Single Ended Amplifier (Q922) changes the push-pull output of U860 to a single-ended signal at Trigger Driver tunnel diode CR920. A feedback loop (consisting of Q914, Q934 and Q918, Q932) is driven push-pull from CR920 to the output of Summing Amplifier U860. The feedback loop acts as a hysteresis reducing network for Trigger Driver tunnel diode CR920. The hysteresis reducing network allows CR920 to trigger on low amplitude trigger signals. Trigger Level Sensitivity adjustment, R920, varies the current feedback into Q922.

HF SYNC Operation. The HF SYNC Delayed Triggering Mode is initiated when the Delayed Triggering LEVEL control (R4) is set lower than the base of Q194. Q194 and Q192 turn on and CR883 is forward biased so that U880 is connected into a feedback loop. Q188 is turned off, forcing U860 into positive slope operation. The base of Q192 pulls down on the emitters of Q932 and Q934 which supplies more current for Q922. The additional current through Q922 turns on CR920 in a free-running condition. The LEVEL control (R4) adjusts the effective frequency of the free-running tunnel diode (CR920) to synchronize with the subharmonic of the triggering signal frequency. Feedback amplifier, U880, offsets the trigger LEVEL voltage to maintain a balance of the push-pull current output from Trigger Summing Amplifier and Slope Comparator U860.

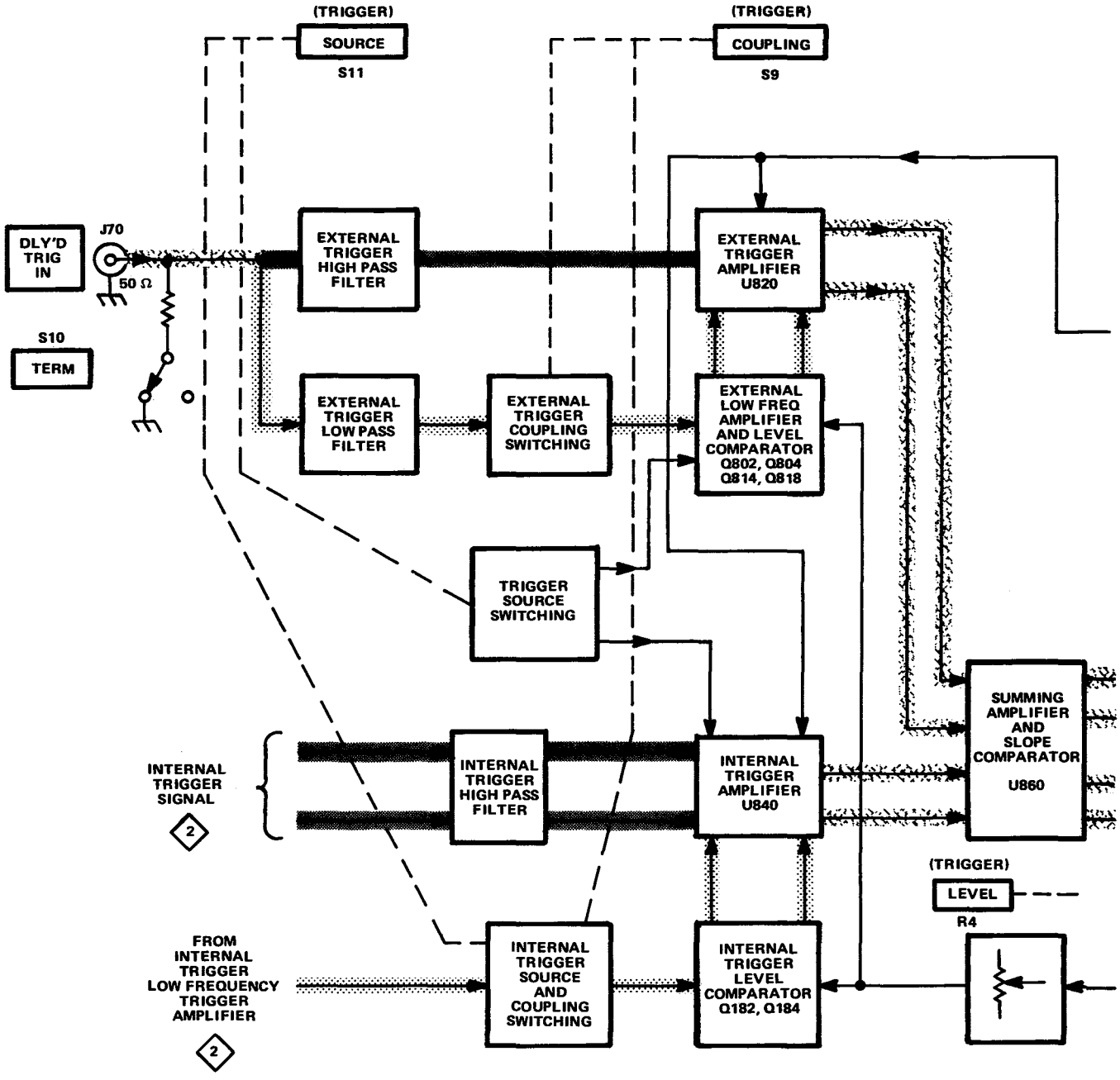
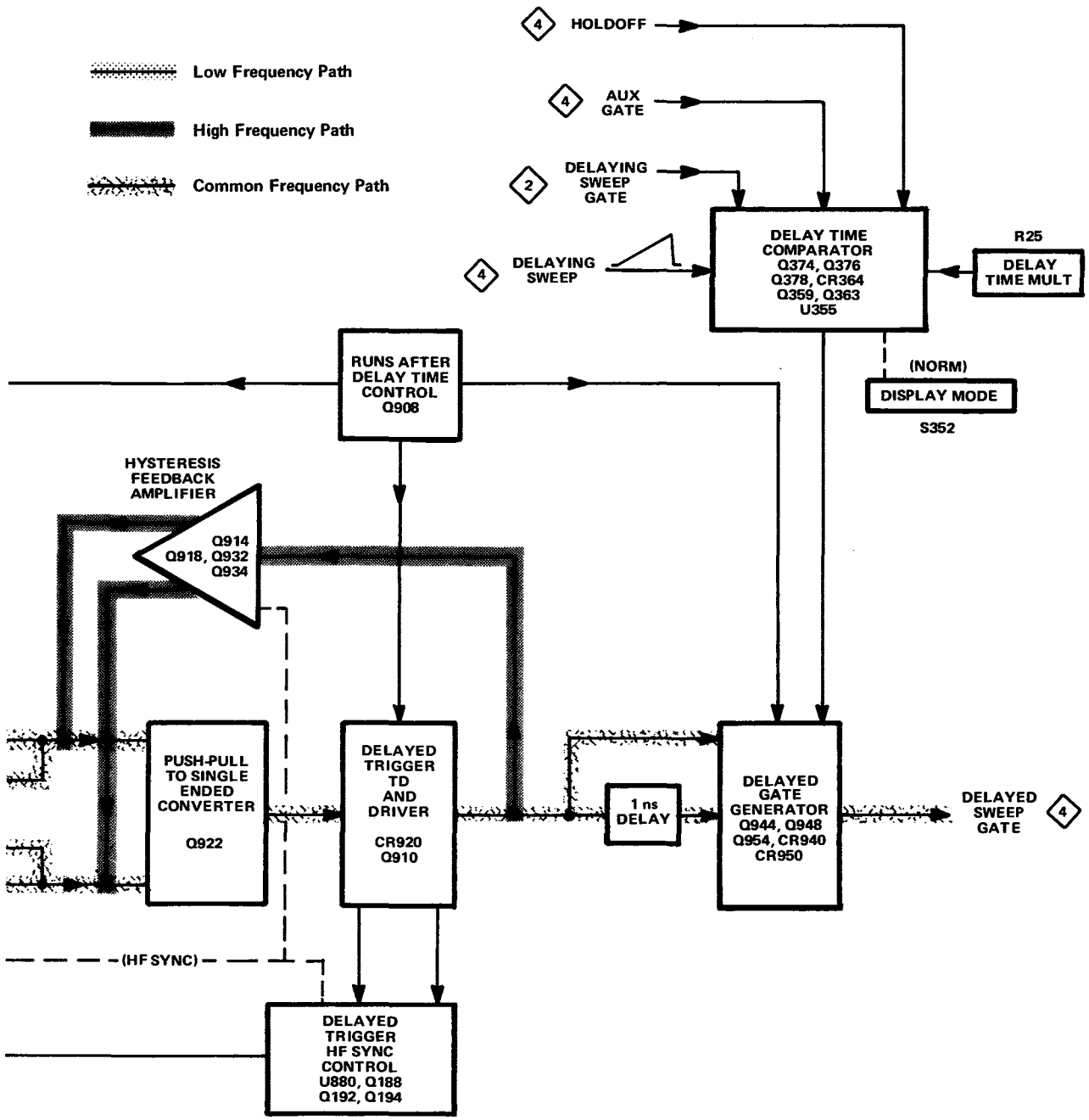


Fig. 3. Delay Pickoff and Delayed Trigger detailed block diagram.



DELAY PICKOFF and DELAYED TRIGGER 3

Fig. 3. (cont)

Delay Time Comparator

The delay time comparator circuit prevents the delayed sweep gate generator from producing a gate pulse until after the delay time is determined by the DELAY TIME MULT dial. Q359A and Q359B compose the comparator; the level at Q359B is set by the delaying sweep, and the level at Q359A is set by the DELAY TIME MULT dial.

Q376 is the current source for delay time gate tunnel diode CR364. S352 initiates the NORMAL SWP Display Mode by setting the input of impedance converter U355 to ground, thereby setting the comparator delay time to zero. At delay time comparison (delaying mode), CR364 generates a delay time gate pulse to the delayed sweep gate generator.

Delayed Sweep Gate Generator

The Sweep Gate Generator produces a positive-going gate pulse to enable the Delayed Sweep Generator. The Delayed Sweep Gate Generator will operate in either the RUNS AFTER DLY TIME or TRIGGERABLE AFTER DLY TIME modes.

In the RUNS AFTER DLY TIME mode, S4 supplies +5 volts to the base of Q948. Q948 saturates and takes the current from CR940, thereby keeping CR940 from accepting a trigger signal.

The +5 volts at S4 also supplies dc current through R957 and R959 to arm CR950 so that a delay time gate pulse will switch CR950 to its high state. At delay time comparison, CR364 generates a positive-going delay time gate pulse that pulls up on CR950. CR950 switches to its high state and couples a delayed sweep gate pulse to the delayed sweep start comparator.

In the DLY'D SWP TRIGGERABLE mode, the +5 volt supply is removed from Q948 and also from R957 and R959. In the absence of a HOLDOFF pulse, Q954 turns off, which allows the current to flow through CR750, thereby arming the tunnel diode. Before delay time comparison, Q948 is turned on by a high level coupled from Q378. Q948 takes the current from CR940, ensuring that CR940 will not accept a trigger pulse. At delay time comparision, the level at the collector of Q378 falls. Q948 turns off, which allows the current to arm CR940. Simultaneously, the delay time gate from CR364 rises and further arms CR950. Upon the initiation of a trigger pulse, Q944 turns on and supplies additional current to switch CR940 to its high state. Approximately one nanosecond later, the trigger signal is seen at the anode of the Sweep Gate tunnel diode CR950. CR950 turns on and a sweep gate is coupled to the Delayed Sweep Start Comparator. At the end of sweep, the HOLDOFF pulse (through Q374) switches tunnel diode CR364 to its low level. The HOLDOFF saturates Q954 and the delayed sweep gate falls.

DELAYING SWEEP GENERATOR 4

The Delaying Sweep Generator circuit produces a sawtooth voltage that is amplified by the Horizontal Amplifier circuits to provide horizontal deflection on the crt of the oscilloscope. This output signal is generated on command (sweep gate pulse) from the main trigger generator. The delaying sweep generator signal is displayed on the oscilloscope only when the 7B92 is operating in the INTEN and ALT display modes. The delaying sweep generator also provides calibrated delay time when operating in a delaying sweep display mode. Fig. 4 shows a detailed block diagram of the Delaying Sweep Generator and the schematic is shown on Diagram 4 at the rear of the service manual. Refer to diagram 1 at the rear of the service manaul for front-panel switching detail. The following circuit description is given with the MAIN TRIGGERING MODE switch set to NORM, except as otherwise stated.

Sweep Start Generator

Q322 and Q326 compose the Delaying sweep Start Comparator. In the NORM MAIN TRIGGERING MODE, pin 3 of U310 is quiescently high. Q326 is on and Q322 is high which inhibits the sweep. When the Main Trigger Generator supplies a sweep gate pulse, the positive transition is coupled to the base of Q322. The base of Q322 rises above the level at the base of Q326 and the current through common emitter resistor R324 is diverted from Q326 to Q322. Q322 turns on. The low at its collector turns off the sweep clamp circuit (Q395, Q398) and allows the sweep to run.

Auxiliary Sweep Gate

The Auxiliary Sweep Gate signal is amplified by Q330 and coupled to Interface connector pin B5. The Auxiliary Sweep Gate corresponds to the sweep that is not being sent to the oscilloscope.

Sawtooth Generator

Q402, Q404, Q406, and Q408 constitute a Miller Integrator and Q395 and Q398 compose the Sweep Clamp circuit. Timing components, Ct and Rt determine the rate of change of the sawtooth waveform. The Miller Integrator produces a linear positive-going sawtooth signal.

When the collector of Q322 (Delaying Sweep Start Comparator output) is high, Q395 and Q398 (Sweep Clamp circuit) turn on. The output of the Miller Integrator is shorted to the input, and the sweep is inhibited. A low at the output of the Delaying Sweep Start comparator turns

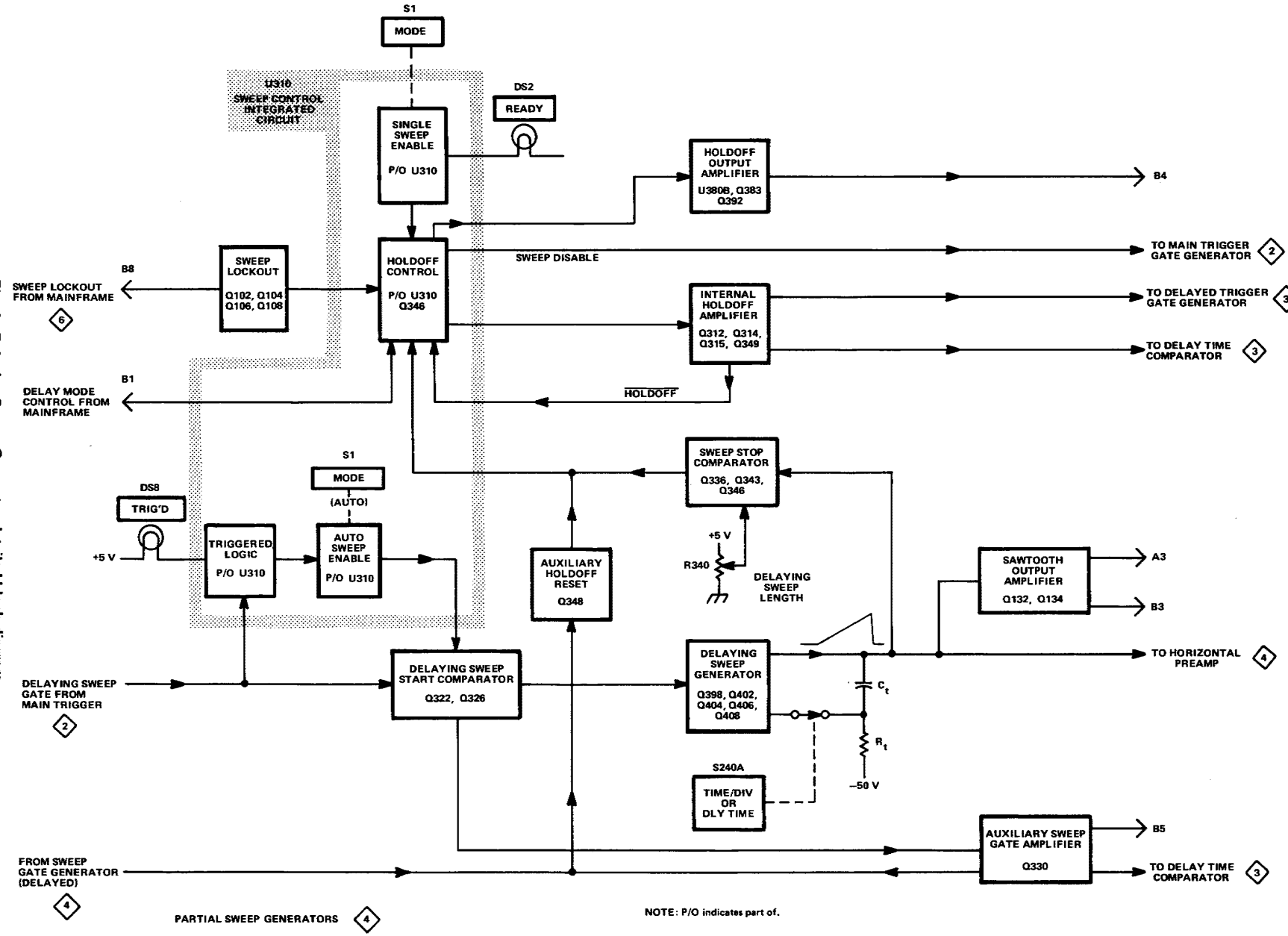


Fig. 4. Delaying Sweep Generator detailed block diagram.

off Q395 and Q398 and allows the sawtooth generator to run. At termination of the delaying sweep gate, the Sweep Start Comparator switches. Q395 and Q398 turn on and terminate the sweep.

Sawtooth Output Amplifier

The delaying sawtooth signal is inverted by Q134 and coupled through emitter follower Q132 to Interface connector pins A3 and B3 for composite use in the oscilloscope.

Sweep Stop Comparator

The Delaying Sweep Stop Comparator consists of Q336, Q343, and Q346. In the absence of a sawtooth signal at the emitter of Q408, Q336 is conducting and Q343 is held off by the positive level set at its base by Delaying Sweep Length adjustment R340. When the sawtooth voltage at the emitter of Q408 raises the base of Q336 higher than the base of Q343, Q336 turns off and Q343 turns on. The collector of Q343 rises; this positive step is coupled through emitter follower Q346 to pin 16 of U310, beginning sweep HOLDOFF.

Holdoff Circuit

The Holdoff Circuit consists of pins 8, 10, 16, and 17 of U310 plus R and C time constants selected by the TIME/DIV switch. The Holdoff circuits prevent retriggering the sweep generator until after the sweep timing capacitor has discharged and the sweep circuits are again ready to generate a sweep.

At the end of the sawtooth waveform, a positive step is coupled to pin 16 of U310 by way of the Sweep Stop Comparator as previously described. The positive pulse seen at pin 16 of U310 is coupled internally through U310 to pin 17 and in turn to Q755 in the Main Trigger Generator. The Main Trigger Generator is reset and the delaying sweep gate pulse at pin D goes low. As a result, Q322 turns off and Q326 turns on. The high level at the collector of Q322 is coupled to the sweep clamp circuit, thus ending the sweep.

After a time determined by the timing components at pin 8, internal circuitry within U310 switches pin 17 to its low state, ending the HOLDOFF gate. The Main Trigger Generator is released to generate a delaying sweep gate pulse.

A negative gate ($\overline{\text{HOLDOFF}}$), coincident with the positive HOLDOFF gate, appears at pin 10 of U310. The negative gate is coupled to the Internal Holdoff Amplifier and Holdoff Output Amplifier where it is processed for composite HOLDOFF functions. Refer to the Horizontal Preamplifier and Display Mode Switching for HOLDOFF functions in the ALT Sweep Display Mode.

TRIG'D Lamp Driver

When the delaying sweep gate is high and the sweep is running, the TRIG'D lamp is on. At all other times the lamp is off.

Delay Mode Control

When the 7B92 is installed in the B Horizontal compartment of an oscilloscope with two horizontal compartments, the Delay Mode Control determines whether the 7B92 operates as in independent time base, a delayed sweep unit in the Runs After Delay Time Mode, or as a delayed sweep unit in the triggerable after Delay Time Mode. When a high level is present at Interface connector B1 (and therefore pin 13 of U310), the Auto Circuit (see Auto Triggering in this section) is disabled. Only a trigger pulse to the Sweep Start Comparator can enable a sweep. During delay time, as determined by the settings of the delaying sweep unit in the A Horizontal compartment, sweep lockout (see lockout discussion in this section) inhibits the sweep. After delay time, the 7B92 can be triggered. A low level, at pin 13 of U310 enables the Auto Circuit, causing the 7B92 to operate as an independent time base.

Auto Triggering Mode

Operation of the Delaying Sweep Generator circuit in the AUTO MAIN TRIGGERING MODE is the same as for NORM MAIN TRIGGERING MODE, just described, when a trigger pulse is applied. However, when a trigger pulse is not present, a free-running reference trace is produced in the AUTO MODE. This occurs as follows:

The Auto Triggering circuit consists of pins 1, 3, 6, and 19 of U310. When the AUTO MODE is selected, a low at pin 19 of U310 enables the Auto Circuit. When a repetitive trigger signal above 30 Hertz and of adequate amplitude is applied to the Main Sweep Start Comparator and pin 1 of U310, the internal Auto Multi at pin 6 of U310 charges towards five volts through R300 and C300, but is discharged by each incoming trigger pulse.

In the absence of a trigger pulse, C300 charges towards +6 volts, switching pin 6 to high state and pin 3 to its low state. Q326 turns off and Q322 turns on. The low level at the emitter of Q395 turns off the Sweep Clamp circuit and allows the sweep to run.

Single Sweep Operation

Operation of the Delaying Sweep Generator in the SINGLE SWEEP position of the MAIN TRIGGERING

MODE switch is similar to operation in the NORM Mode as previously described. However, after one sweep has run, all other sweeps are inhibited until the RESET button is pressed. A READY lamp is provided to indicate when the sweep is ready to accept a trigger.

The Single Sweep circuit consists of pins 11, 12, 14, 15, and 17 of U310. For SINGLE SWEEP operation, the +5 volt supply is applied to pin 12 of U310. The HOLDOFF pulse at pin 17 of U310 goes positive, preventing generation of a sweep. When the RESET button is pressed, pin 15 is momentarily held to ground, and pin 17 goes low to allow the Main Trigger Generator to accept a trigger. The HOLDOFF line (pin 17 of U310) stays low until a sweep has been completed. At this time, the HOLDOFF pulse rises at pin 17 and stays in the HOLDOFF state until the RESET button is pressed.

When operating in the SINGLE SWEEP MAIN TRIGGERING MODE, the Auxiliary Holdoff Reset circuit (Q348) ensures that the Holdoff circuits (previously described) are reset at the end of each sweep.

Q304 acts as a switch for the READY lamp. When the HOLDOFF gate at pin 17 is high (preventing the sweep generator from accepting a trigger), pin 11 is high and Q304 and the READY lamp are off. When the RESET button is pressed, the HOLDOFF gate at pin 17 goes low and allows the Delaying Sweep Generator to accept a trigger. Pin 11 rises and turns on Q304, which provides current to turn on the READY lamp.

Sweep Lockout

Q102, Q104, Q106, Q108 and pins 3, 16, and 18 of U310 compose the Sweep Lockout circuit. The Sweep Lockout circuit is functional when the 7B92 is installed in the B Horizontal compartment of an oscilloscope which accomodates two horizontal plug-in units, and it is desired to operate in the oscilloscope Alternate Horizontal Mode, or to operate the 7B92 as a delayed sweep unit. LOCKOUT is applied to the 7B92 during the time that the sweep from the associated time base unit is displayed.

The oscilloscope controls inititation of a sweep by supplying current to the base of Q102 when LOCKOUT is required. This current causes a positive step at pin 18 of U310. Pin 3 of U310 steps positive and Q326 turns on. Q322 turns off, which couples a positive level to the Sweep Clamp circuit (Q395, Q398), thus preventing a sweep.

DELAYED SWEEP GENERATOR ◇4◇

The Delayed Sweep Generator produces a sawtooth voltage that is amplified by the Horizontal Amplifier circuits to provide a delayed sweep crt display. The sawtooth output voltage is generated on command from the Delayed Trigger Generator. The delayed sweep generator signal is displayed on the oscilloscope only when the 7B92 is operating in the Normal Sweep, DLY'D SWP and ALT Sweep Display Modes. Figure 5 shows a detailed block diagram of the Delayed Sweep Generator and a schematic is shown on diagram 4 at the rear of the service manual. Refer to diagram 1 at the rear of the service manual for front-panel switching detail.

Sweep Start Comparator

Q422 and Q426 compose the Delayed Sweep Start Comparator. Quiescently, in the absence of a trigger pulse, Q422 is off and Q426 is on. The high level at the collector of Q422 turns on the Sweep Clamp circuit (Q432, Q434, and Q440) and inhibits the sweep. When the Delayed Trigger Generator supplies a sweep gate pulse, the positive transition is coupled to the base of Q422. The base of Q422 rises above the level at the base of Q426 and the current through common emitter resistor R422 is diverted from Q426 to Q422. Q422 turns on. The low at its collector turns off the Sweep Clamp circuit (Q432, Q434, and Q440) and allows the sweep to run.

Sawtooth Generator

Q454, Q456, Q450 and Q462 constitute a Miller Integrator. Q432, Q434, and Q440 compose the Sweep Clamp circuit at sweep rates from .2 s/DIV through 50 ns/DIV. Q432, Q434, CR445, and CR446 compose the Sweep Clamp circuit at sweep rates above 50 ns/DIV. Timing components Ct and Rt determine the rate of change of the sawtooth waveform. The Miller Integrator produces a linear positive-going sawtooth signal that is coupled to the horizontal preamplifier.

When operating at sweep rates below 20 ns/DIV, the absence of a sweep gate at the Sweep Start Comparator sets the output of the comparator (collector of Q422) high. Q432 turns off. Q435 and Q440 turn on, thereby shorting the input of the Miller Integrator to the output. The sweep is inhibited. At sweep rates faster than 50 ns, a sweep gate at the Sweep Start Comparator sets the output of the comparator (collector of Q422) low. Q432 turns on. Q434 turns off and reverse-biases CR445 and CR446. The sweep generator is released to produce a sweep. At termination of the sweep gate, from the Delayed Trigger circuits, Q432 turns off, Q434 turns on and forward biases CR445 and CR446. The sweep is terminated.

Sweep Gate Stop Comparator

The Delayed Sweep Gate Stop Comparator consists of Q468, Q472, and Q475. In the absence of a sawtooth signal at the emitter of Q426, Q472 is conducting and Q468 is held off by the positive level set at its base by the Delayed

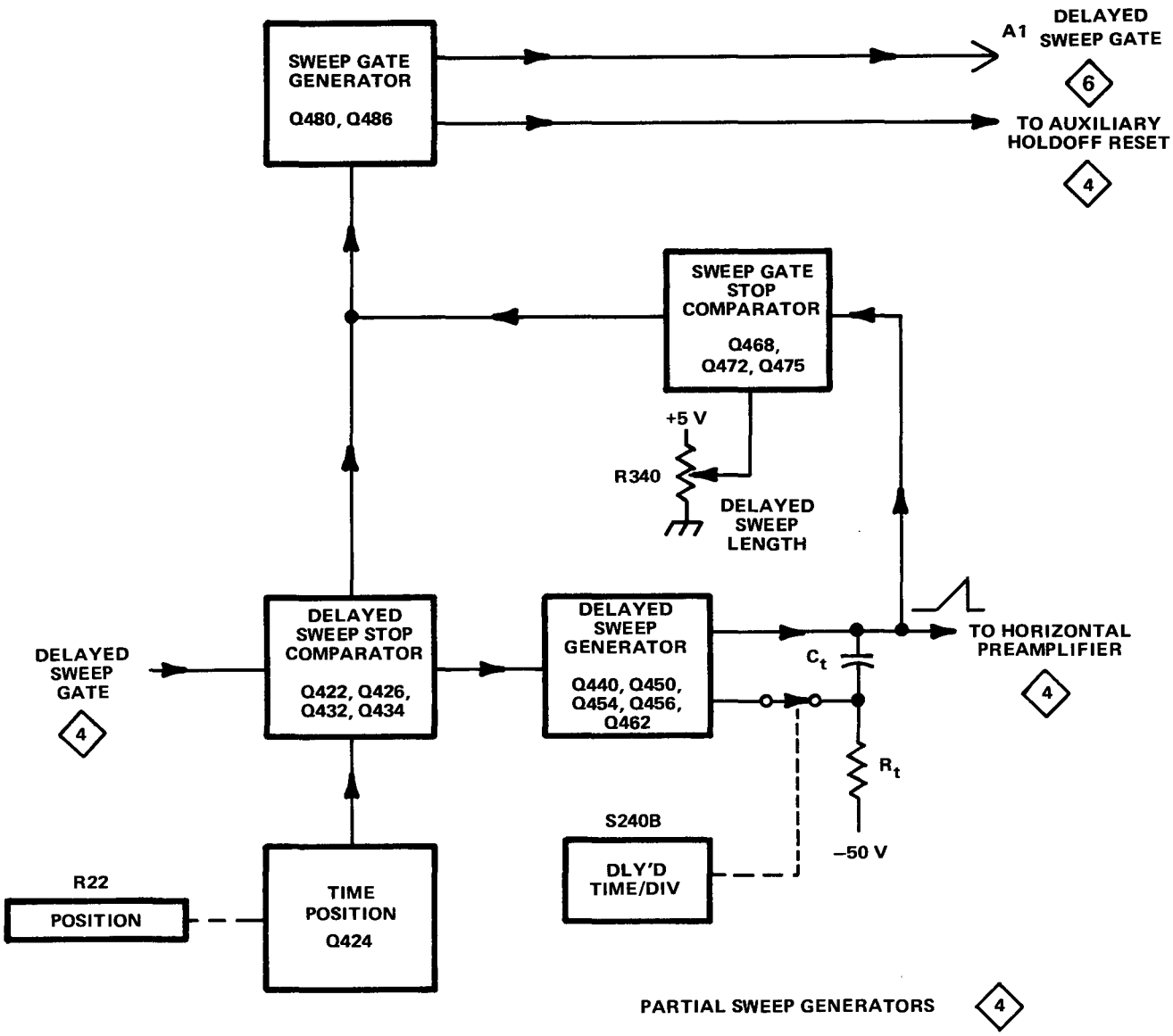


Fig. 5. Delayed Sweep Generator detailed block diagram.

Sweep Length adjustment R465. When the sawtooth voltage at the base of Q472 raises higher than the base of Q468, Q472 turns off and Q468 turns on. A high level is coupled to the sweep gate generator by way of Q475.

Sweep Gate Generator

The Sweep Gate Generator provides a gate pulse to generate unblanking signals for the oscilloscope crt. The unblanking signal is coupled to the oscilloscope by way of Interface connector pin A1.

In the absence of a sweep gate at the delayed sweep start comparator, the collector of Q426 is low. Q480 and Q486 are off and the gate pulse is low at pin A1. Upon arrival of a sweep gate pulse from the Delayed Trigger circuits, the Sweep Start Comparator switches. Q480 turns on and its collector rises. The high level is coupled through emitter follower Q486 to pin A1. At Delayed Sweep Gate Stop Comparison or at Delaying Sweep Stop comparison (whichever occurs first) the high level at its base turns on Q475. Its collector falls; Q480 and Q482 turn off and set the sweep gate to the low level.

HORIZONTAL PREAMPLIFIER AND DISPLAY MODE SWITCHING (4)

The Horizontal Preamplifier and Display Mode Switching Circuits select the source of the output signal (delaying or delayed sweep) and supplies an amplified sawtooth signal to the horizontal circuits in the oscilloscope. In addition, this circuit contains the horizontal positioning networks. Figure 6 shows a detailed block diagram and the schematic is shown on schematic 4 in the diagrams section of the service manual. Refer to diagram 1 at the rear of the service manual for front-panel switching detail.

Horizontal Source Selector and Output Amplifier

The Horizontal Source selector circuits work in conjunction with the Display Mode Switching circuits to determine whether the delaying sweep or delayed sweep sawtooth signal is coupled to the oscilloscope at interface connector pins A11 and B11. Both the delaying and the delayed sweeps run simultaneously.

When pin 5 of Display Mode Switching integrated circuit U380A is high and pin 6 is low, the high level at its base turns off Q517. Emitter current is removed from paraphase amplifier Q514 and Q533 and the delaying sweep sawtooth signal is locked out. The low level at pin 6 of U380A is coupled to the base of Q550. Q550 turns on and supplies emitter current for paraphase amplifier Q555 and Q559. The delayed sweep sawtooth signal, coupled into the base of Q559, is amplified push-pull to Interface connector pins A11 and B11. The base of Q555 is driven by the POSITION control.

When pin 5 of U380A is low and pin 6 is high, Q550, Q555, and Q559 turn off. Q517 turns on and supplies

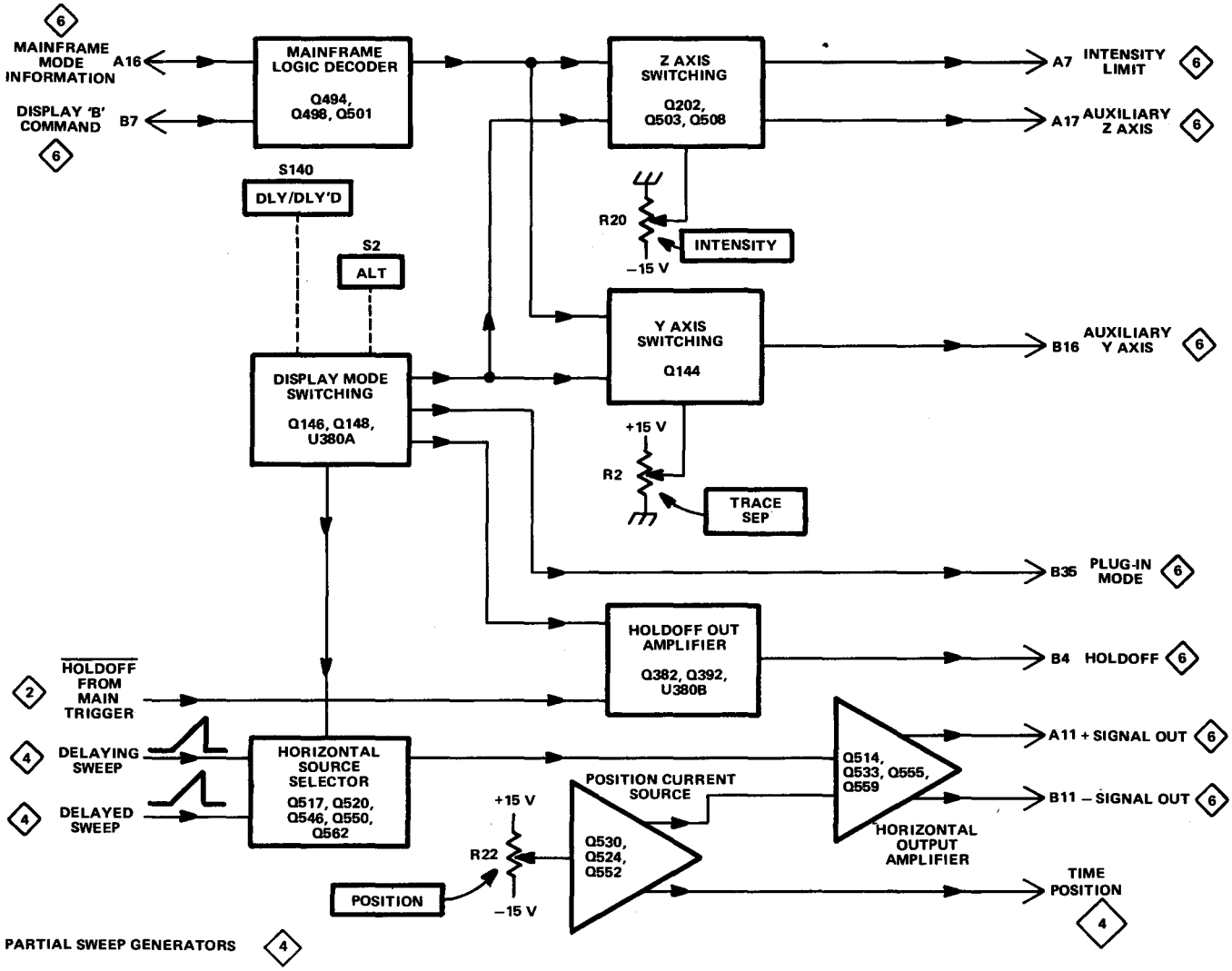


Fig. 6. Horizontal Preamplifier and Display Mode Switching detailed block diagram.

emitter current for paraphase amplifer Q514 and Q533. The delaying sweep sawtooth signal, coupled into the base of Q514, is amplified push-pull to interface connector pins A11 and B11. The base of Q533 is driven by the POSITION control.

Position Current Amplifier

The POSITION control (R22) varies the current through Q524. This sets the bias on the bases of Q530 and Q552, thus setting the DC current coupled to the horizontal amplifier.

Display Mode Switching

When the ALT switch (S2) is pressed in (non-alternate mode), +5 volts is applied to Q146. Q146 saturates and its collector falls to ground. With S140 set to Delayed, pin 4 of flip-flop U380A is set to ground. Pin 5 is low and pin 6 is high. Therefore, the delayed sweep sawtooth signal is coupled to the horizontal preamplifier. When S140 is set to Delayed Sweep, pin 1 of U380A is set to ground. Pin 5 is high and pin 6 is low. Therefore, the delaying sweep sawtooth signal is coupled to the horizontal preamplifier.

When the ALT switch is released for the ALT Display Mode, the ground level is removed from Flip Flop U380A. U380A switches to the clocked mode.

The $\overline{\text{SWEEP GATE}}$ pulse into pin 3 of U380A alternately changes the level of pins 5 and 6. Therefore, the delaying and delayed sweep sawtooth signals are alternately coupled to the horizontal amplifer.

Holdoff Output Amplifier

U380B, Q382, and Q392 compose the Holdoff output amplifier and Holdoff divide by two network. When the ALT switch (S2) is pressed in (non-alternate mode), the collector of saturated Q146 pulls pin 10 of flip-flop U380B to ground. This sets the level at pin 10 low. In this condition, Q382 supplies current to Q392 so that each $\overline{\text{HOLDOFF}}$ pulse at its base will provide a positive-going HOLDOFF pulse at the collector of Q392, and therefore Interface connector pin B4.

When ALT switch is OUT (Alternate Display Mode), the ground is removed from pin 10 of U380B. Flip-flop U380B switches to the divide by 2 mode.

On alternate $\overline{\text{HOLDOFF}}$ pulses from U310, a negative level at pin 8 of U380B activates Q382 and supplies current to Q392. Therefore, Q392 supplies a positive-going gate pulse to Interface connector pin B4 at the arrival of every other $\overline{\text{HOLDOFF}}$ pulse from U310.

Mainframe Logic Decoder

The mainframe logic decoder includes Q494, Q498, and Q501. These circuits use the oscilloscope mode and switching levels to determine when the sweep signal from the 7B92 is being displayed on the crt.

Aux Z Axis Switching

When the delaying sweep is being displayed and the appropriate levels are present at Interface connector pins A16 and B17 (one level high and one level low), the proper current flows at Interface connector pin A17 to intensify the 7B92 delaying sweep trace. INTENSITY control R20 varies the current at A17 to vary the intensity of the 7B92 delaying sweep trace. Q202 limits the Z-AXIS drive when slow sweep speeds are used. Q503 couples delaying sweep display information.

Aux Y Axis Switching

When the delaying sweep is being displayed and the appropriate levels are present at Interface connector pins A16 and B7 (one level high and one level low), the proper current flows at Interface connector pin B16 to vertically position the delaying sweep trace on the crt display. The vertical position is determined by the TRACE SEP control R2.

READOUT SWITCHING ◇5

The Readout Switching circuit consists of switching resistors that signal the oscilloscope readout system of the Time Base unit sweep rate. The switching resistors are selected by the TIME/DIV switch. The schematic for Readout Switching is shown on diagram 5 at the rear of the service manual. Table 1 lists the resistors that control the various readout characters and functions.

The Readout System

The Readout System in the 7000-series oscilloscope provides alpha-numeric display of information encoded by the plug-in units. This display is presented on the crt and is written by the crt beam on a time-shared basis with the analog waveform display.

The Readout System produces a pulse train consisting of ten negative-going pulses called time-slots. These pulses represent a possible character in a readout word, and each is assigned a time-slot number corresponding to its position in the word. Each time-slot pulse is directed to one of ten output lines, labelled TS-1 through TS-10 (time-slots one through ten), which are connected to the vertical and horizontal plug-in compartments. Two output lines, row and column, are connected from each channel (two channels per plug-in compartment) back to the Readout System.

Data is encoded on these output lines either by connecting resistors between them and the time-slot input lines or by generating equivalent currents. The resultant output is a sequence of analog current levels on the row and column output lines.. The row and column current levels are decoded by the Readout System to address a character matrix during each time-slot, thus selecting a character to be displayed or a special instruction to be followed.

TABLE 1

7B92 Readout Character Selection

Characters	Time-Slot	Description	Encoded By	
			Channel 1 (Delaying Sweep)	Channel 2 (Delayed Sweep)
Decimal	TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information)	R239, R1031, R1033	R238, R1003, R1005
Uncalibrated (>)	TS-3	Indicates calibrated or uncalibrated sweep rates	R234	R233
1,2,5	TS-4	Scaling	R232, R1027, R1029	R231, R1007 R1009
m, μ, n, p	TS-8	Defines the prefix which modifies the units of measurement	R228, R229, R1023, R1025	R226, R227, R1011, R1013, R1015
s (seconds)	TS-9	Defines the unit of measurement	R223, R224	R221, R222

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