

NCR 5380 FAMILY

1 INTRODUCTION

1.1 GENERAL DESCRIPTION

The NCR 5380 family of devices are designed to meet the SCSI protocol as defined by the ANSI X3.131-1986 standard. This family of chips can function as an initiator or a target allowing them to be used in host adaptor and peripheral controller applications. These devices support arbitration as well as reselection. All chips in this family contain on-chip single-ended drivers which allow for direct connection to the SCSI bus. These chips are controlled by reading and writing several internal registers which may be accessed by standard or memory-mapped I/O. Minimal processor intervention is required for DMA transfers because the 5380 family of chips control the SCSI handshaking signals.

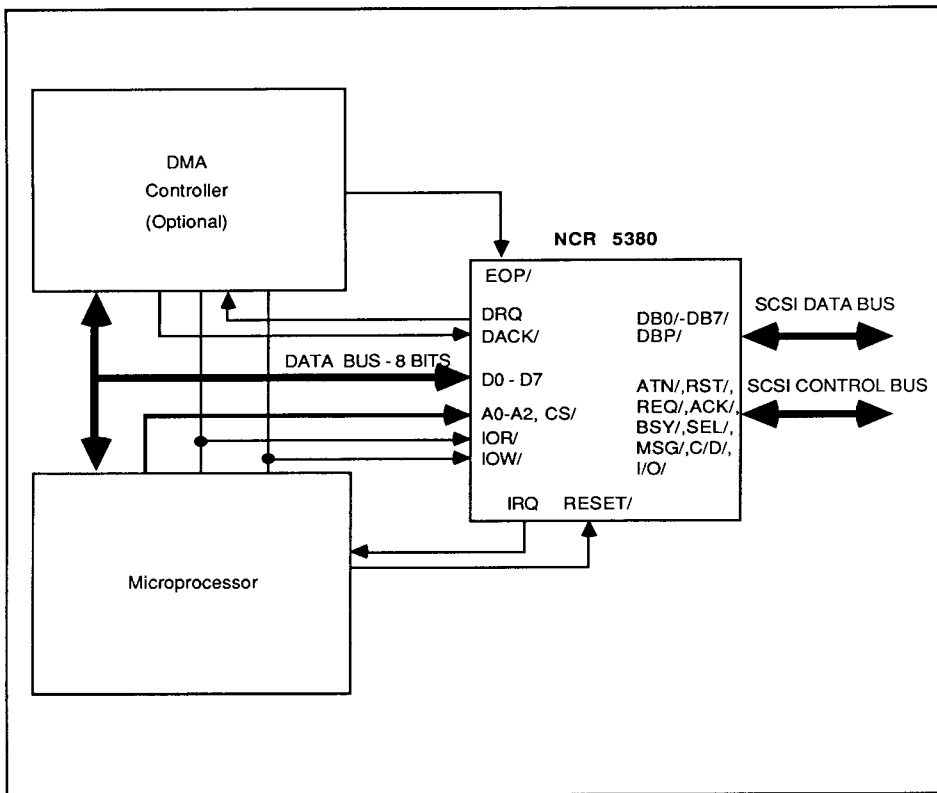
The 53C80 chip can be used as a core cell in ASIC designs. The design methodology and functionality has been proven in many core cell designs including the 53C300 & 53C400.

There are five products that are described in this manual: the NCR 5380, the 53C80-40, the 53C80, the 5381, and the 53C81. The 5380 is an SCSI protocol controller that contains several registers which are used to control the SCSI signals. The 53C80-40 is a CMOS part designed as a higher performance CMOS replacement for the NMOS 5380. The 53C80 is functionally equivalent to the 5380 except that it was designed using CMOS technology. The NMOS 5381 is also functionally equivalent to the NMOS 5380 except that the 5381 includes signals which support the SCSI differential mode of operation. The 53C81 is identical to the 5381 except that it is a CMOS version of the part. All of these parts come in a variety of packages. (See Section 2.2.)

1.2 FEATURES SUMMARY

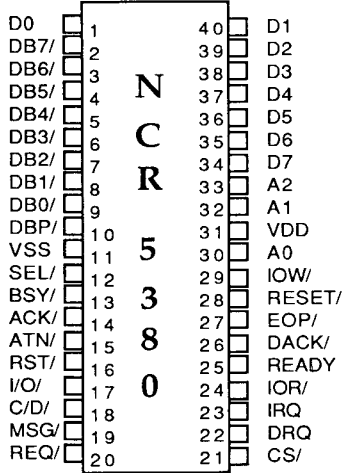
- Supports the ANSI X3.131-1986 standard
- Parity generation with optional checking
- No external clock required
- On-chip 48mA single-ended drivers and receivers
- Functions in both the target and initiator roles
- Direct control of all SCSI signals
- Asynchronous data transfers of up to 3.0 Mbytes/sec
- Variety of packaging options
- SCSI protocol efficiency is directly proportional to the speed of the microprocessor.
- CMOS parts provide additional grounding and controlled fall times that reduce noise generated by SCSI bus switching
- 5381/53C81 provide control logic for differential mode operation

1.3 NCR 5380 SYSTEM DIAGRAM

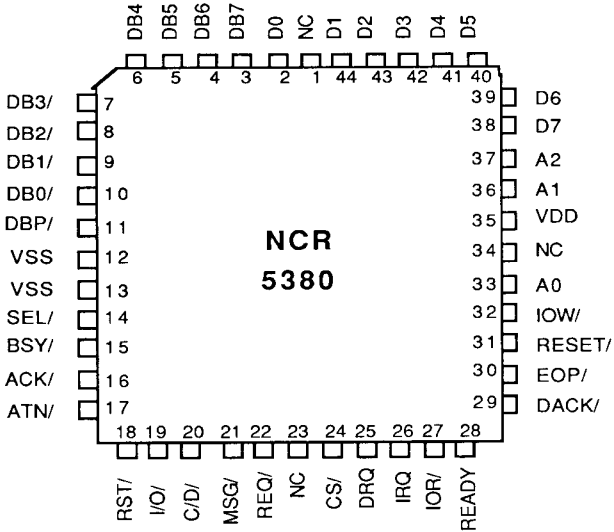


NCR 5380 PIN DIAGRAM

The following pin diagrams describe the NCR 5380 and the NCR 53C80-40.



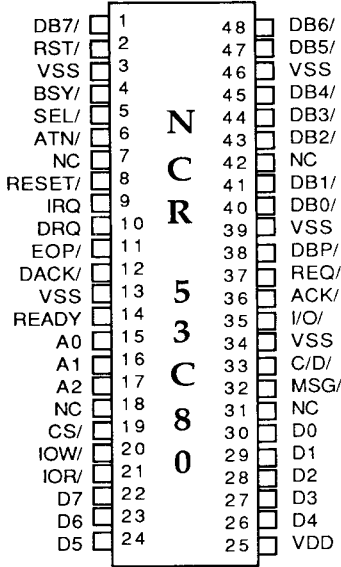
40-pin DIP package



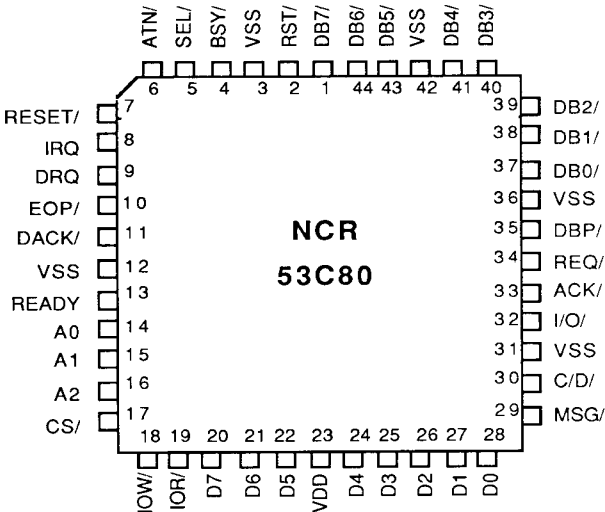
44-pin PLCC package

NCR 53C80 PIN DIAGRAM

The following pin diagrams describe the NCR 53C80.



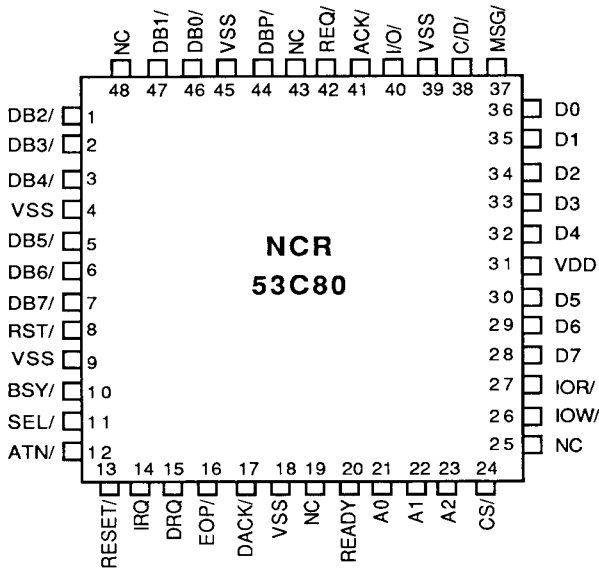
48-pin DIP package



44-pin PLCC package

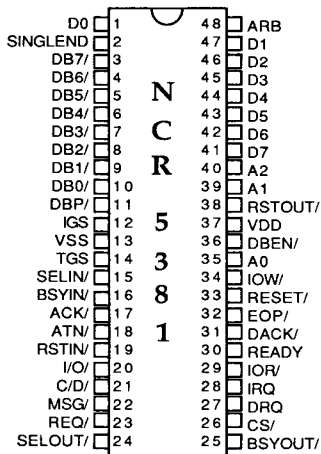
NCR 53C80 PIN DIAGRAM

The following pin diagram describes the NCR 53C80 48 pin Quad Flat Pack package.



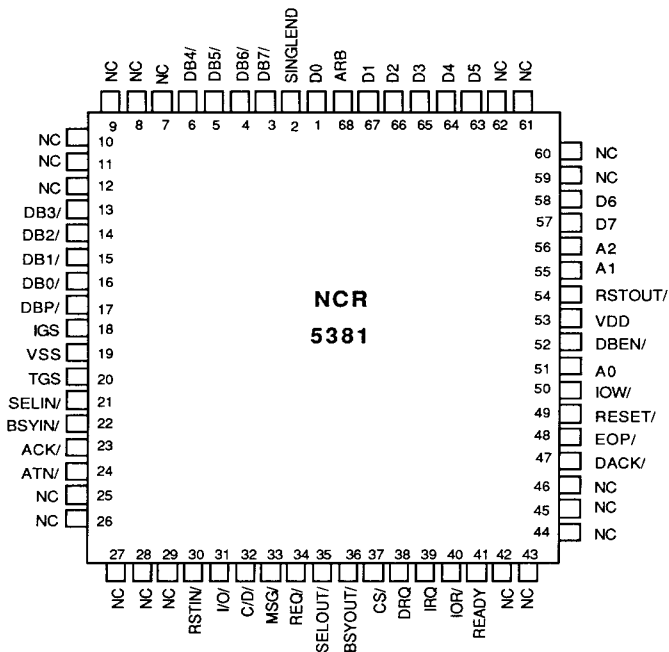
NCR 5381 PIN DIAGRAM

The following pin diagram describes the NCR 5381 48 pin DIP package.



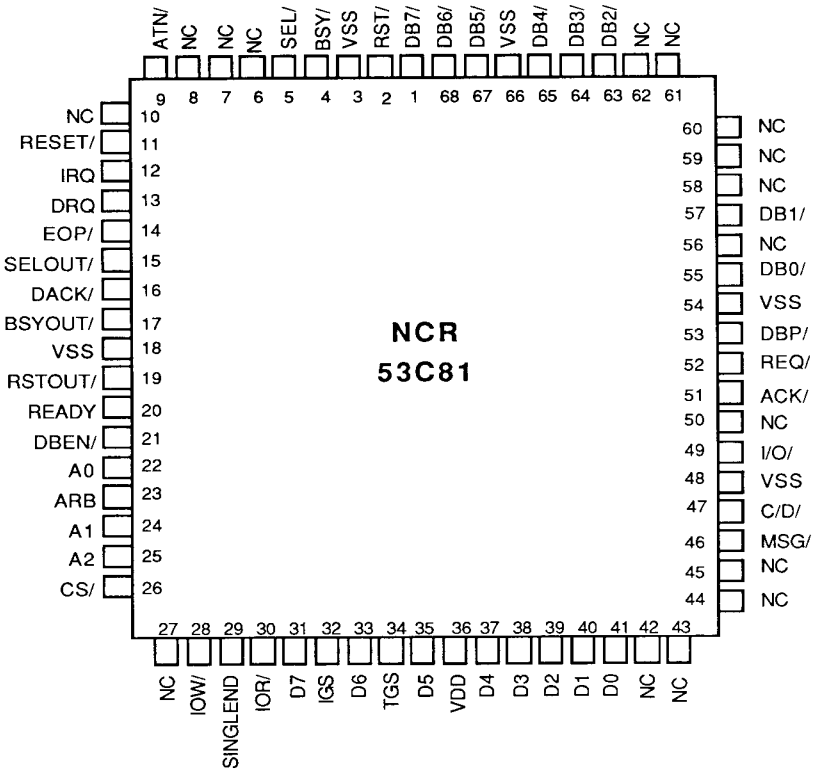
NCR 5381 PIN DIAGRAM

The following pin diagram describes the NCR 5381 68 pin PLCC package.



NCR 53C81 PIN DIAGRAM

The following pin diagram describes the NCR 53C81 68 pin PLCC package.



2 PIN INFORMATION

(Note: A slash "/" indicates an active low signal)

2.1 PIN DESCRIPTION

2.1.1 MICROPROCESSOR INTERFACE SIGNALS

<u>SYMBOL</u>	<u>TYPE</u>	<u>Description</u>
A0-A2	Input	Address Lines - A0-A2 are used with CS/, IOR/, and IOW/ to access all internal registers.
CS/	Input	Chip Select - CS/ enables the microprocessor to read or write any one of the internal registers selected by Address Lines A0-A2. CS/ and DACK/ must never be active at the same time.
DACK/	Input	DMA Acknowledge - DACK/ is used in conjunction with IOR/ and IOW/ to enable reading or writing the SCSI Input and Output Data Registers when the chip is in DMA Mode. This signal is received in response to the DRQ to acknowledge that the byte has been successfully transferred to/from the DMA controller. DACK/ and CS/ must never be active at the same time.
DRQ	Output	DMA Request - DRQ indicates that the chip is ready to transfer a data byte to/from the DMA controller. The DMA Request will only occur if the DMA Mode bit (Register 2, Bit 1) is set. Upon receipt of DACK/, the transfer is complete.
D0-D7	Input/Output	Data Bus - The Data Bus is shared between the microprocessor and the DMA controller. Both DMA and programmed I/O transfers occur on this bus. D7 is the most significant bit of this bus.
EOP/	Input	End of Process - EOP/ is used to terminate a DMA transfer. If asserted during a DMA cycle, the current byte will be transferred but no additional bytes will be requested. EOP/ can be used to generate an interrupt when it is received from a DMA Controller.
IOR/	Input	I/O Read - IOR/ is used to read an internal register selected by CS/ and A0-A2. It also selects the Input Data Register when DACK/ is active during DMA transfers.
IOW/	Input	I/O Write - IOW/ is used to write to an internal register selected by CS/ and A0-A2. It also selects the Output Data Register when used with DACK/ during DMA transfers.

IRQ	Output	Interrupt Request - IRQ alerts the microprocessor of a condition that needs to be serviced. Most of the interrupts are individually maskable.
READY	Output	Ready - READY can be used to control the data transfer handshaking of block mode DMA transfers. This signal goes active to indicate that the chip is ready to transfer data and remains false after a transfer until the chip is ready for another DMA transfer. READY is always active when the DMA Mode Bit is a zero (0).
RESET/	Input	Reset - Reset clears all internal registers when active. It does not assert the SCSI RST/ signal and therefore does not reset the SCSI bus.

2.1.2 SCSI INTERFACE SIGNALS

The following signals are all bi-directional, active low, open-drain signals. With 48mA sink capability, all pins can interface directly with the SCSI Bus.

ACK/	Input/Output	Acknowledge - Driven by an initiator, ACK/ indicates an acknowledgment for an SCSI data transfer. In the target mode, ACK/ is received as a response to the REQ/ Signal.
ATN/	Input/Output	Attention - ATN/, driven by an initiator, indicates an attention condition. In the target role, ATN/ is received and is responded to by entering the Message Out Phase.
BSY/	Input/Output	Busy - BSY/ indicates that the SCSI Bus is being used. BSY/ can be driven by both the initiator and the target device.
CD/	Input/Output	Control/Data - CD/, driven by a target, indicates Control or Data Information is on the SCSI Bus. This signal is received by the initiator.
IO/	Input/Output	Input/Output - IO/, driven by a target, controls the direction of data transfer on the SCSI Bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.
MSG/	Input/Output	Message - MSG/ is driven active by a target during the Message Phase. This signal is received by the initiator.

REQ/	Input/Output	Request - REQ/, driven by a target, indicates a request for an SCSI data-transfer handshake. This signal is received by the initiator.
RST/	Input/Output	Reset - RST/ indicates an SCSI Bus reset condition.
DB0/-DB7/, DBP/	Input/Output	SCSI Data Bits and Parity Bit - These eight Data Bits (DB0/-DB7/), plus a Parity Bit (DBP/), form the SCSI Bus. DB7/ is the most significant bit and has the highest priority ID during the Arbitration Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.
SEL/	Input/Output	Select - SEL/ is used by an initiator to select a target or by a target to reselect an initiator.

2.1.3 5381/53C81 SIGNALS

<u>SYMBOL</u>	<u>TYPE</u>	<u>Description</u>
ARB	Output	Arbitrate - ARB is asserted when the Arbitrate Bit is set and the device has detected a bus free condition. It can be used to assert the proper device ID on the bus during the Arbitration Phase.
BSYOUT/	Output	Busy Output Enable- BSYOUT/ is asserted whenever the Assert BSY/ Bit is set or the chip is driving BSY/ active during the Arbitration Phase. It will be inactive at all other times.
DBEN/	Output	Data Bus Enable - DBEN/ is used to enable the external transceivers to drive the data bus when the 5381/53C81 is functioning in the differential mode (SINGLE Signal inactive). The DBEN/ Signal is asserted whenever the Assert Data Bus Bit and the Target Mode Bit are set. DBEN/ is also asserted when the Assert Data Bus Bit and the Phase Match Bit are set and both the Target Mode Bit and the IO/ Bit are not set.
IGS	Output	Initiator Group Select - IGS is used to enable the external transceivers to drive ACK/ and ATN/ when the 5381/53C81 is functioning as an initiator in the differential mode. IGS is active when the Target Mode Bit is not set and the Differential Enable Bit is set.
RSTOUT/	Output	Reset Output Enable- RSTOUT/ is active whenever the Assert RST/ Bit is set. Conversely, this signal is inactive whenever the Assert RST/ Bit is not set.

SELOUT/	Output	Select Output Enable- SELOUT/ is active whenever the Assert SEL/ Bit is set. Conversely, this signal is inactive whenever the Assert SEL/ Bit is not set.
SINGLE	Input	Single-ended Mode - SINGLE determines whether the 5381/53C81 functions in single-ended or differential mode. When active, the SINGLE pin forces the chip to operate in the single-ended mode. When inactive, the SINGLE pin forces the chip to operate in differential mode.

The following signals are affected by the status of the SINGLE pin:

<u>SINGLE = 1</u>	<u>SINGLE = 0</u>
BSY/ -- Input/Output	BSY/ -- Input Only
SEL/ -- Input/Output	SEL/ -- Input Only
RST/ -- Input/Output	RST/ -- Input Only
BSYOUT/ -- Not used	BYSOUT/ -- Output Only
SELOUT/ -- Not used	SELOUT/ -- Output Only
RSTOUT/ -- Not used	RSTOUT/ -- Output Only

TGS	Output	Target Group Select - TGS is used to enable external transceivers to drive IO/, CD/, MSG/, and REQ/ when the 5381/53C81 is functioning as a target in the differential mode. TGS is active when the Target Mode Bit and the Differential Enable Bit are set.
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3 REGISTERS

The NCR 5380 family of devices appear as a set of eight registers to the controlling microprocessor. By reading and writing the appropriate registers, the microprocessor may initiate any SCSI bus activity or may sample and assert any signal on the SCSI bus. This allows the user to implement all or portions of the SCSI protocol in software. These registers can be accessed by activating CS/ with a valid address on the A0-A2 Address Lines and then issuing an IOR/ or IOW/ pulse.

Even though some signals are active low, their register representations are active high. For example a one (1) is used to indicate signal assertion and a zero (0) is used to indicate the non-asserted or inactive state.

REGISTER SUMMARY

Address			Type	Register Name
A2	A1	A0	RW	
0	0	0	R	Current SCSI Data
0	0	0	W	Output Data
0	0	1	RW	Initiator Command
0	1	0	RW	Mode
0	1	1	RW	Target Command
1	0	0	R	Current SCSI Bus Status
1	0	0	W	Select Enable
1	0	1	R	Bus and Status
1	0	1	W	Start DMA Send
1	1	0	R	Input Data
1	1	0	W	Start DMA Target Receive
1	1	1	R	Reset Parity/Interrupt
1	1	1	W	Start DMA Initiator Receive

3.1 CURRENT SCSI DATA REGISTER - ADDRESS 0

The Current SCSI Data Register is a read-only register which allows the microprocessor to monitor the active SCSI Bus. If parity checking is enabled, the SCSI Bus parity is checked at the beginning of the read cycle. This register is used during a programmed I/O data read or during arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during arbitration. Note that the SCSI Data Bus is inverted to become active high when presented to the CPU.

3.2 OUTPUT DATA REGISTER - ADDRESS 0

The Output Data Register is a write-only register that sends data to the SCSI Bus. The proper ID bits to drive the SCSI Bus are written to this register during the Arbitration and Selection

Phases. In DMA Mode, this register is written when DACK/ and IOW/ are active. Note that a 1 written to the Output Data Register becomes an active low signal on the SCSI Data Bus.

3.3 INITIATOR COMMAND REGISTER - ADDRESS 1

The Initiator Command Register is a read/write register which asserts certain SCSI Bus signals, monitors those signals, and monitors the progress of SCSI Bus arbitration. Many of these bits are significant only when used as an initiator. However, most can be used during target role operation.

Bit 7 - Assert RST/ - Read/Write

When set, the RST/ Signal is asserted on the SCSI Bus. The RST/ Signal will remain asserted until this bit is reset or until RESET/ (pin 28) is asserted. After this bit is set, IRQ goes active and all SCSI signals are removed except for RST/. Registers 0-7 are reset.

Bit 6 - Arbitration In Progress - Read Only

This bit is used to determine if arbitration is in progress. For this bit to be active, the Arbitrate Bit (Register 2, Bit 0) must have previously been set. The Arbitration In Progress Bit indicates that a bus-free condition has been detected, and that the chip has asserted BSY/ and the contents of the Output Data Register onto the SCSI Bus. Arbitration In Progress will remain set until the Arbitrate Bit is reset.

Bit 6 - Tri-State Mode - Write Only

This bit may be set in a test environment to place all output drivers in the high impedance state.

Bit 5 - Lost Arbitration - Read Only

When set, this bit indicates that the chip has detected a bus-free condition, arbitrated for use of the bus by asserting BSY/ and its ID on the SCSI Bus and lost arbitration due to SEL/ being asserted by another bus device with a higher priority. For this bit to be set, the Arbitrate Bit (Register 2, Bit 0) must be set.

Bit 5 - Differential Enable - Write Only (NCR 5381 and 53C81 Only)

When this bit is set and the SINGLE Signal is inactive, the 5381/53C81 will function in the differential mode. When this bit is set, the TGS Signal or the IGS Signal will be asserted depending on the status of the Target Mode Bit (Register 2, Bit 6).

Bit 4 - Assert ACK/ - Read/Write

This bit is used by the initiator to assert ACK/ onto the SCSI Bus. In order to assert ACK/, the Target Mode Bit (Register 2, Bit 6) must not be set. Writing a zero to this bit de-asserts ACK/ on the SCSI Bus. Reading this register reflects the status of this bit.

Bit 3 - Assert BSY/ - Read/Write

When set, this bit asserts BSY/ onto the SCSI Bus. When reset, this bit de-asserts the BSY/ Signal. Asserting BSY/ indicates a successful selection or reselection and resetting this bit creates a bus free condition. Reading this register reflects the status of this bit.

Bit 2 - Assert SEL/ - Read/Write

When set, this bit asserts SEL/ onto the SCSI Bus. SEL/ is normally asserted after arbitration has been successfully completed. When reset, this bit de-asserts the SEL/ Signal. Reading this register reflects the status of this bit.

Bit 1 - Assert ATN/ - Read/Write

When set, this bit asserts ATN/ onto the SCSI Bus if the Target Mode Bit (Register 2, Bit 6) is not set. ATN/ is normally asserted by the initiator to request a Message Out Phase. When reset, this bit de-asserts the ATN/ Signal. Reading this register reflects the status of this bit.

Bit 0 - Assert Data Bus - Read/Write

When set, this bit allows the contents of the Output Data Register to be enabled as chip outputs on SCSI signals DB0/ through DB7/. Parity is also generated and asserted on DBP/. When connected as an initiator, the outputs are only enabled if the Target Mode Bit (Register 2, Bit 6) is not set, and the phase signals CD/, IO/, and MSG/ match the contents of the Assert CD/, Assert I/O, and Assert MSG/ in the Target Command Register. When connected as a target, the contents of the Output Data Register will be enabled on the SCSI Data Bus unconditionally. The Assert Data Bus Bit should also be set during DMA operations. Reading this register reflects the status of this bit.

During arbitration, the Assert Data Bus Bit does not need to be set for the contents of the Output Data Register to be enabled. It should not be set during the arbitration phase.

When set and using the NCR 5381/53C81, this bit will assert the DBEN/ Signal which can be used to enable the external transceivers to drive the SCSI Data Bus.

3.4 MODE REGISTER - ADDRESS 2

The Mode Register is a read/write register used to control the operation of the chip. This register determines whether the chip operates as an initiator or target, whether parity is checked, and whether interrupts are generated on various external conditions.

Bit 7 - Block Mode DMA - Read/Write

The Block Mode DMA Bit controls the characteristics of the DMA data transfer handshake. When this bit is reset and the DMA Mode Bit is active, the DMA data transfer handshake is the normal DRQ-DACK/ handshake and the rising edge of DACK/ indicates the end of each byte being transferred. In block mode operation, when the Block Mode DMA Bit is set, and the DMA Mode Bit set, the end of IOR/ or IOW/ signifies the end of each byte transferred and DRQ and DACK/ are allowed to

remain active throughout the DMA operation. **READY** can then be used to request the next transfer. Reading this register reflects the status of this bit.

Bit 6 - Target Mode - Read/Write

When set, the chip operates as an SCSI Bus target device. When reset, the chip operates as an SCSI Bus initiator device. In order for the signals **ATN/** and **ACK/** to be asserted onto the SCSI Bus, the Target Mode Bit must not be set. In order for the signals **CD/**, **IO/**, **MSG/**, and **REQ/** to be asserted onto the SCSI Bus, the Target Mode Bit must be set. Reading this register reflects the status of this bit.

When using the NCR 5381/53C81 this signal will assert the TGS Signal which can be used to enable the external transceivers to drive the **IO/**, **CD/**, **MSG/**, and **REQ/** Signals.

Bit 5 - Enable Parity Checking - Read/Write

When this bit is set, data received on the SCSI Data Bus is checked for odd parity. If a parity error occurs, the Parity Error Bit (Register 5, Bit 5) will be set. When this bit is reset or not set, parity errors are ignored. This bit must be set if a Parity Error Interrupt is to be generated when bad parity is detected. Reading this register reflects the status of this bit.

Bit 4 - Enable Parity Interrupt - Read/Write

When set, this bit causes the **IRQ** Signal to be asserted if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking Bit is also set. Reading this register reflects the status of this bit.

Bit 3 - Enable EOP Interrupt - Read/Write

When set, this bit causes the **IRQ** Signal to be asserted when an **EOP/** signal is received from the DMA controller. Normally the DMA controller will generate the valid **EOP/** Signal to indicate the end of a DMA transfer. The **EOP/** Signal, **IOR/** or **IOW/** Signal, and **DACK/** Signal must be active simultaneously for the **EOP/** Signal to be recognized. Reading this register reflects the status of this bit.

Bit 2 - Monitor Busy - Read/Write

When set, this bit causes the **IRQ** Signal to be asserted when **BSY/** unexpectedly changes to the inactive state for at least a Bus Settle Delay (400 ns). When the interrupt is generated, the lower six bits of the Initiator Command Register are reset and all signals are de-asserted on the SCSI Bus. The Busy Error Bit (Register 5, Bit 2) will also be set when this condition occurs. This bit also allows the microprocessor to be interrupted when the SCSI Bus is free in systems where the Arbitration Phase is not implemented. Reading this register reflects the status of this bit.

Bit 1 - DMA Mode - Read/Write

The DMA Mode Bit allows a DMA transfer to occur and must be set prior to writing Registers 5 to 7. Registers 5 to 7 are used to start DMA transfers. The Target Mode Bit (Register 2, Bit 6) must be set for a write to Register 6 and reset for a write to Register 7. The Assert Data Bus Bit (Register 1, Bit 0) must be set for all DMA send operations. In the DMA Mode, **REQ/** and **ACK/** are automatically controlled. Reading this register reflects the status of this bit.

Bit 0 - Arbitrate - Read/Write

When set, this bit starts the arbitration process when a bus free condition has been detected. Prior to setting this bit the Output Data Register should contain the proper SCSI device ID value. One data bit should be active for SCSI Bus arbitration. The chip will wait for a bus-free condition before entering the Arbitration Phase. The status of the Arbitration Phase may be determined by reading the Lost Arbitration and Arbitration In Progress Bits (Register 1, Bits 5 and 6 respectively). Reading this register reflects the status of this bit.

When using the NCR 5381/53C81, setting the Arbitrate bit will assert the ARB Signal which can be used to assert the proper device ID on the SCSI Data Bus during the Arbitration Phase.

3.5 TARGET COMMAND REGISTER - ADDRESS 3

The Target Command Register is a read/write register that controls some target functions. When the chip is connected as a target device this register allows the microprocessor to control the SCSI Bus Information Transfer Phase and/or to assert REQ/ by writing this register. The Target Mode Bit (Register 2, Bit 6) must be set for bus assertion to occur. If the chip is connected as an initiator with the DMA Mode Bit (Register 2, Bit 1) set, and the IO/, CD/, and MSG/ phase lines do not match the phase bits in the Target Command Register, a phase mismatch interrupt will be generated when REQ/ goes active. In order to send data as an initiator, the Assert IO/, Assert CD/, and Assert MSG/ Bits must match the corresponding bits in the Current SCSI Bus Status Register (Register 4). The Assert REQ/ Bit has no meaning when operating as an initiator.

Bit 7 - Last Byte Sent - Read Only (Included on all but the 5380 and 5381)

This bit indicates that the last byte of the DMA send operation has been transferred on the SCSI Data Bus. This flag is necessary since the End of DMA Transfer Bit (Register 5, Bit 7) only reflects when the last byte was received from the DMA Controller. This bit is reset when the DMA Mode Bit is reset. This bit should only be examined after the EOP/ signal has been pulsed with DACK/ on the last DMA transfer.

Bit 3 - Assert REQ/ - Read/Write

When this bit is set, REQ/ is asserted. The REQ/ Signal will only be asserted if the Target Mode Bit is set indicating that the chip is functioning as a target. Reading this register reflects the status of this bit.

Bit 2 - Assert MSG/ - Read/Write

When this bit is set, MSG/ is asserted. The MSG/ Signal will only be asserted if the Target Mode Bit is set indicating that the chip is functioning as a target. When the chip is functioning as an initiator, this bit is compared with the MSG/ Bit in the Current SCSI Bus Status Register and an interrupt is generated if they differ on the falling edge of REQ/. Reading this register reflects the status of this bit.

Bit 1 - Assert CD/ - Read/Write

When this bit is set, CD/ is asserted. The CD/ Signal will only be asserted if the Target Mode Bit is set indicating that the chip is functioning as a target. When the chip is functioning as an initiator, this bit is compared with the CD/ Bit in the Current SCSI Bus Status Register and an interrupt is generated if they differ on the falling edge of REQ/. Reading this register reflects the status of this bit.

Bit 0 - Assert IO/ - Read/Write

When this bit is set, IO/ is asserted. The IO/ Signal will only be asserted if the Target Mode Bit is set indicating that the chip is functioning as a target. When the chip is functioning as an initiator, this bit is compared with the IO/ Bit in the Current SCSI Bus Status Register and an interrupt is generated if they differ on the falling edge of REQ/. Reading this register reflects the status of this bit.

SCSI Information Transfer Phases

Bus Phase	SMSG/	SC/D/	SI/O/
Data Out	0	0	0
Data In	0	0	1
Command	0	1	0
Status	0	1	1
Unspecified	1	0	0
Unspecified	1	0	1
Message Out	1	1	0
Message In	1	1	1

Note: A (0) represents an inactive state and a (1) represents an active state.

3.6 CURRENT SCSI BUS STATUS REGISTER - ADDRESS 4

The Current SCSI Bus Status Register is a read-only register which monitors seven SCSI Bus control signals plus the SCSI Data Bus Parity Bit. The SCSI control signals are not latched, but actually represent the current state of that signal.

When a bit is set, it represents an active signal; when a bit is not set or reset, it represents an inactive signal.

Bit 7 - RST/

Bit 6 - BSY/

Bit 5 - REQ/

Bit 4 - MSG/

Bit 3 - CD/

Bit 2 - IO/

Bit 1 - SEL/

Bit 0 - DBP/

3.7 SELECT ENABLE REGISTER - ADDRESS 4

The Select Enable Register is a write-only register which masks all but a single ID bit during a selection attempt. The SCSI ID to be monitored is written as a one (1) in the register. For example, if the chip has SCSI ID 7, then Bit 7 must be set for the interrupt to be generated after another device has successfully selected the chip. The simultaneous occurrence of the correct SCSI ID, BSY/ inactive, and SEL/ active will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the Enable Parity Checking Bit (Register 2, Bit 5) is active, parity will be checked during selection.

3.8 BUS AND STATUS REGISTER - ADDRESS 5

The Bus and Status Register is a read-only register which monitors six status bits and the two SCSI control signals (ATN/ and ACK/) which are not found in the Current SCSI Bus Status Register (Register 4). It provides a means for the microprocessor to determine the status of the DMA transfer.

Bit 7 - End of DMA Transfer

This bit is set if EOP/, DACK/, and IOR/ or IOW/ are simultaneously active. Since the EOP/ Signal can occur during the last byte sent to the Output Data Register, the REQ/ and ACK/ Signals should be monitored to insure that the last byte has been transferred. On all chips, except the 5380 and 5381, the Last Byte Sent Bit (Register 3, Bit 7) should be monitored after receipt of an EOP/ pulse to ensure that the last byte sent to the Output Data Register (Register 0) has been transferred to the SCSI Bus. This bit is reset when the DMA Mode Bit (Register 2, Bit 1) is reset.

The DMA Mode Bit is automatically reset whenever a Busy Error occurs, which in turn resets the End of DMA Transfer Bit. Therefore, the Bus and Status Register should be read prior to resetting the Assert BSY/ Bit at the conclusion of a DMA transfer.

Bit 6 - DMA Request

This bit allows the microprocessor to sample the DRQ Signal. DRQ can be cleared by asserting the DACK/ Signal and the IOR/ or IOW/ Signal or by resetting the DMA Mode Bit (Register 2, Bit 1). The DRQ Signal does not reset when a phase mismatch interrupt occurs.

Bit 5 - Parity Error

This bit is set if a parity error occurs when receiving data or during a device selection. Parity errors can be detected in both initiator and target modes of operation. It can only be set if the Enable Parity Checking Bit (Register 2, Bit 5) is set. This bit may be cleared by reading the Reset Parity/Interrupt Register (Register 7).

Bit 4 - Interrupt Request Active

This bit indicates whether an interrupt condition has been detected. It reflects the current state of the IRQ Signal and can be cleared by reading the Reset Parity/Interrupt Register (Register 7).

Bit 3 - Phase Match

The SCSI MSG/, CD/, and IO/ Signals represent the current Information Transfer Phase. The Phase Match Bit indicates whether the current SCSI Bus phase matches the Assert MSG/ Bit, the Assert CD/ Bit, and the Assert IO/ Bit of the Target Command Register (Register 3). The Phase Match Bit is continuously updated and is only significant when operating as a bus initiator. A phase match is required for data transfer to occur on the SCSI Bus.

Bit 2 - Busy Error

This bit is active if the BSY/ Signal unexpectedly changes to the inactive state for at least a Bus Settle Delay (400 ns) while the Monitor Busy Bit (Register 2, Bit 2) is set. The Busy Error Bit will disable any SCSI outputs and will reset the DMA Mode Bit (Register 2, Bit 1). The Busy Error Bit can be reset by reading the Reset Error/Interrupt Register (Register 7).

Bit 1 - ATN/

This bit reflects the condition of the SCSI ATN/ Signal . When this bit is set, ATN/ is active. This signal is normally monitored by the target device.

Bit 0 - ACK/

This bit reflects the condition of the SCSI Bus control signal ACK/. When this bit is set, ACK/ is active. This signal is normally monitored by the target device.

3.9 START DMA SEND REGISTER - ADDRESS 5

The Start DMA Send Register produces a strobe which starts a DMA send from the chip to the SCSI Bus. To initiate a DMA Send operation, the DMA Mode Bit (Register 2, Bit 1) must be set. Any value written to this write only register will start the DMA send operation. The Start DMA Send operation can be issued in either the initiator or the target mode.

3.10 INPUT DATA REGISTER - ADDRESS 6

The Input Data Register is a read-only register that is used to receive data from the SCSI Bus during DMA transfers. In the initiator mode the data is latched on the falling edge of REQ/ and in the target mode the data is latched on the falling edge of ACK/. The contents of this

register represent the complement of the active low SCSI Data Bus. Parity may optionally be checked as data is latched into this register.

3.11 START DMA TARGET RECEIVE REGISTER - ADDRESS 6

The Start DMA Target Receive Register is a write only register which is written to initiate a DMA receive from the SCSI Bus to the chip for target operation only. To initiate a DMA Target Receive operation, the DMA Mode Bit (Register 2, Bit 1) and the Target Mode Bit (Register 2, Bit 6) must be set. Any value written to this register will start the DMA Target Receive Operation.

3.12 RESET PARITY/INTERRUPT REGISTER - ADDRESS 7

The Reset Parity/Interrupt Register, a read only register, resets the Parity Error Bit, the Interrupt Request Bit, and the Busy Error Bit in the Bus and Status Register (Register 5). Reading this register will de-assert the IRQ Signal.

3.13 START DMA INITIATOR RECEIVE REGISTER - ADDRESS 7

The Start DMA Initiator Receive Register, a write only register, is written to initiate a DMA Receive from the SCSI Bus to the chip for initiator operation only. To initiate a DMA Initiator Receive operation, the DMA Mode Bit (Register 2, Bit 1) must be set and the Target Mode Bit (Register 2, Bit 6) must not be set. Any value written to this register will start the DMA Initiator Receive Operation.

4 FUNCTIONAL DESCRIPTION

4.1 RESET CONDITIONS

4.1.1 HARDWARE CHIP RESET

When the RESET/ signal goes active, the NCR 5380 family of devices will clear all internal logic and control registers. This is a chip reset only and it does not create an SCSI Bus reset condition.

4.1.2 SCSI BUS RST/ RECEIVED

When an SCSI RST/ Signal is received, the IRQ Signal is asserted and a chip reset is performed. All internal logic and registers are cleared, except for the IRQ interrupt latch and the Assert RST/ Bit in the Initiator Command Register. The RST/ Signal may be sampled by reading the Current SCSI Bus Status Register; however this signal is not latched and may not be present when this register is read.

4.1.3 SCSI BUS RST/ ISSUED

If the microprocessor sets the Assert RST/ bit in the Initiator Command Register, the RST/ Signal goes active on the SCSI Bus and an internal reset is performed. All internal logic and registers are cleared except for the IRQ interrupt latch and the Assert RST/ Bit in the Initiator Command Register. The RST/ Signal will continue to be active until the Assert RST/ Bit is reset or until a hardware reset occurs.

4.2 INTERRUPT CONDITIONS

The NCR 5380 family of chips include an interrupt output (IRQ) to indicate a task completion or an abnormal bus occurrence. The use of interrupts is optional and may be disabled by resetting the appropriate bits in the Mode Register or the Select Enable Register.

When an interrupt occurs, the Bus and Status Register and the Current SCSI Bus Status Register must be read to determine which condition created the interrupt. IRQ can be reset simply by reading the Reset Parity/Interrupt Register or by an external chip reset.

If the NCR 5380 family of devices have been initialized properly, an interrupt will be generated: if the chip is selected or reselected, if an EOP/ Signal occurs during DMA transfer, if an SCSI bus reset occurs, if a parity error occurs during a data transfer, if a bus phase mismatch occurs, or if an SCSI Bus disconnection occurs.

4.2.1 SELECTION/RESELECTION INTERRUPT

The NCR 5380 family of devices can generate a select interrupt if the SEL/ Signal is active, the 5380's device ID is active on the SCSI Data Bus, and the BSY/ Signal is false for at least a Bus Settle Delay (400 ns). If the IO/ Signal is active, a reselection has taken place. The correct device ID is determined by a match in the Select Enable Register. Only a single bit match is required to generate the interrupt. This interrupt may be disabled by writing zeros into all bits of the Select Enable Register.

During the Selection/Reselection Phase, parity should be valid. Therefore, if the Enable Parity Checking Bit is active, then the Parity Error Bit should be checked to insure that a proper selection has occurred. The Enable Parity Interrupt Bit does not need to be set for this interrupt to be generated.

Note: The ANSI SCSI specification requires that no more than two device ID's be active during the Selection Phase. To insure this, the Current SCSI Data Register should be read.

4.2.2 EOP/ INTERRUPT

The EOP/ Signal, which indicates the end of a DMA transfer, will set the End of DMA Bit and will optionally generate an interrupt if the Enable EOP/ Interrupt Bit is set. The EOP/ pulse will not be recognized unless EOP/, DACK/, and either IOR/ or IOW/ are concurrently active. DMA transfers will still occur if EOP/ is not asserted at the correct time. This interrupt can be disabled by resetting the Enable EOP/ Interrupt Bit.

The End of DMA Bit is used to determine when a block transfer is complete. Receive operations are complete when there is no data left in the chip and no additional handshakes are occurring. The only exception to this is when the chip is receiving data as an initiator and the target opts to send additional data for the same phase. In this case, REQ/ goes active and the new data is present in the Input Data Register. Since a phase mismatch interrupt will not occur, REQ/ and ACK/ need to be sampled to determine that the target is attempting to send more data.

For send operations, the End of DMA Bit is set when the DMA finishes its transfer, but the SCSI transfer may still be in progress. Because of this the REQ/ and ACK/ signals should be sampled until both are inactive. On all chips (**except the 5380 and the 5381**), the Last Byte Sent Bit may be sampled after receipt of the EOP/ signal to determine when the last byte has been transferred. If the chip is connected as an initiator, a phase change interrupt can be used to signal the completion of the transfer .

4.2.3 PARITY ERROR INTERRUPT

An interrupt is generated for a received parity error if the Enable Parity Checking Bit and the Enable Parity Interrupt Bit are set in the Mode Register. Parity is checked during a read of the Current SCSI Data Register, during any SCSI handshake when in DMA mode, and during Selection or Reselection. A parity error can be detected without generating an interrupt by disabling the Enable Parity Interrupt Bit and checking the Parity Error Bit.

4.2.4 BUS PHASE MISMATCH INTERRUPT

The SCSI phase lines are comprised of the signals IO/, CD/, and MSG/. These signals are compared with the corresponding bits in the Target Command Register: Assert IO/, Assert CD/, and Assert MSG/. The comparison occurs continuously and is reflected in the Phase Match Bit of the Bus and Status Register. If the DMA Mode Bit is active and a phase mismatch occurs when REQ/ transitions from false to true, an interrupt is generated.

A phase mismatch prevents any further transfer from occurring. The SCSI Data Bus Signals DB0/-DB7/ and DBP/ will not be driven even though the Assert Data Bus Bit is active. This

interrupt is only significant when the chip is connected as an initiator and may be disabled by resetting the DMA Mode Bit. (Note: It is possible for this interrupt to occur when connected as a target if another device is driving the phase lines to a different state.)

4.2.5 LOSS OF BSY/ INTERRUPT

If the Monitor BSY/ Bit in the Mode Register is active, an interrupt will be generated if the BSY/ Signal goes inactive for at least a Bus Settle Delay (400 ns). This interrupt may be disabled by resetting the Monitor BSY/ Bit.

4.3 DATA TRANSFERS

Data may be transferred between SCSI bus devices in one of four modes: Programmed I/O, Normal DMA, Block Mode DMA, or Pseudo DMA. The following sections describe these modes in detail. (Note: For all data transfer operations DACK/ and CS/ should never be active simultaneously.)

4.3.1 PROGRAMMED I/O TRANSFERS

Programmed I/O is the most primitive form of data transfer. All of the protocol is controlled through software. The REQ/ and ACK/ handshake signals are individually monitored and asserted by reading the appropriate register bits. This type of transfer is normally used when transferring small blocks of data such as command blocks or message and status bytes.

For example, an initiator send operation would begin by setting the CD/, IO/, and MSG/ to the Data Out Phase by setting the appropriate bits in the Target Command Register so that a phase match exists. The data is then loaded into the Output Data Register. The Assert Data Bus Bit is set to enable the contents of the Output Data Register as outputs on the SCSI bus. The microprocessor then polls the REQ/ Bit until it is active. Once REQ/ becomes active, the Phase Match Bit is checked and the Assert ACK/ Bit is set. The REQ/ Bit is sampled until it becomes inactive and the microprocessor resets the Assert ACK/ Bit to complete the transfer.

4.3.2 NORMAL DMA MODE TRANSFERS

DMA transfers are normally used for large block transfers or high speed transfers. The SCSI chip asserts the DRQ DMA Request Signal whenever it is ready for a transfer. The DMA controller or external logic uses the DRQ Signal to generate the DACK/ Signal and an IOR/ or IOW/ pulse to the SCSI chip. The DRQ Signal goes inactive when DACK/ is asserted and DACK/ goes inactive sometime after the minimum read or write pulse width. This process is repeated for every byte. For this mode, DACK/ should not be allowed to cycle unless a transfer is taking place.

4.3.3 BLOCK MODE TRANSFERS

Block Mode DMA transfers allow an external DMA controller (for example, the Intel 8237) to perform sequential DMA transfers without relinquishing the data bus to the microprocessor. Holding DACK/ active prevents the Intel-type microprocessors from gaining control of the system bus. The Block Mode handshake itself does not increase the transfer rate. Preventing

the microprocessor from sharing the system bus does not have any speed advantages and therefore is not recommended for initiator use.

When using Block Mode, the DRQ Signal is asserted by the 5380 to initiate the transfer. In response to the DRQ signal, DACK/ is asserted by the DMA controller and remains asserted throughout the transfer. The SCSI chip asserts the READY Signal after the IOW/ or IOR/ pulse goes inactive, effectively replacing the DRQ Signal. In Intel-type DMA controllers, the READY signal extends the memory read and write cycles. Therefore, the data, D0..D7, is available to be read or written on the system bus until the 5380 is ready for the next byte transfer. This method of transfer prevents the microprocessor from performing any action such as a refresh cycle on the system bus. When using non-block mode DMA, the system bus is free until the SCSI chip asserts DRQ, indicating it is ready for the next byte transfer. The advantage of Non-block mode DMA over block mode DMA is that it allows the microprocessor to use the system bus while the SCSI chip is transferring data across the SCSI bus.

Care must be taken when using this mode due to the operation of READY. If, for example, a phase mismatch interrupt occurs, READY will remain inactive and IRQ will be active. The DMA controller cannot return control of the bus to the microprocessor for the SCSI chip interrupt to be serviced because READY remains inactive. READY must go active to continue the bus cycle. Therefore, the use of EOP/ is suggested in Block Mode so that the microprocessor can regain control of the bus after the last byte has been transferred. Resetting the DMA mode bit will cause READY to go active.

The Block Mode transfers are halted in the same manner as the Non-Block Mode: by resetting the DMA Mode Bit or by using the EOP/ Signal. Information on halting a DMA transfer can be found in the Normal DMA Transfer Section. (See section 4.3.2)

4.3.4 PSEUDO DMA MODE TRANSFERS

The Pseudo DMA Mode of transfer may be used to avoid monitoring and asserting the REQ/-ACK/ handshake signals for programmed I/O transfers. This mode is implemented by programming the SCSI chip to operate in the DMA Mode, but the microprocessor instead of the DMA Controller controls the DMA handshaking. The DRQ Signal may be detected by polling the DRQ Bit in the Bus and Status Register, by sampling the signal through an external port or by using it to generate a microprocessor interrupt. Once DRQ is detected, the microprocessor can perform a DMA read or a DMA write data transfer. This microprocessor read/write is externally decoded to generate the appropriate DACK/ and IOR/ or IOW/ signals.

Often, external decoding logic is necessary to generate the CS/ signal. This same logic may be used to generate DACK/ at no extra system cost and also provides an increased performance in programmed I/O transfers.

4.3.5 HALTING DMA TRANSFERS

The EOP/ Signal can be used to halt a DMA transfer. It should be asserted while DACK/ and IOR/ or IOW/ are simultaneously active to indicate that DMA activity has stopped. If EOP/ is asserted and IOR/ or IOW/ are not active an interrupt will be generated, but the DMA activity will continue. Although an EOP/ signal may indicate that DMA has halted, the last byte must be monitored across the SCSI bus to ensure that it has been sent and the data transfer is complete. This is done on the 5380 and the 5381 by monitoring REQ/ and ACK/. For the

53C80 and the 53C81, the Last Byte Sent Bit (not available on the 5380 and 5381) in the Target Command Register is monitored. The EOP/ Signal does not reset the DMA Mode Bit.

If no EOP/ signal is provided by the DMA controller, the DMA transfer can be halted at any time by resetting the DMA Mode Bit. Resetting the DMA Mode Bit causes DRQ to go inactive. Care must be taken when resetting the DMA Mode Bit. The DMA Mode Bit must be reset after the last DRQ is received and before DACK is asserted to prevent an additional transfer to take place.

A bus phase mismatch interrupt may be used to halt a DMA transfer if the chip is operating as an initiator. This preferred method frees the host from maintaining a data length counter and frees the DMA logic from providing the EOP/ Signal. Because the chip performs a prefetch of the next data byte, in order to successfully complete a DMA send operation, an additional byte of data must be written to the chip. This method is not feasible for the target operation since the target device controls the phase lines.

Since the DMA Mode Bit must be reset and then set again before another DMA transfer can be initiated, it is recommended that the DMA Mode Bit be reset after receiving an EOP/ pulse or a phase mismatch interrupt.

PART V - ELECTRICAL CHARACTERISTICS

D.C. Characteristics

Absolute Maximum Stress Ratings

<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>
Tstg	Storage Temperature	-55	150	°C
VDD	Supply Voltage	-0.5	7.0	V
VIN	Input Voltage	VSS - 0.5	VDD + 0.5	V
ESD*	Electrostatic Discharge Sensitivity	-4000	4000	V

* Test using the human body model--100pF at 1.5kΩ

Operating Conditions

<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>
VDD	Supply Voltage	4.75	5.25	V
IDD	Supply Current (5380 & 5381)		145	mA
IDD	Supply Current (53C80, 53C81, & 53C80-40)		15	mA
Ta	Operating Free-Air	0	70	°C

SCSI Signals

<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>	<u>CONDITIONS</u>
VIH	Input High Voltage	2.0	VDD + 0.5	V	
VIH	Input High Voltage (53C80-40 AC testing only)	2.4	VDD + 0.5	V	
VIL	Input Low Voltage	VSS - 0.5	0.8	V	
VOL	Output Low Voltage	VSS	0.5	V	IOL = 48mA
VHYS	Hysteresis	200	450	mV	
IOL	Output Low Current	48		mA	VOL = 0.5V

I _{IH}	Input High Leakage	50	μA	V _{IH} = 5.25V
I _{IL}	Input Low Leakage (Except RST/)	-50	μA	V _{IL} = V _{SS}
I _{IL}	Input Low Leakage (RST/)	-750	μA	V _{IL} = V _{SS}

Microprocessor Data Bus D0-D7

<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>	<u>CONDITIONS</u>
V _{IH}	Input High Voltage	2.0	VDD + 0.5	V	
V _{IH}	Input High Voltage (53C80 AC testing only)	2.2	VDD + 0.5	V	
V _{IH}	Input High Voltage (53C80-40 AC testing only)	2.4	VDD + 0.5	V	
V _{IL}	Input Low Voltage	VSS - 0.5	0.8	V	
V _{OH}	Output High Voltage	2.4	VDD	V	I _{OH} = -4.0mA
V _{OL}	Output Low Voltage	VSS	0.4	V	I _{OL} = 8.0mA
I _{OH}	Output High Current	-4.0		mA	V _{OH} = VDD-0.5V
I _{OL}	Output Low Current	8.0		mA	V _{OL} = 0.4V
I _{IH}	Input High Leakage		10	μA	V _{IH} = 5.25V
I _{IL}	Input Low Leakage		-10	μA	V _{IL} = V _{SS}
I _{TL}	Tri-State Leakage	-10	10	μA	

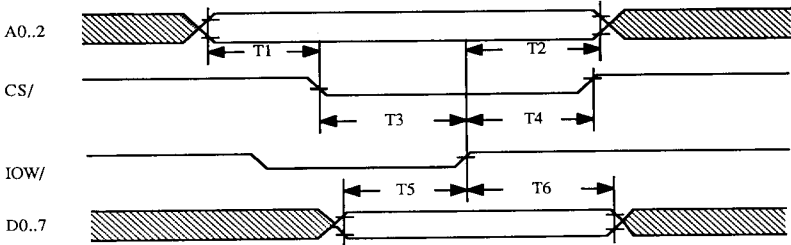
A0-A2, CS/, DACK/, EOP/, IOR/, IOW/, RESET/, SINGLE

<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>	<u>CONDITIONS</u>
V _{IH}	Input High Voltage	2.0	VDD + 0.5	V	
V _{IH}	Input High Voltage (53C80 AC testing only)	2.2	VDD + 0.5	V	
V _{IH}	Input High Voltage (53C80-40 AC testing only)	2.4	VDD + 0.5	V	
V _{IL}	Input Low Voltage	VSS - 0.5	0.8	V	
I _{IH}	Input High Leakage		10	μA	V _{IH} = 5.25V

IIL	Input Low Leakage		-10	μ A	VIL = VSS
DRQ, IRQ, READY, ARB, BSYOUT/, DBEN/, IGS, RSTOUT/, SELOUT/, TGS					
<u>SYMBOL</u>	<u>PARAMETER</u>	<u>MIN</u>	<u>MAX</u>	<u>UNIT</u>	<u>CONDITIONS</u>
VOH	Output High Voltage	2.4	VDD	V	IOH = -4.0mA
VOL	Output Low Voltage	VSS	0.4	V	IOL = 8.0mA
IOH	Output High Current	-4.0		mA	VOH = VDD-0.5V
IOL	Output Low Current	8.0		mA	VOL = 0.4V

TIMING DIAGRAMS

CPU WRITE

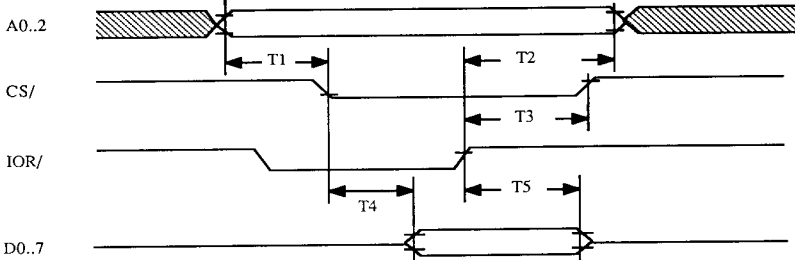


53C80 53C81 5380/81 53C80-40

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	Address setup to write enable*	10		10		20		10		ns
T2	Address hold from end write enable*	10		0		20		10		ns
T3	Write enable width*	40		40		70		40		ns
T4	Chip select hold from end of IOW/	0		0		0		0		ns
T5	Data setup to end of write enable*	20		20		50		20		ns
T6	Data hold time from end of IOW/	20		30		30		30		ns

* Write enable is the occurrence of both IOW/ and CS/.

CPU READ



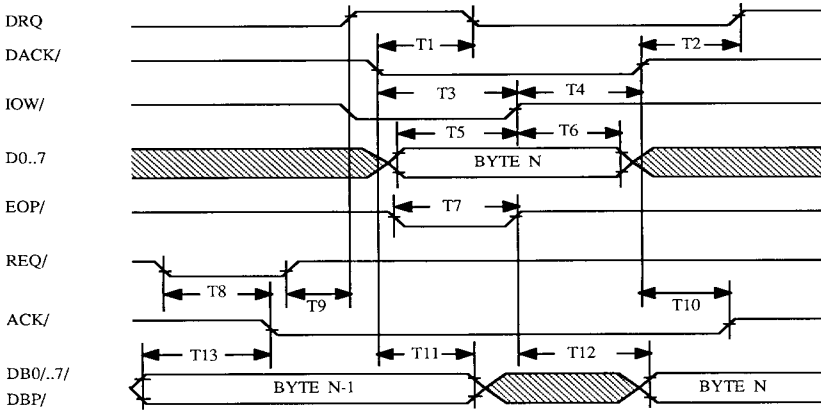
53C80 53C81 5380/81 53C80-40

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	Address setup to read enable*	10		10		20		10		ns
T2	Address hold from end read enable*	10		0		20		10		ns
T3	Chip select hold from end of IOR/	0		0		0		0		ns
T4	Data access time from read enable*		70		100		130		100	ns
T5	Data tri-state time from end of IOR/	10		20		20		10		ns

* Read enable is the occurrence of both IOR/ and CS/.

DMA WRITE (NON-BLOCK MODE) INITIATOR SEND

(Except for the 53C80-40)



53C80

53C81

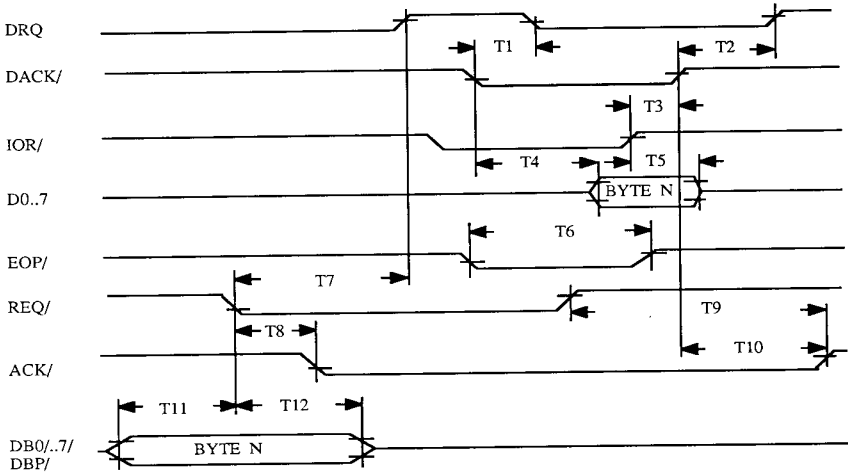
5380/81

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	DRQ false from DACK/ true		60		100		130	ns
T2	DACK/ false to DRQ true	30		30		30		ns
T3	Write enable width*	50		70		100		ns
T4	DACK/ hold from end of IOW/	0		0		0		ns
T5	Data setup to end of write enable*	50		50		50		ns
T6	Data hold time from end of IOW/	25		40		40		ns
T7	Width of EOP/ pulse (see note)	50		70		100		ns
T8	REQ/ true to ACK/ true		70		110		160	ns
T9	REQ/ false to DRQ true		70		110		110	ns
T10	DACK/ false to ACK/ false		90		130		150	ns
T11	Data hold from write enable*	15		15		15		ns
T12	IOW/ false to valid SCSI data		50		100		100	ns
T13	Data setup to ACK/ true	55		55		55		ns

* Write enable is the occurrence of both IOW/ and DACK/.
 Note: EOP/, IOW/, and DACK/ must be concurrently true for at least T7 for proper recognition of the EOP/ pulse.

DMA READ (NON-BLOCK MODE) INITIATOR RECEIVE

(Except for the 53C80-40)

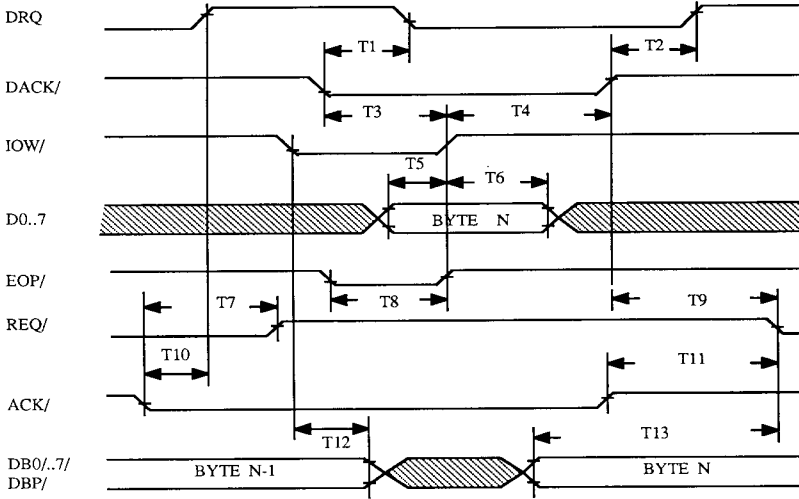


53C80 53C81 5380/81

NAME	DESCRIPTION	MIN	MAX	MIN	MA	MIN	MAX	UNIT
T1	DRQ false from DACK/ true		60		100		130	ns
T2	DACK/ false to DRQ true	30		30		30		ns
T3	DACK/ hold time from end of IOR/	0		0		0		ns
T4	Data access time from read enable*		70		100		115	ns
T5	Data hold time from end of IOR/	10		20		20		ns
T6	Width of EOP/ pulse (see note)	50		70		100		ns
T7	REQ/ true to DRQ true		70		140		150	ns
T8	REQ/ true to ACK/ true		70		115		160	ns
T9	REQ/ false to ACK/ false (DACK/ false)		80		100		140	ns
T10	DACK/ false to ACK/ false (REQ/ false)		90		100		160	ns
T11	DATA setup time to REQ/	20		20		20		ns
T12	DATA hold time from REQ/ true	50		50		50		ns

* Read enable is the occurrence of both IOR/ and DACK/.
 Note: EOP/, IOR/ and DACK/ must be concurrently true for at least T6 for proper recognition of the EOP/ pulse.

DMA WRITE (NON-BLOCK MODE) TARGET SEND

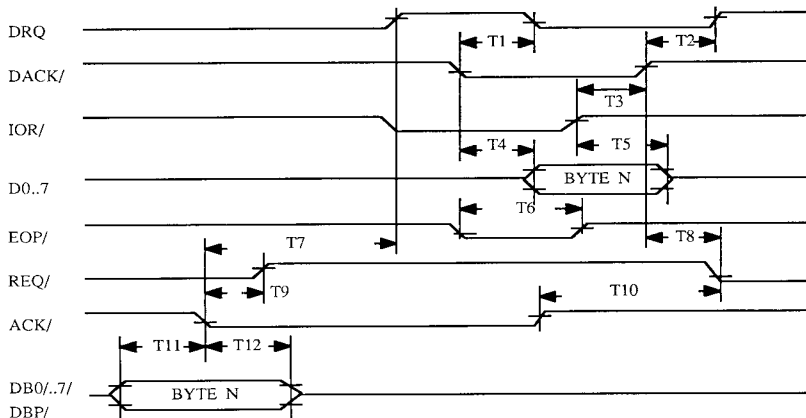


53C80 53C81 5380/81 53C80-40

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	DRQ false from DACK/ true		60		100		130		60	ns
T2	DACK/ false to DRQ true	30		30		30		30		ns
T3	Write enable width *	50		70		100		50		ns
T4	DACK/ hold from end of IOW/	0		0		0		0		ns
T5	Data setup to end of write enable *	50		50		50		50		ns
T6	Data hold time from end of IOW/	25		40		40		25		ns
T7	ACK/ true to REQ/ false		80		125		125		80	ns
T8	Width of EOP/ pulse (see note)	50		70		100		50		ns
T9	REQ/ from end of DACK/ (ACK/ false)		90		130		150		100	ns
T10	ACK/ true to DRQ true (target)		70		110		110		70	ns
T11	ACK/ false to REQ/ true (DACK/ false)		100		130		150		110	ns
T12	Data hold from write enable	15		15		15		15		ns
T13	Data setup to REQ/ true (target)	55		55		60		55		ns

* Write enable is the occurrence of IOW/ and DACK/.
 Note: EOP/, IOW/, and DACK/ must be concurrently true for at least T8 for proper recognition of the EOP/ pulse.

DMA READ (NON-BLOCK MODE) TARGET RECEIVE

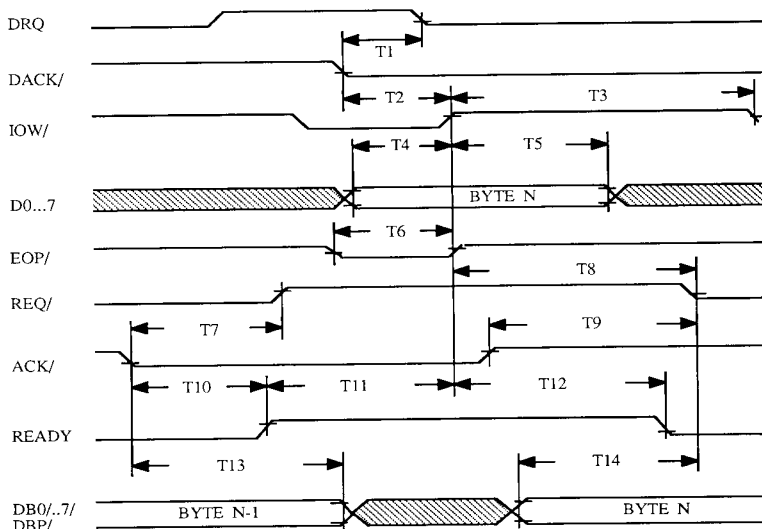


53C80 53C81 5380/81 53C80-40

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	DRQ false from DACK/ true		60		100		130		60	ns
T2	DACK/ false to DRQ true	30		30		30		30		ns
T3	DACK/ hold time from end of IOR/	0		0		0		0		ns
T4	Data access time from read enable*		70		100		115		100	ns
T5	Data hold time from end of IOR/	10		20		20		10		ns
T6	Width of EOP/ pulse (see note)	50		70		100		50		ns
T7	ACK/ true to DRQ true		70		110		110		70	ns
T8	DACK/ false to REQ/ true (ACK/ false)		90		120		150		110	ns
T9	ACK/ true to REQ/ false		80		125		125		80	ns
T10	ACK/ false to REQ/ true (DACK/ false)		100		120		150		110	ns
T11	DATA setup time to ACK/	20		20		20		20		ns
T12	DATA hold time from ACK/ true	30		50		50		50		ns

* Read enable is the occurrence of both IOR/ and DACK/.
 Note: EOP/, IOR/ and DACK/ must be concurrently true for at least T6 for proper recognition of the EOP/ pulse.

DMA WRITE (BLOCK MODE) TARGET SEND

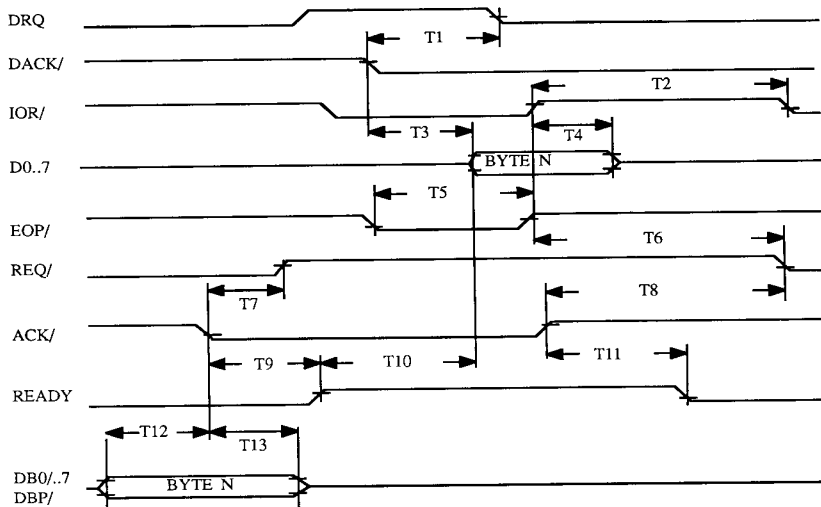


53C80 53C81 5380/81 53C80-40

NAME	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
T1	DRQ false from DACK/ true		60	80	100	100	130	50	60	ns
T2	Write enable width*	50		80		100		50		ns
T3	Write recovery time	120		120		120		120		ns
T4	Data setup to end of write enable*	50		50		50		50		ns
T5	Data hold time from end of IOW/	25		40		40		30		ns
T6	Width of EOP/ pulse (see note)	50		70		100		50		ns
T7	ACK/ true to REQ/ false		80		125		125		90	ns
T8	REQ/ from end of IOW/ (ACK/ false)		90		130		180		110	ns
T9	REQ/ from end of ACK/ (IOW/ false)		100		110		170		100	ns
T10	ACK/ true to READY true		70		140		140		85	ns
T11	READY true to IOW/ false	70		70		70		70		ns
T12	IOW/ false to READY false		70		120		140		80	ns
T13	DATA hold from ACK/ true	40		40		40		40		ns
T14	Data setup to REQ/ true	55		55		60		55		ns

* Write enable is the occurrence of both IOW/ and DACK/.
 Note: EOP/, IOW/, and DACK/ must be concurrently true for at least T6 for proper recognition of the EOP/ pulse.

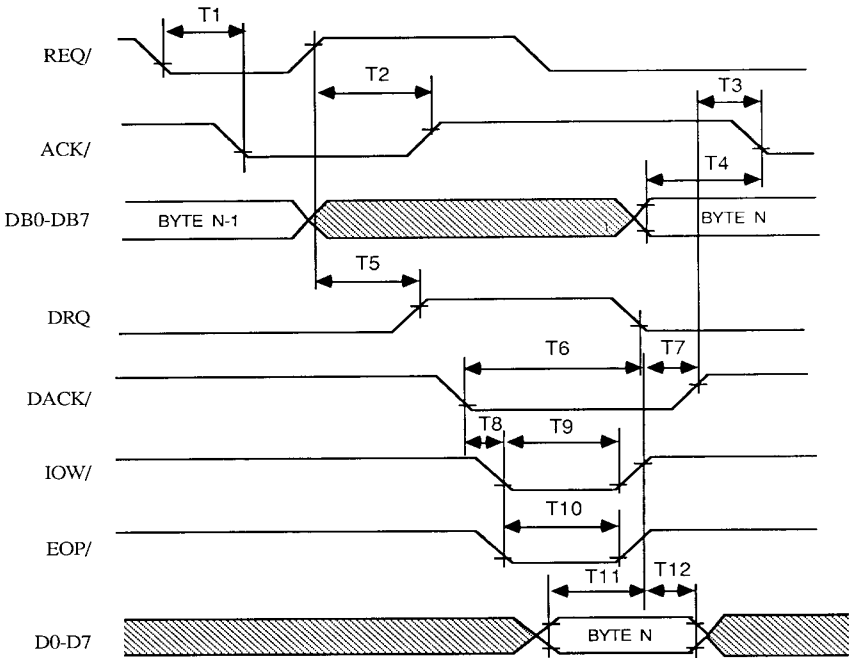
DMA READ (BLOCK MODE) TARGET RECEIVE



NAME	DESCRIPTION	53C80		53C81		5380/81		53C80-40		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T1	DRQ false from DACK/ true		60		100		130		60	ns
T2	IOR/ recovery time	120		120		120		120		ns
T3	Data access time from read enable*		70		100		110		100	ns
T4	Data hold time from end of IOR/	10		20		20		10		ns
T5	Width of EOP/ pulse (see note)	50		70		100		50		ns
T6	IOR/ false to REQ/ true (ACK/ false)		90		130		190		110	ns
T7	ACK/ true to REQ/ false		80		125		125		90	ns
T8	ACK/ false to REQ/ true (IOR/ false)		100		110		170		100	ns
T9	ACK/ true to READY true		70		140		140		80	ns
T10	READY true to valid data		50		50		50		50	ns
T11	IOR/ false to READY false		70		120		140		80	ns
T12	DATA setup time to ACK/	20		20		20		20		ns
T13	DATA hold time from ACK/	30		50		50		30		ns

* Read enable is the occurrence of both IOR/ and DACK/.
 Note: EOP/, IOR/, and DACK/ must be concurrently true for at least T5 for proper recognition of the EOP/ pulse.

53C80-40 DMA WRITE (NON-BLOCK MODE) INITIATOR SEND

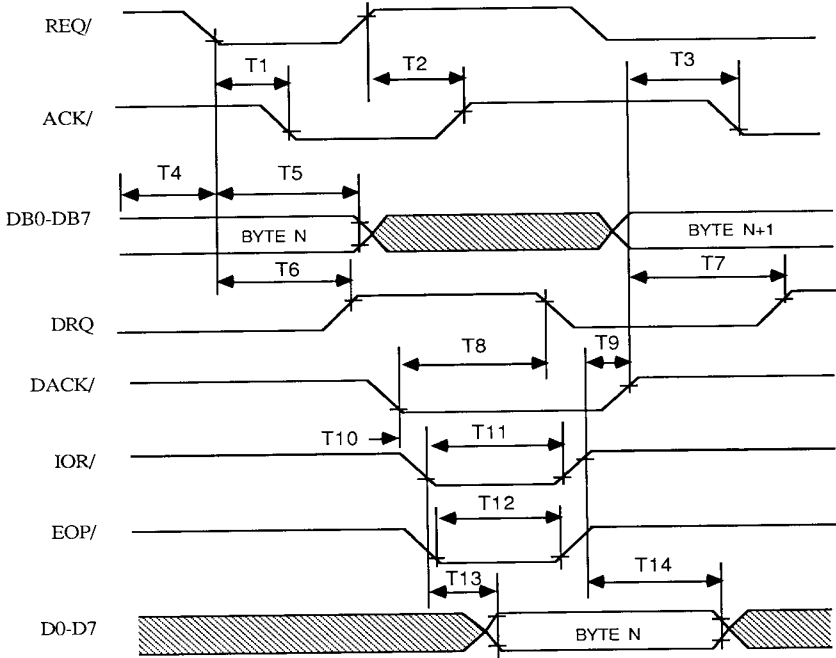


Name	Description	Min.	Max.	Unit
T1	REQ/ True to ACK/ True		95	ns
T2	REQ/ False to ACK/ False		75	ns
T3	DACK/ False to ACK/ True		115	ns
T4	Data Setup before ACK/ True	55		ns
T5	REQ/ False to DRQ True		75	ns
T6	DACK/ True to DRQ False		60	ns
T7	DACK/ Hold from IOW/ False	0		ns
T8	DACK/ True to IOW/ True	0		ns
T9	Write Enable Width*	50		ns
T10	EOP/ Pulse Width**	50		ns
T11	Data Setup to End of Write Enable	50		ns
T12	Data Hold after IOW/ False	25		ns

* Write Enable is the occurrence of IOW/ and DACK/.

** EOP/, IOW/, and DACK/ must be concurrently active for at least T10 for proper recognition of the EOP/ pulse

53C80-40 DMA READ (NON-BLOCK MODE) INITIATOR RECEIVE

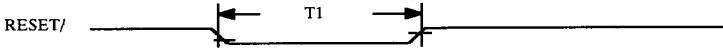


Name	Description	Min.	Max.	Unit
T1	REQ/ True to ACK/ True		95	ns
T2	REQ/ False to ACK/ False		75	ns
T3	DACK/ False to ACK/ True		115	ns
T4	Data Setup to REQ/ True	20		ns
T5	Data Hold after REQ/ True	50		ns
T6	REQ/ True to DRQ True		85	ns
T7	DACK/ False to DRQ True		100	ns
T8	DACK/ True to DRQ False		60	ns
T9	DACK/ Hold from IOR/ False	0		ns
T10	DACK/ True to IOR/ True	0		ns
T11	Read Enable Pulse Width*	100		ns
T12	EOP/ Pulse Width**	50		ns
T13	DMA Read Access Time		100	ns
T14	Data Hold from IOR/ False	10		ns

* Read Enable is the occurrence of IOR/ and DACK/.

** EOP/, IOR/, and DACK/ must be concurrently active for at least T12 for proper recognition of the EOP/ pulse

RESET

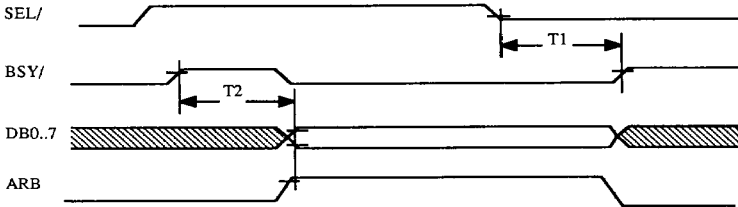


53C80/81 & 53C80-40

5380/81

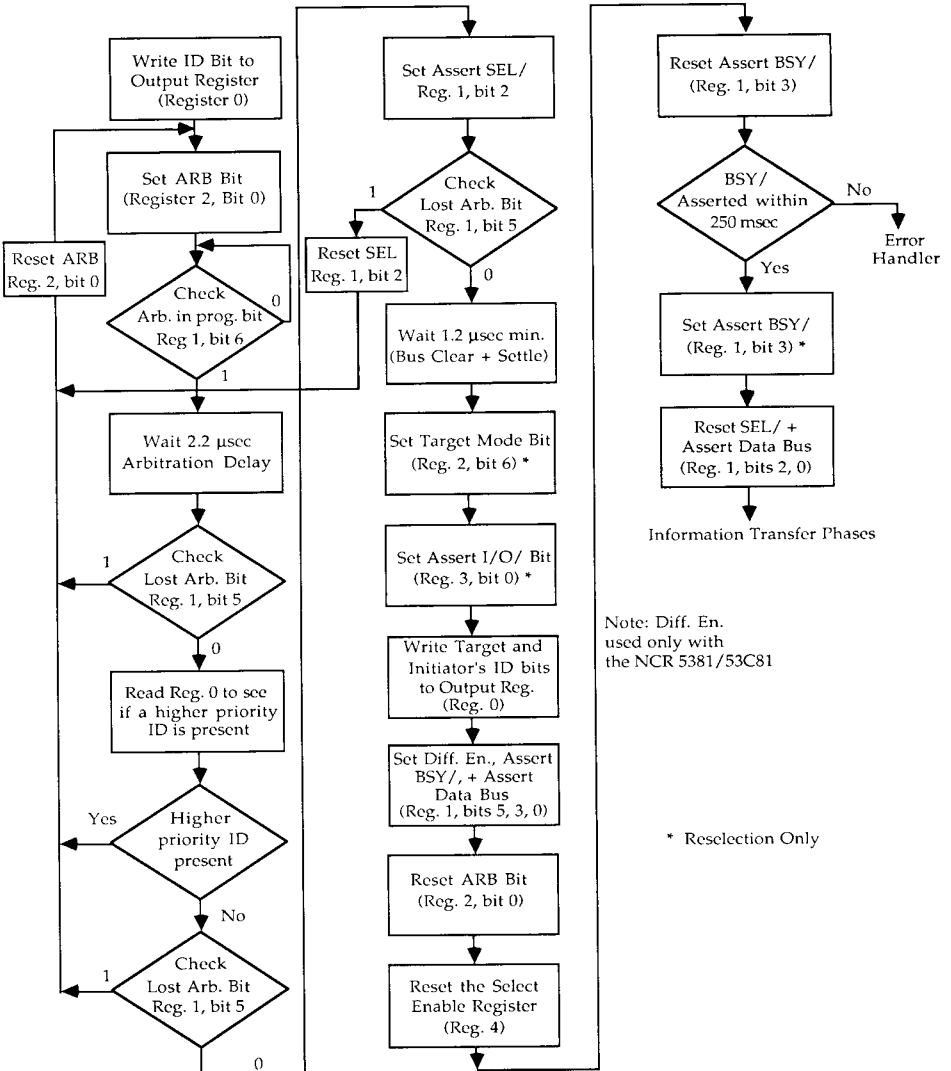
NAME	DESCRIPTION	MIN.	MAX.	UNIT	MIN.	MAX.	UNIT
T1	Minimum width of reset	100		ns	200		ns

ARBITRATION



NAME	DESCRIPTION	MIN	MAX	UNIT
T1	Bus clear from SEL true		600	ns
T2	ARBITRATE start from BSY false	1200	2200	ns

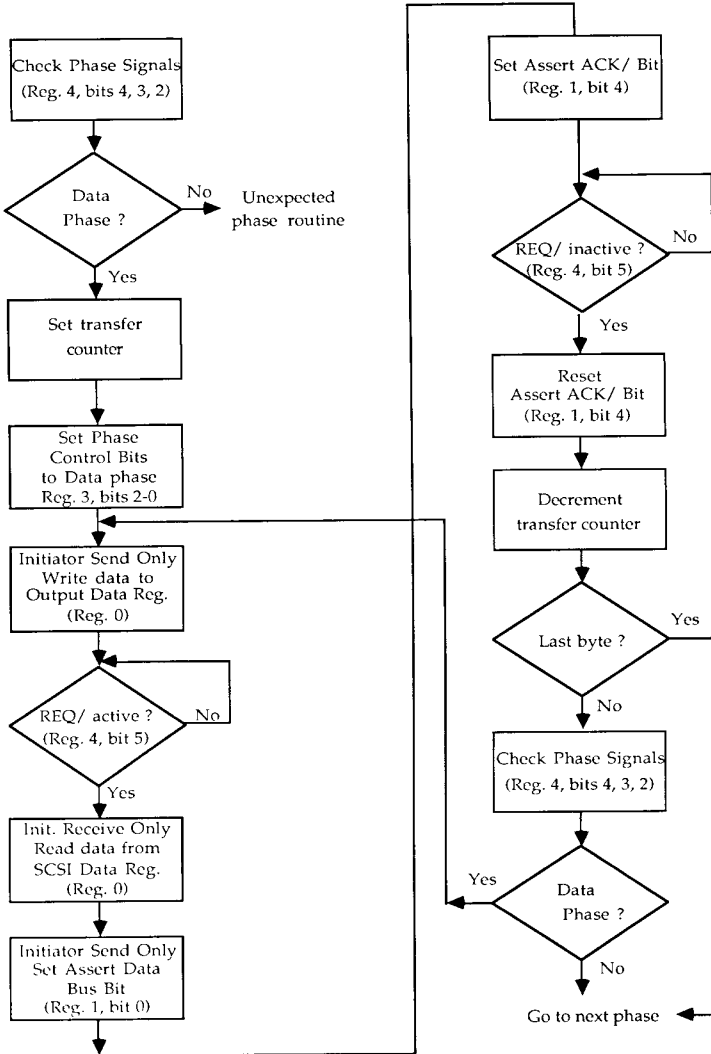
ARBITRATION AND SELECTION/RESELECTION



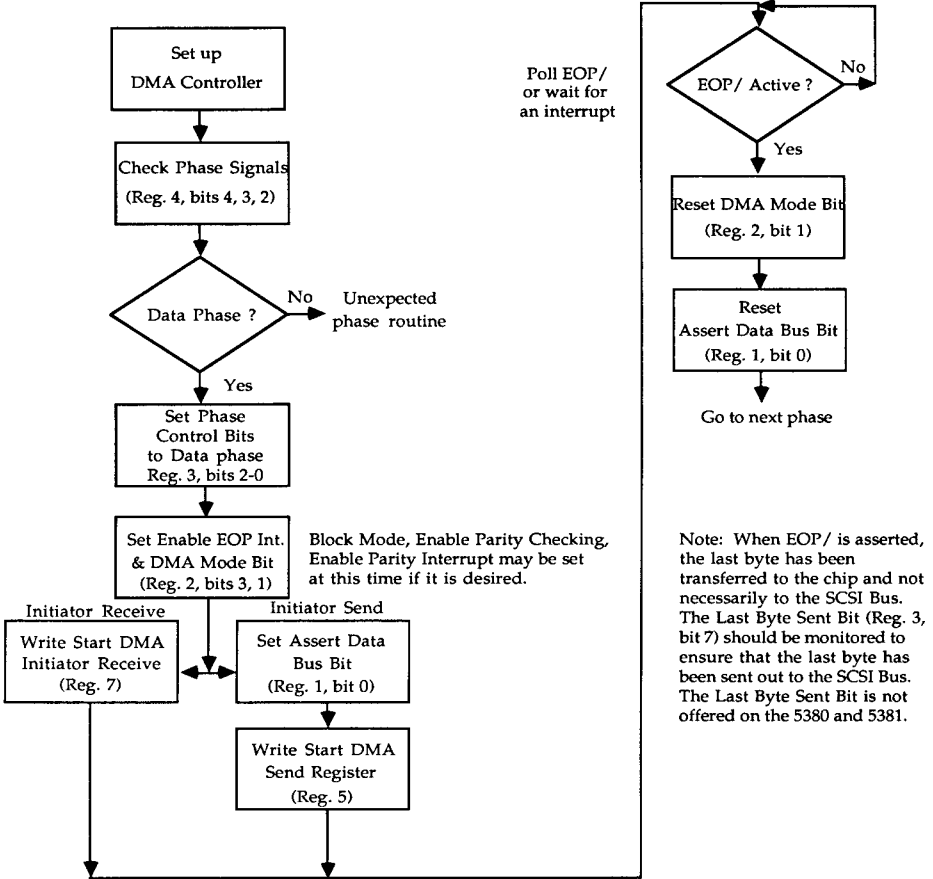
Note: Diff. En.
used only with
the NCR 5381/53C81

* Reselection Only

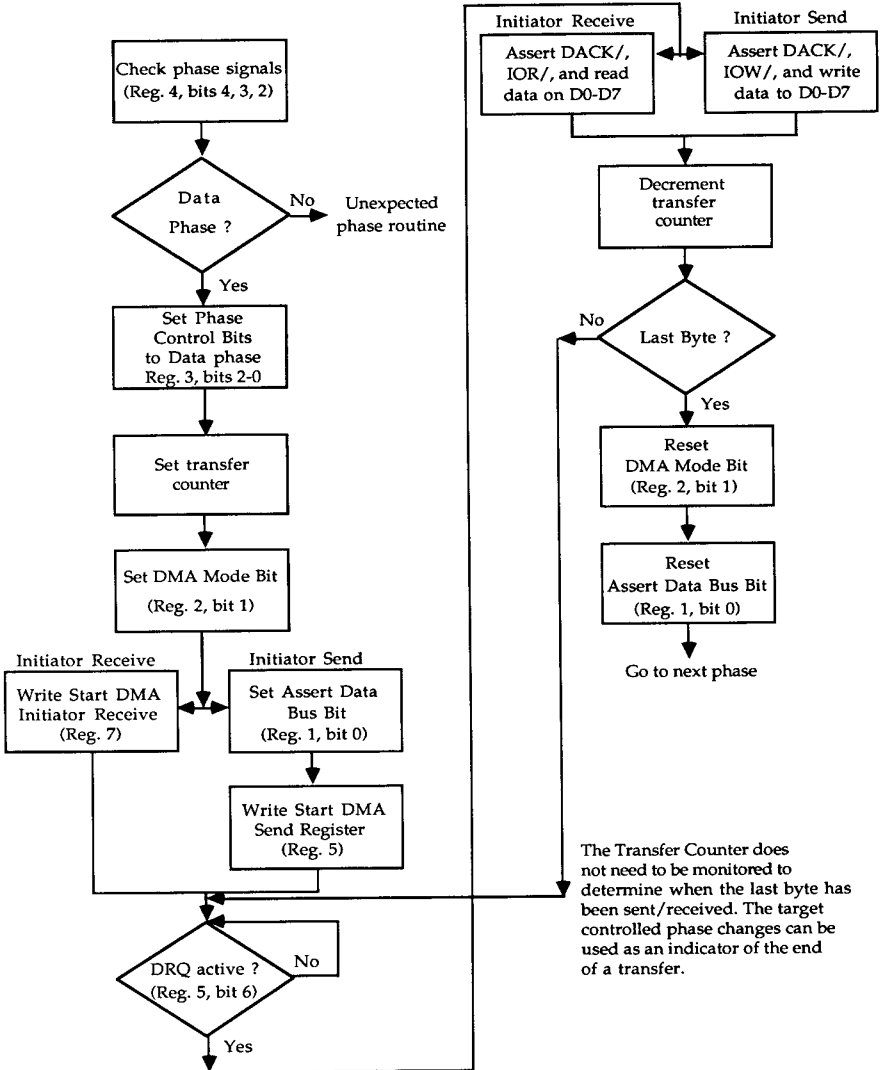
INITIATOR TRANSFERS - PROGRAMMED I/O



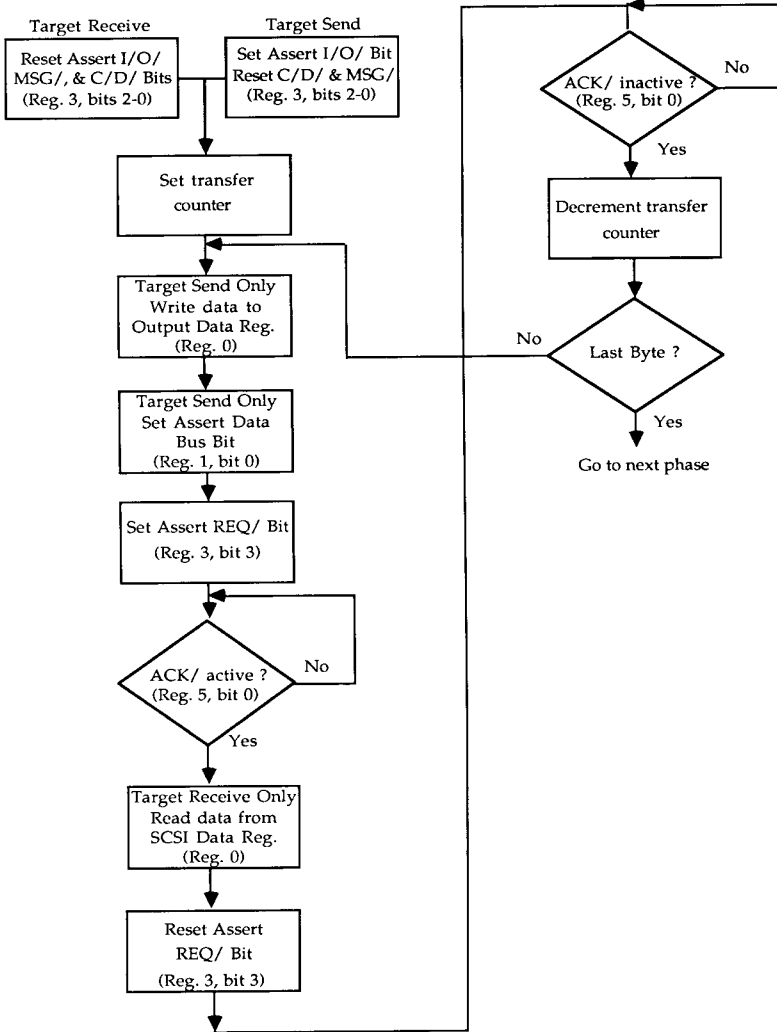
INITIATOR TRANSFERS - DMA MODE



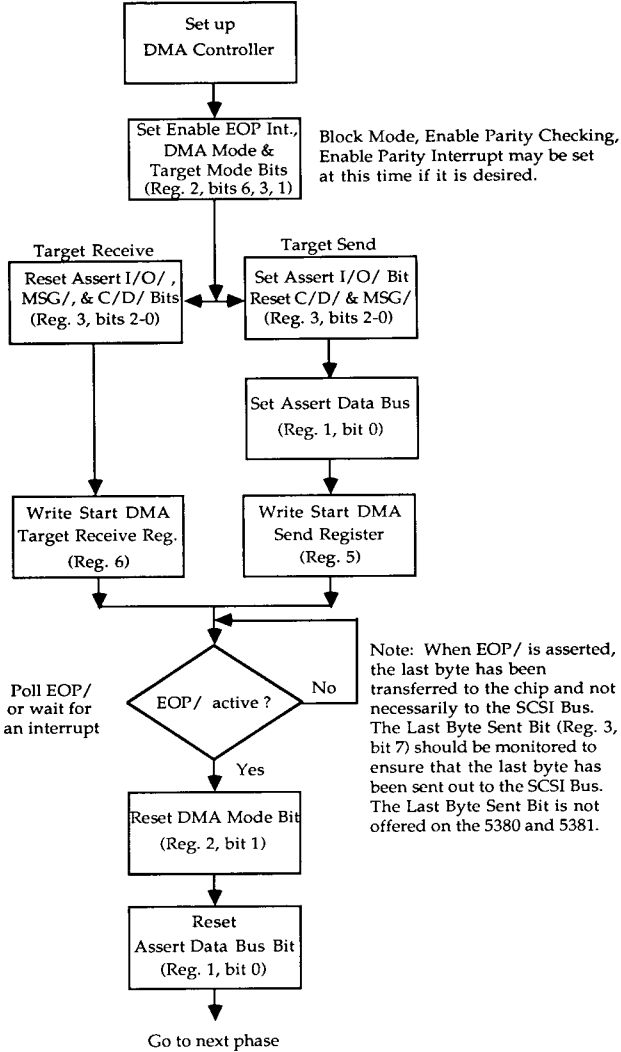
INITIATOR TRANSFERS - PSEUDO DMA



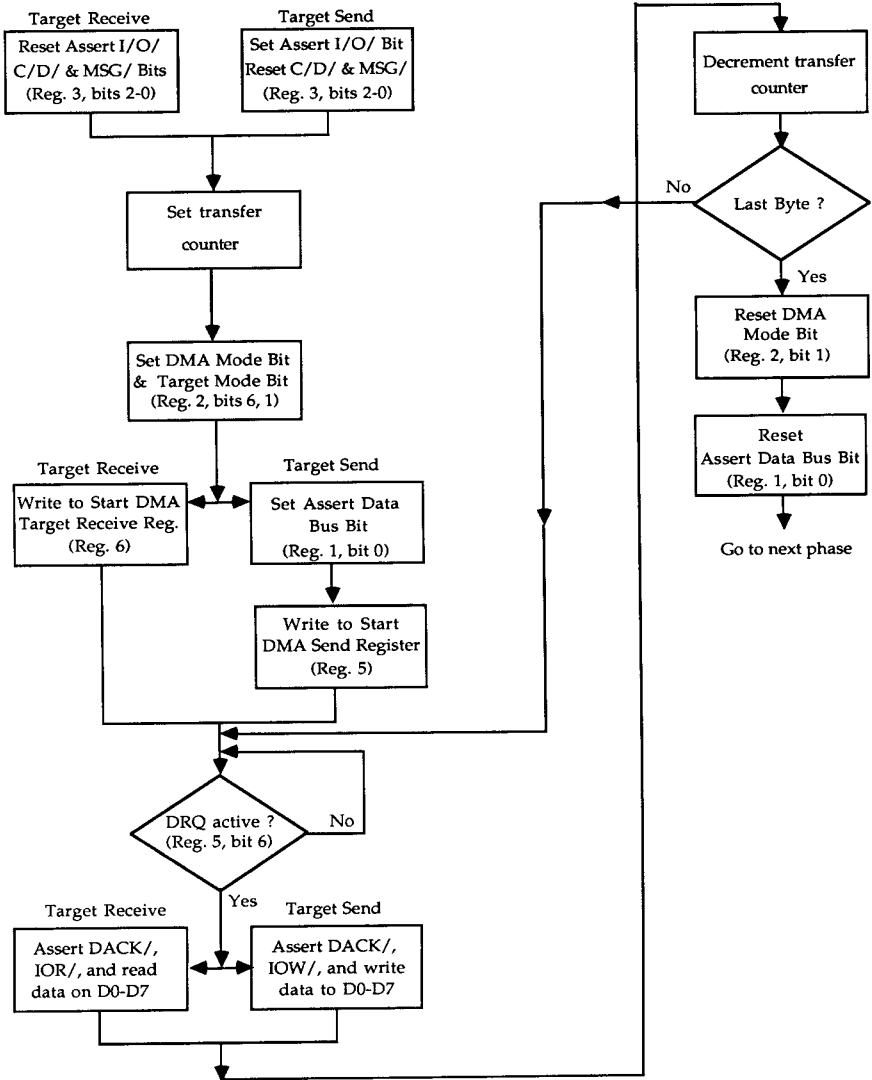
TARGET TRANSFERS - PROGRAMMED I/O



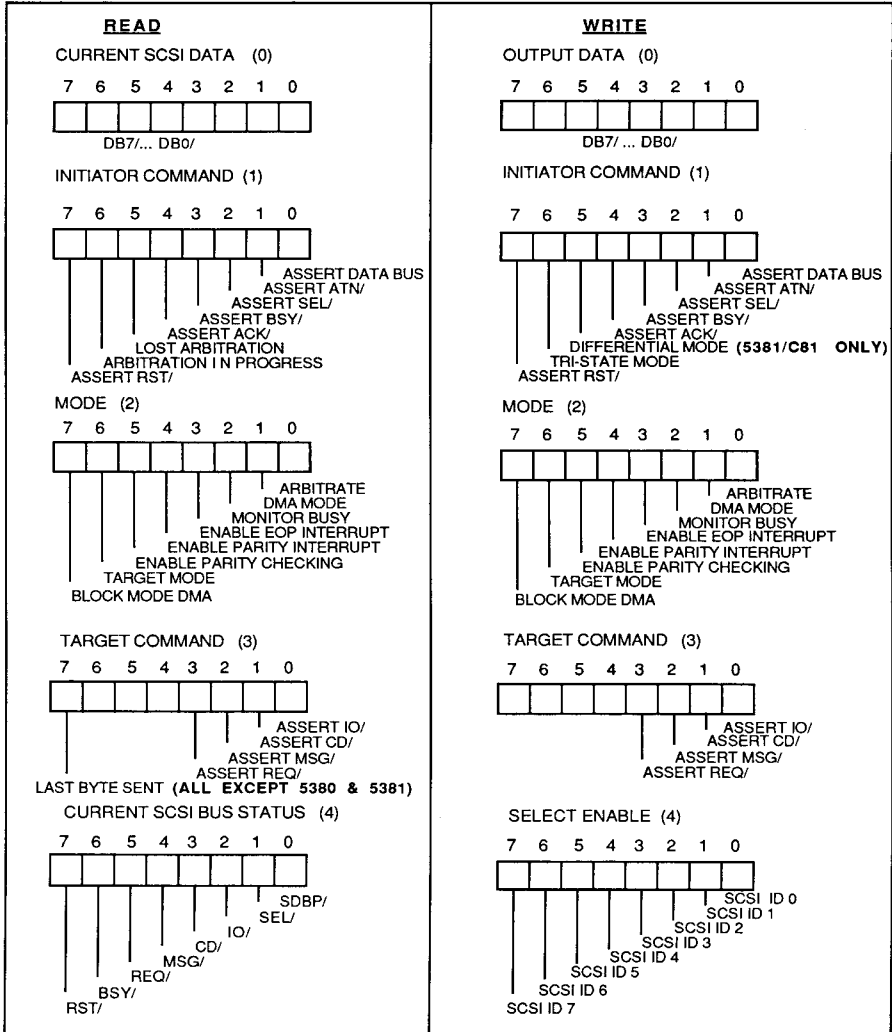
TARGET TRANSFERS - DMA MODE



TARGET TRANSFERS - PSEUDO DMA



REGISTER SUMMARY



REGISTER SUMMARY CONT'D

READ								WRITE							
BUS AND STATUS (5)								START DMA SEND (5)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
								X	X	X	X	X	X	X	X
ACK/ ATN/ BUSY ERROR PHASE MATCH INTERRUPT REQUEST ACTIVE PARITY ERROR DMA REQUEST END OF DMA TRANSFER															
INPUT DATA (6)								START DMA TARGET RECEIVE (6)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
								X	X	X	X	X	X	X	X
DB7/ ... DB0/															
RESET PARITY / INTERRUPT (7)								START DMA INITIATOR RECEIVE (7)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = DON'T CARE

Appendix A
Differences in the NCR 5380 Family

The different 5380/53C80 SCSI chips can be easily identified by the ten digit part number which is marked on every device and is unique to the specific part's process and package.

<u>Part</u>	<u>Package</u>	<u>Part Number</u>
5380	40 pin DIP	006-1082073
53C80-40	40 pin DIP	609-3400389
5380	44 pin PLCC	609-3400246
53C80-40	44 pin PLCC	609-3400456
3 μ m 53C80	44 pin PLCC	609-3400257
2 μ m 53C80	44 pin PLCC	609-3400443
3 μ m 53C80	48 pin DIP	609-3400276
2 μ m 53C80	48 pin DIP	609-3400359

2 μ m 53C80 vs. 3 μ m 53C80:

The 2 μ m 53C80 is a pin compatible replacement for the 3 μ m 53C80. It is manufactured using a faster process, thus allowing better margin on timing specs and requiring no modifications to current designs.

Differences between the 2 μ m 53C80 and the 3 μ m 53C80:

	<u>2μm 53C80</u>	<u>3μm 53C80</u>
process:	2 μ m DLM(double level metal) CMOS	3 μ m CMOS
function:	Voltage feedthrough has been eliminated due to the removal of the protection diodes. The diodes provided a path between the SCSI pin and VDD which caused the SCSI bus levels to be lowered when the chip was powered down. This is a common problem with CMOS IC designs and has been eliminated in the 2 μ m version.	
AC char:	This process is inherently faster allowing more margin on timing specs. Designs using 3 μ m CMOS timings will work with the 2 μ m version. The improved timings have been documented in the data sheet. The exceptions are noted in the following:	
	CPU Write and Read: Address hold time, T2 = 10ns The address must be held longer in the 2 μ m 53C80 than for the 3 μ m 53C80. Designs which do not hold the address will not be compatible with the 2 μ m version.	CPU Write and Read: address hold time, T2 = 0ns
	Data reads, DMA or PIO: data hold time, T5 = 10ns This means the data is held for less time after a read from the host computer.	Data reads, DMA and PIO: data hold time, T5 = 20ns
DC char:	VIH = 2.2V Due to noise margin of the testers, VIH has been relaxed for all inputs.	VIH = 2.0V

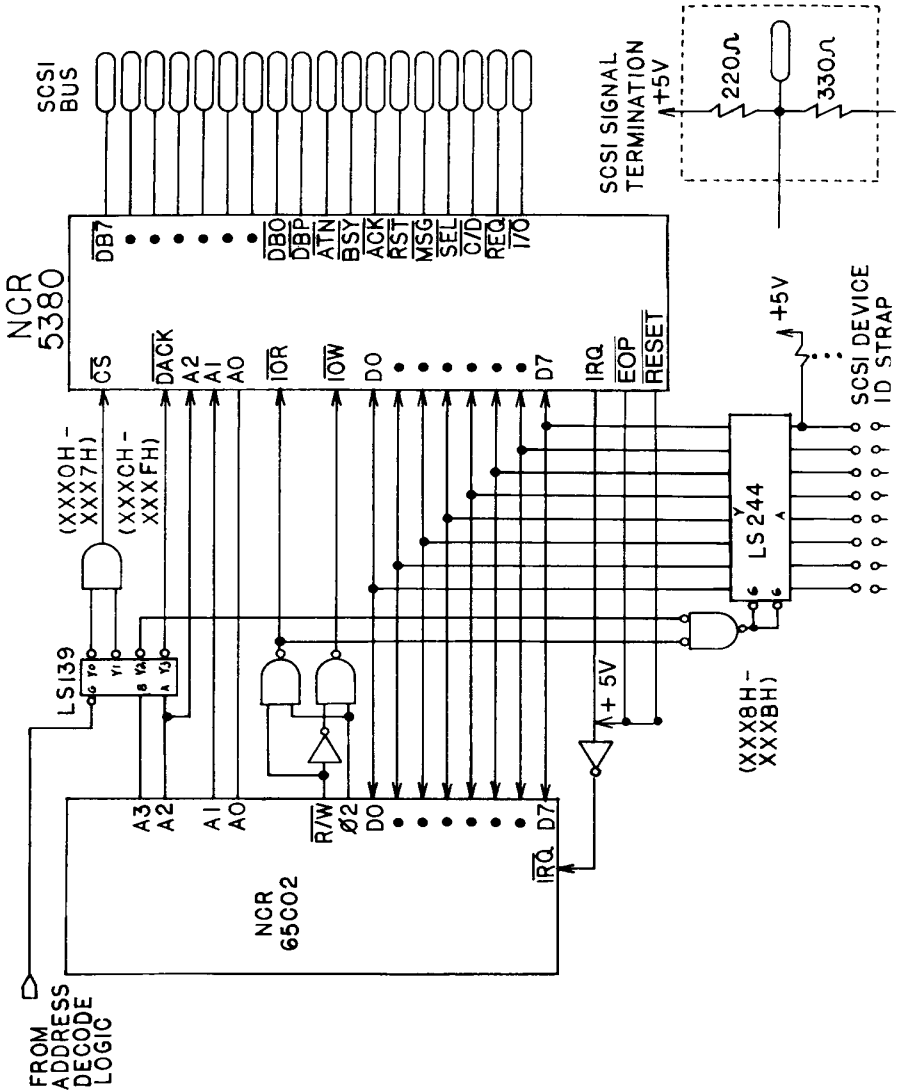
53C80-40 vs. 5380:

The 53C80-40 is a pin compatible CMOS replacement for the NMOS 5380. It is targeted for customers who have designed in a NMOS 5380 and wish to replace it with a lower cost CMOS version without having to alter their system firmware or hardware.

Differences between the 53C80-40 and the 5380:

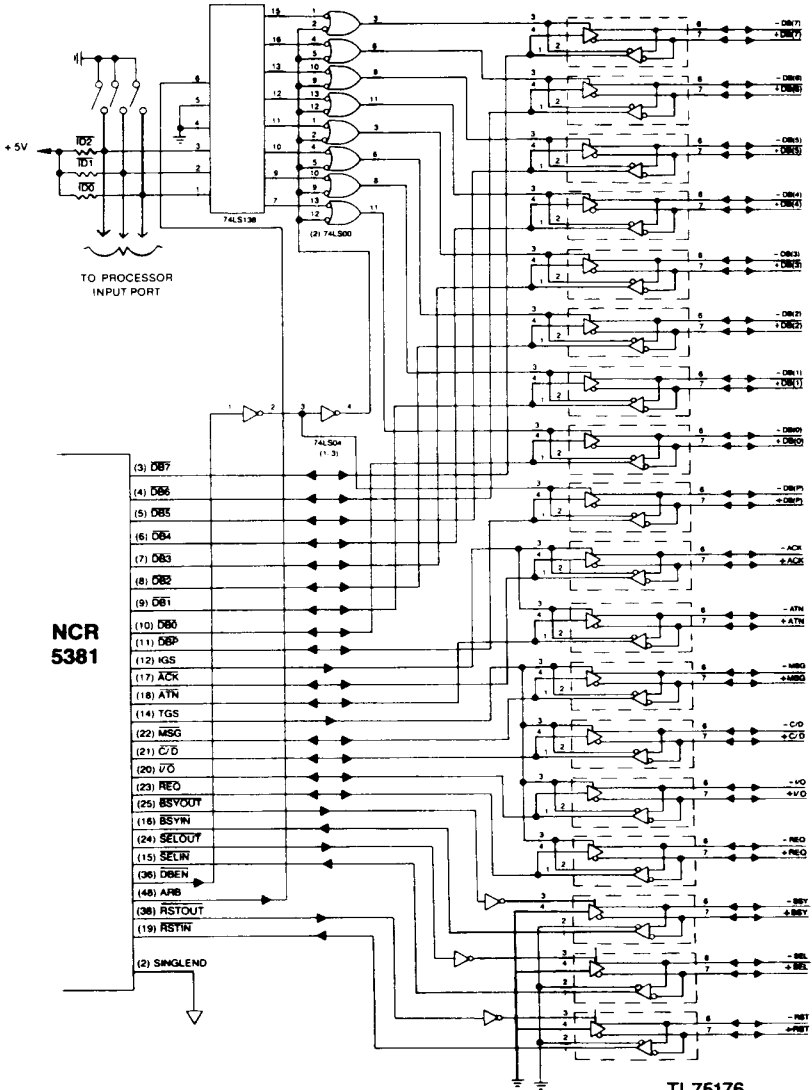
<u>53C80-40</u>	<u>5380</u>
process: 2 μ m DLM(double level metal) CMOS	3 μ m NMOS
function: The Last Byte Sent Bit has been added as bit 7 in the Target Command Register(register 3). This bit is set when the last byte has been sent across the SCSI bus after an EOP/ signal during a DMA write. This bit can be masked off to retain software compatibility.	Because there is no Last Byte Sent Bit in the 5380, the last REQ/, ACK/ handshake must be monitored after an EOP/ to ensure the last byte has been sent across the SCSI bus during a DMA write.
An internal pull-up resistor has been added to the RST/ signal to prevent spurious interrupts when the SCSI bus is not terminated. Therefore, an external pull-up is not needed.	The 5380 needs an external pull-up resistor on the RST/ signal to prevent spurious interrupts from occurring due to the floating condition of a non-terminated SCSI bus.
AC char : Because CMOS is a faster process, there is more margin on timing specs. However, designs using 5380 timings will work with the 53C80-40. Some important timing differences are documented in the following:	
CPU READ: Data access time, T4 = 100ns. This means that data will be available faster for the host computer to read.	CPU READ: Data access time, T4 = 130ns
To speed up SCSI transfer rates, ACK/ is now released some time after REQ/ allowing REQ/ to go active earlier in the 53C80-40 than in the 5380.	The 5380 waits for DACK/ to become inactive before releasing ACK/. The ACK/ signal is active during the entire DMA handshake. The 53C80-40 eliminates this dependence.
DC char : IDD = 15mA Because of the CMOS process, max IDD is lower which reduces power consumption.	IDD = 145mA
VIH = 2.4V Due to noise margin of the testers, VIH has been relaxed for all inputs.	VIH = 2.0V

Appendix B
65C02 Interface Diagram



Appendix C

NCR 5381 Suggested Differential Pair Interface



NOTE: DB0-7, DBP, ACK, ATN, MSG, C/D, I/O, and REQ require pull-ups.

TI 75176
OR
NATIONAL
3695