Triple 8-bit DAC-MUX with Genlock PLL & Analog Color Key

Features

- Triple 8-bit DAC and buffers support up to 1280 x 1024 resolution
- On-chip genlock PLL regenerates pixel clock for video processor
- Programmable color key for analog RGB inputs
- Genlock & analog keying capability eliminates the need for VGA-Video feature connector
- High-speed multiplexing between digital and analog RGB signals
- 24-bit interface supports up to 16.7M colors
- Supports CCIR601 4:2:2 YCbCr input format
- Built in YUV-to-RGB color space conversion
- Analog RGB inputs with programmable attenuation
- 2's complement input capability on two channels
- Programmable brightness, contrast, and hue attributes for the digital input signals
- Programmable switching delay compensation
- Two-wire serial programming
- CMOS technology in 64-pin PQFP
- 5V supply

Description

Chrontel's CH8439 combines three 8-bit DACs, a YUV-to-RGB color space converter, high-speed analog multiplexers, analog input attenuators, video buffers, a genlock PLL, analog color key detector, and numerous programmable features in one integrated circuit.

The CH8439's high-speed analog multiplexer allows simultaneous display of video (digital RGB or YUV) with graphics (analog RGB), making the CH8439 ideal for video games, video editing, CD and PC video, and for applications requiring picture-in-picture capability.

The CH8439 provides a 24-bit digital interface, which supports both RGB and 4:2:2 YCbCr input formats. With the 4:2:2 YCbCr input format, a built-in color space converter translates YUV video information to RGB before mixing with the analog graphics input.

There are eighteen control registers, which provide access to video attribute control functions of contrast, hue, brightness, PLL divider value, and analog color key range. These functions are programmable via the two-wire serial interface pins.

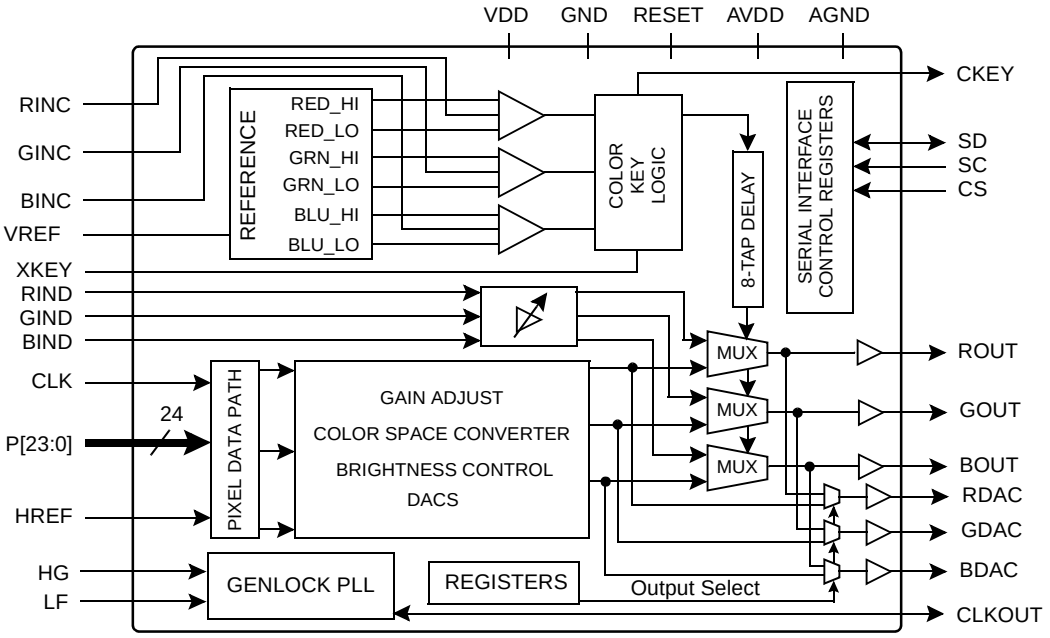

Figure 1: Block Diagram

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Pinout Diagram

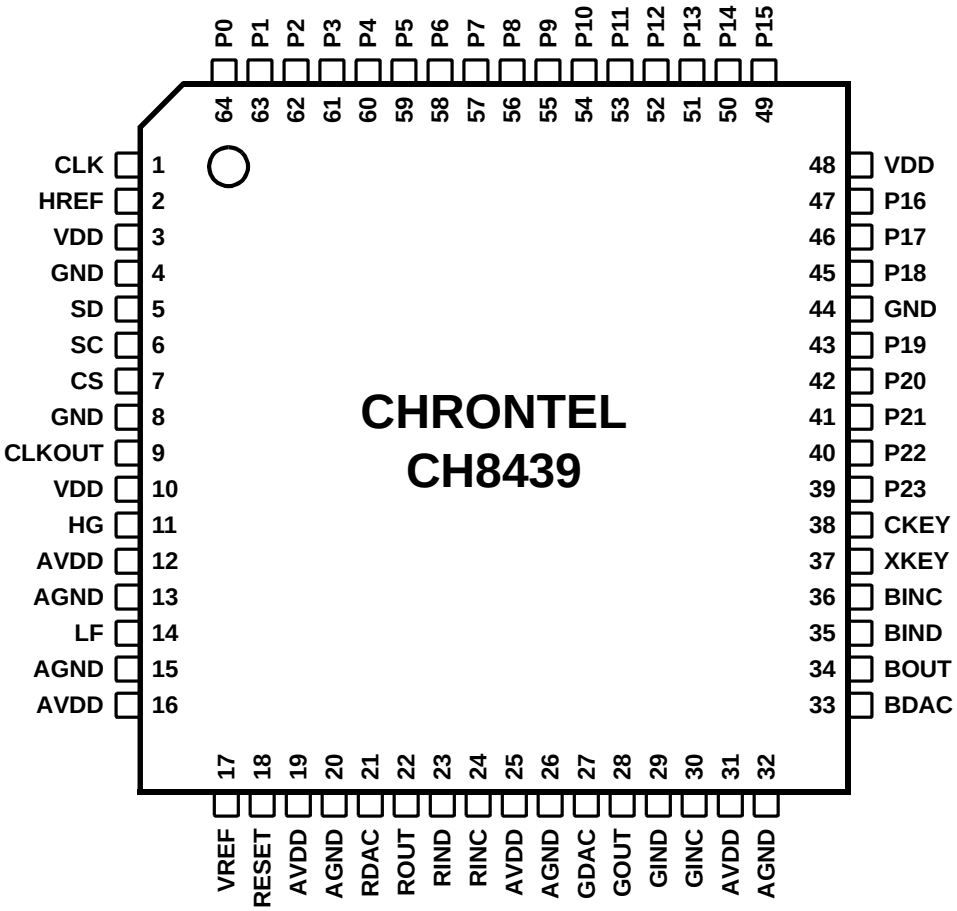


Figure 2: 64-pin PQFP

Table 1 • Pin Description

Symbol	Type	Pin #	Description
CLK	Input	1	**Digital Video Pixel Clock** The clock signal supplied from the video processor along with the 24-bit video pixel data, P[23:0].
HREF	Input	2	**Horizontal Reference** HREF is latched on the rising edge of CLK. The rising edge of CLK that latches the transition from low-to-high also latches the first set of data from P[23:0].
VDD	Power	3, 10, 48	**Digital Power Supply** These pins supply the positive 5V power to the digital circuits of the CH8439. Typically, a 0.1 µF decoupling capacitor should be attached to each of these power pins to ground. The decoupling capacitors should also be placed as close as possible to the power pins.
GND	Power	4, 8, 44	**Digital Ground** These pins provide the ground reference for the digital circuits of the CH8439.
SD	Input/Output	5	Serial Data Input (internal pull-up)
SC	Input	6	Serial Clock Input (internal pull-up)
CS	Input	7	**Chip Select** (active high, internal pull-down) Asserting this signal high enables the CH8439 serial programming interface.
CLKOUT	Input/Output	9	**Genlock PLL Clock Output** (default upon power-up) If register bit CT4 of the Comparator Adjustment register (R15) is set to 1, this pin can be used as an input for an external pixel clock source to provide the timing reference of the CH8439 on-chip comparators.
HG	Input	11	**Graphics Horizontal Sync Input** The input to this pin is typically the buffered version of the horizontal SYNC signal coming from the graphics card.
AVDD	Power	12, 16, 19, 25, 31	**Analog 5V supply** These pins supply the positive 5V power to the analog circuitry in the CH8439. Typically, a 0.1 µF decoupling capacitor should be attached to each of these power pins to ground. The decoupling capacitors should also be placed as close as possible to the power pins.
AGND	Power	13, 15, 20, 26, 32	**Analog ground** These pins provide the ground reference for the analog circuits of the CH8439.
LF	Input	14	**External Loop Filter** The external loop filter for the internal genlock PLL. A 3.7nF - 4.7nF ceramic capacitor should be attached between this pin and the analog ground. The capacitor should be placed as close as possible to the LF pin.
VREF	Input	17	**External Voltage Reference** Typically, a 0.1 µF capacitor should be attached between this pin and ground.
RESET	Input	18	**Chip Reset** (active high, internal pull-down) Asserting this signal high initializes the CH8439 serial interface and resets all registers into their power-on default states. The SD pin must be high during reset for proper initialization.
RDAC	Output	21	**Analog output, channel R DAC output** Red channel DAC output. The output to this pin can be programmed to be a duplicate of the output to the ROUT pin. For more information, please refer to Register R16 on page 31 for the description of this control.

Symbol	Type	Pin #	Description
ROUT	Output	22	**Analog output, channel R** The analog R or V output, consisting of a low-impedance, wide-bandwidth output buffer.
RIND	Input	23	**Auxiliary analog input, channel R** This pin is the input pin for the delayed version of the analog Red channel input, RINC.
RINC	Input	24	**Red analog color key detection input** This pin accepts the analog Red channel input used in detecting the Red color key color.
GDAC	Output	27	**Analog output, channel G DAC output** Green channel DAC output. The output to this pin can be programmed to be a duplicate of the output to the GOUT pin. For more information, please refer to Register R16 on page 31 for the description of this control.
GOUT	Output	28	**Analog output, channel G** The analog G or Y output, consisting of a low-impedance, wide-bandwidth output buffer.
GIND	Input	29	**Auxiliary analog input, channel G** This pin is the input pin for the delayed version of the analog Green channel input, GINC.
GINC	Input	30	**Green analog color key detection** This pin accepts the analog Green channel input used in detecting the Green color key color.
BDAC	Output	33	**Analog output, channel B DAC output** Blue channel DAC output. The output to this pin can be programmed to be a duplicate of the output to the BOUT pin. For more information, please refer to Register R16 on page 31 for the description of this control.
BOUT	Output	34	**Analog output, channel B** The analog B or U output, consisting of a low-impedance, wide-bandwidth output buffer.
BIND	Input	35	**Auxiliary analog input, channel B** This pin is the input pin for the delayed version of the analog Blue channel input, BINC.
BINC	Input	36	**Blue analog color key detection** This pin accepts the analog Blue channel input used in detecting the Blue color key color.
XKEY	Input	37	**External Keying Control** When XKEY = 0, graphics is being displayed. When XKEY = 1, color is being monitored. Video will be displayed if the color key is matched while XKEY=1.
CKEY	Output	38	**Color Key Detection Output** This pin can be programmed (Miscellaneous Control Register, R16) to reflect the state of the internal analog color key detection. If a color key match is detected, CKEY=1; if a color key match is not detected, CKEY=0.
P[23:19], P[18:16], P[15:0]	Input	39 – 43, 45 – 47, 49 – 64	**24-bit Digital Video Pixel Data Input** The input format to these bits can be programmed via the Digital Video Input Format Control register (R0). Upon power-up, 24-bit RGB is the default input format. For more information, please refer to **Table 5** on page 15 where all the digital video input format supported by the CH8439 are listed.

General Description

Analog Color Key

Analog color keying (along with the genlock PLL) is a critical feature that allows pull-down menu and cursor support in video/graphics overlay applications without the requirement of a feature connector. In general, a color key range must be defined for the R, G & B colors. When the auxiliary analog RGB inputs each fall within the specified color key range, respectively, the color key is considered to be matched. The external signal XKEY is used to control the display to switch from graphics to video. During the time at which XKEY=1, the analog RGB inputs are compared against the specified color key range. If a color key match is detected, video will be displayed. However if a color key mismatch is detected, the display is switched back immediately to graphics. In order to provide sufficient flexibility, the range of each of the R,G & B color key values are fully programmable (Please refer to the RGB color key upper and lower threshold registers, R7 - R12). Upon power up, the color key range registers are set such that the color key expected is magenta. Therefore, in this case, the color key from the graphics card should be set to magenta with Red = FF hex, Green = 00 hex, Blue = FF hex.

Genlock Phase Locked-Loop

A block diagram of the genlock PLL is shown in **Figure 3**. The genlock PLL consists of a phase detector, a charge pump, a loop filter, VCO, a feedback divider n, and an output divider k.

Using the On-Chip Feedback Divider

The on-chip feedback divider value is fully programmable through the PLL Control Registers I and II described on page 29. The on-chip divider can be used to define up to 13-bits for the feedback divider ratio. Two out of the 13 bits are used to select an output divider of value k=K+1, where K is the value of the two programming bits. The remaining 11 bits are used to program the “divide by n” counter as shown in **Figure 3**, whereby the feedback divider value n=N+2, with N being the value of the 11 programmable bits. The output of the “divide by n” counter is then genlocked with the graphics HSYNC signal from the graphics card.

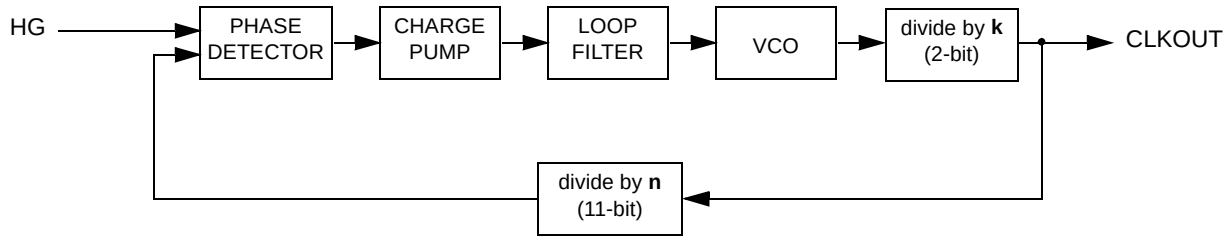


Figure 3: Genlock Phase-Locked Loop

Feedback Divider Values versus VCO Frequency Range

The on-chip VCO is designed to operate between 65 to 135 MHz for optimal performance. Therefore, the use of the output divider is required in order to generate frequencies lower than 65 MHz. For example, if the graphics mode selected is the Standard VGA mode (640x480 with 60Hz refresh, 800 pixels per horizontal line with horizontal frequency = 31.47 kHz), then the pixel clock frequency is 25.175 MHz. To generate this frequency and make it available at pin CLKOUT, a feedback divider value of 800x4 is desired giving a VCO running frequency of 800x4x31.47 kHz = 100.7 MHz. Hence, an output divider of 4 should be used to provide 25.175 MHz off-chip. In general, video system designers might want to confine the CLKOUT frequency to be less than 45 MHz due to memory speed issues. Sample frequencies and the register programming values are provided in **Tables 2** and **3** for reference.

Table 2 • Divider Values for Graphics Modes

Compatible Graphics Modes	VGA and MCGA			XGA-2's VGA Modes			Mac II, Quadra, or LC	VESA (72 Hz)	VESA (56 Hz)
Resolution	640x350	720x400	640x480	720x350	720x400	640x480	640x480	640x480	800x600
Horizontal Freq. (kHz)	31.469	31.469	31.469	39.444	39.444	39.375	35.000	37.860	35.156
Pixels/Horizontal Line	800	900	800	878	878	782	864	832	1024
Feedback Divider, n	800	900	800	878	878	782	864	832	1024
Output Divider, k	4	4	4	2	2	4	4	4	2
VCO Frequency (MHz) (65MHz < f_{VCO} < 135MHz)	100.7	113.3	100.7	69.3	69.3	123.1	121	126	72
CLKOUT Freq. (MHz) (f_{CLKOUT} <45 MhZ)	25.175	28.322	25.175	34.65	34.65	30.775	30.25	31.5	36
Regiter R13 (hex)†	33	33	33	13	13	33	33	33	13
Regiter R14 (hex)	1E	82	1E	6C	6C	0C	5E	3E	FE

Note: For more information on the programmable parameters of the genlock PLL, please refer to PLL Control Registers I and II (R13 and R14, respectively) described on page 29.

Table 3 • Divider Values for Graphics Modes (continued)

Compatible Graphics Modes	VESA (60 Hz)	VESA (72 Hz)	Mac II, Quadra	8514/A, XGA inter-laced	VESA (60 Hz)	VESA (70 Hz)	XGA -2 (75 Hz)	VESA (76 Hz)	VESA (60 Hz)	VESA (75 Hz)
Resolution	800x 600	800x 600	832x 624	1024x 768	1024x 768	1024x 768	1024x 768	1024x 768	1280x 1024	1280x 1024
Horizontal Freq. (kHz)	37.879	48.077	49.725	35.522	48.363	56.476	61.080	60.975	63.974	79.976
Pixels/Horizontal Line	1056	1040	1152	1264	1344	1328	1408	1312	1,696	1688
Feedback Divider, n	1056	520	576	1264	672	664	704	656	424	422
Output Divider, k	2	4	4	2	4	2	2	2	4	4
VCO Frequency (MHz) (65MHz < f_{VCO} < 135MHz)	80	100	114.57	89.8	130	75	86	80	108.5	135
CLKOUT Freq. (MHz) (f_{CLKOUT} <45 MhZ)	40	25	28.64	44.9	32.5	37.5	43	40	27.125	33.75
Regiter R13 (hex)†	14	32	32	14	32	12	12	12	31	31
Regiter R14 (hex)	1E	06	3E	EE	9E	96	BE	8E	A6	A4

Note: † The programming number N = n - 2, K = k - 1

Video Display Window and Graphics Window Alignment

The number of graphics pixels per horizontal line is a well defined number under standard VGA mode (640x480, 16-color). Unfortunately, this number is not standardized in super VGA modes. Therefore, if the feature connector is not used between the graphics card and the video card, the information regarding the graphics pixel clock frequency is not available to the video card. Hence, the video card firmware can only assume a certain number of pixels per line for a given super VGA mode which may not be exactly the same as the actual pixel clock rate of the graphics card. For this reason, the video display window cannot be perfectly aligned with the graphics window at which the video is supposed to be displayed. To eliminate this problem, the CH8439 makes available two possible solutions:

1. PLL Feedback Counter Adjustment

(A) A software utility can be designed to read the register value of the "Horizontal Total" from the VGA controller, where "Horizontal Total" represents the number of characters per line. Using this number and the criteria that the VCO frequency should be between 65MHz and 135 MHz, the value of the feedback counter can be set (Feedback Counter Value = "Horizontal Total" * C1 * C2, where C1 is the number of pixels per character (C1 = 8, typically) and C2 is the multiplication factor that would put the VCO frequency to fall within the desired range of operation). The frequency at output pin CLKOUT = GPCLK (the "Graphics Pixel Clock") when the output divider k is also set to the value C2.

(B) A software utility can be designed to allow the end user to adjust the default count for any given Super VGA modes by ± 25%. This would allow the user to fine tune the re-synthesized pixel clock frequency on the video card to match the actual graphics pixel rate.

2. Analog Color Key Controlled Switching

When the CH8439's high performance comparators detect the presence of the color key, the output signal CKEY will go high, and it will stay high as long as the presence of the color key is detected. Using the information given by signal CKEY, the video processor can generate a video display window with acceptable alignment to the graphics window.

Color Key Leak-Through Suppression

The color key can be detected only after the analog RGB signals have arrived at the inputs of the analog mux. However, the analog RGB signals at the analog mux inputs are displayed immediately at the color monitor. Therefore, the color key will be "leaked" through at the left hand edge of the switching transition between graphics and video, which may be acceptable for some applications. The CH8439 provides an optional solution to this issue for higher-end system products by including an additional set of analog RGB inputs. This allows system designers to allocate one set of RGB inputs for analog color key detection, while using the second set as inputs of a "delayed" version of the same signals. The amount of delay required would be in the range of 10 to 40ns using external wide-band analog delay lines. For systems not requiring the color key leak suppression, the two pairs of RGB inputs can simply be shorted together.

Genlock CLKOUT versus Horizontal and Vertical Sync Timing

It is important to control the timing relationship between the regenerated pixel clock CLKOUT and the graphics HSYNC and VSYNC signals. Chrontel's circuit technology allows the CH8439 to guarantee synchronization timing as shown in **Figure 4**. Hence, system designers can use the rising edge of CLKOUT to latch the HSYNC and VSYNC signals. The possible synchronization metastable state (i.e., the rising clock edge aligns with the transition of the sync signal) is ***eliminated***, independent of the frequency of CLKOUT.

It is important to note that the falling edge of the graphics HSYNC pulse is assumed to be the leading edge. In cases where the polarity of the graphics HSYNC pulse is reversed, as it may be in certain super VGA modes, the CH8439 has the provision to invert the polarity of the incoming graphics HSYNC. This control is available through the register bit H_INV of the PLL Control Register I described on page 29.

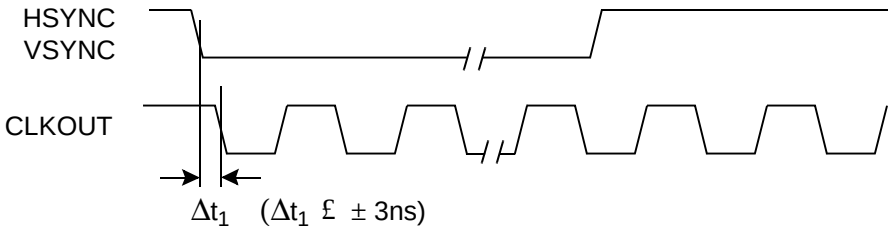


Figure 4: Synchronization Timing

Contrast and Hue Control

The digital input contrast and hue attributes can be controlled by adjusting the gain on each of the three 8-bit digital-to-analog converters. The R, G, and B (mode 0) or the Y, U, and V (modes 1 – 5) gains can be adjusted via the Digital Input Gain Control registers R4, R5, and R6, respectively. For more information on the controls available through these registers, please refer to refer to registers R4 through R6 on page 26.

Brightness Control

The digital RGB input brightness attribute can be controlled by introducing a DC offset to the output. The DC offset is programmable via the Digital Video Brightness Control register R3 described on page 25. **Figure 5** on page 12 shows an example of the analog output waveform with the programmable offset introduced.

Multiplexer Timing Control

The CH8439 provides an 8-tap delay line for the multiplexer switch control signal XKEY, with each tap offering a nominal 5 ns delay. The delay control allows adjustment of the sub-pixel alignment between the video signal coming from the digital interface, and the graphics signal coming from the analog RGB inputs. The tap select is controlled by the multiplexer delay select control bits MDS[2:0] of the Multiplexer Delay Control register R2 described on page 25.

Auxiliary Analog Input Attenuation

Due to possible variations of analog RGB input levels, the CH8439 provides an analog input attenuation control that allows the inputs to be gain-scaled to the appropriate levels. The four levels of attenuation are programmable through the Analog Input Attenuation Control register R1 described on page 24. It should be noted that the color key is compared against the analog RGB signals prior to the attenuation. **Figure 6** on page 13 and **Figure 7** on page 14 illustrate analog input and output waveforms with the input gain-scale set to one (i.e., no attenuation).

Analog Outputs

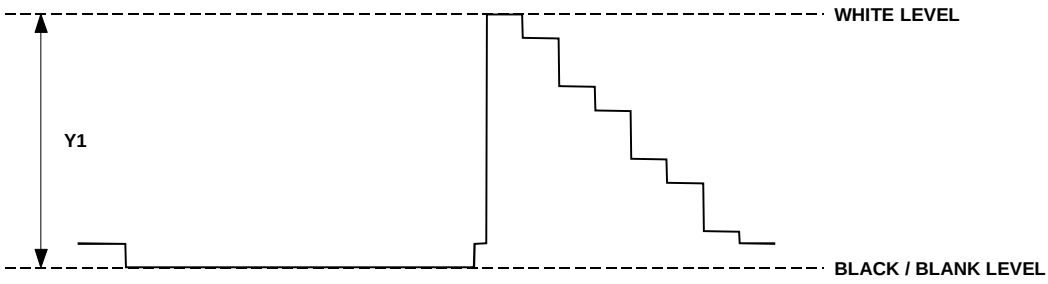
The analog RGB or YUV outputs consist of low impedance, wide-band output buffers designed to drive 75 Ω controlled impedance lines and 75 Ω-terminated color monitors. The default and maximum voltage levels at these outputs are shown in **Table 4** below.

Table 4 • Analog Output of Digital RGB Signal

Color/Level	Default Value (V)	Max Setting (V)†
White	0.66	0.970
Blank/Black	0.00	0.164

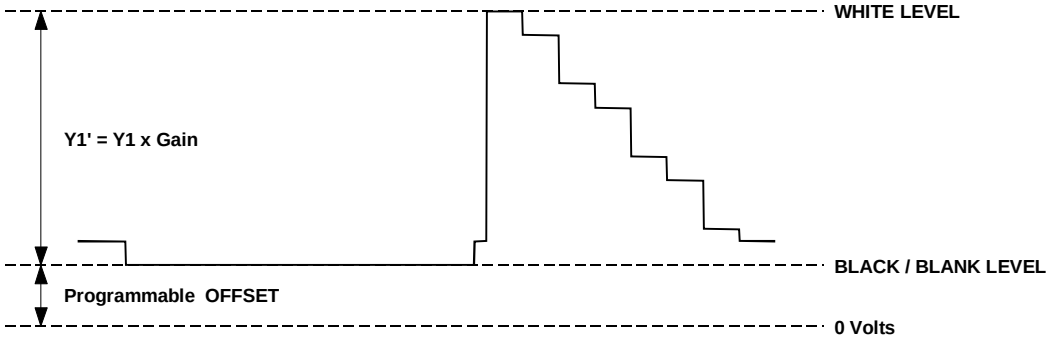
Note: † Digital input gain and brightness control registers are set at maximum settings

3(a) Internal DAC Output



Note: The D/A output shown is for a converted digital RGB input, with the D/A converter configured under the default setting

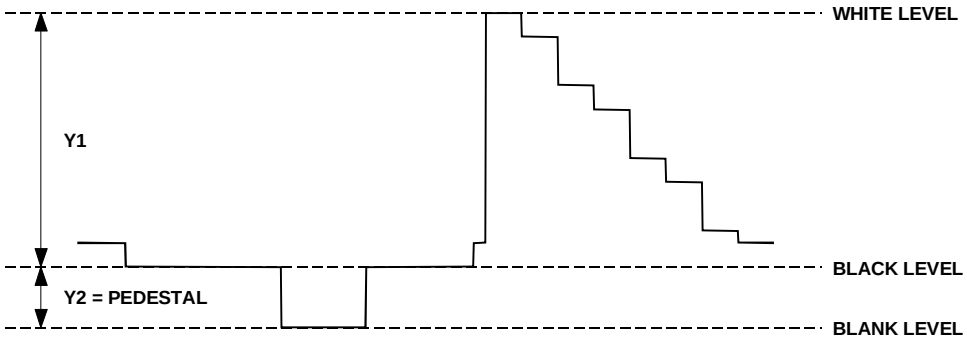
3(b) Analog Output with DC Offset



Note: The analog output shown includes a DC offset that can be controlled via the Digital Video Brightness Control Register, R3. The offset level can be adjusted from 0 – 0.164V (mode 0) or 0 – 0.191V (modes 2 – 5). Similarly, the gain-scale can be adjusted from 0.75x – 1.22x via the digital RGB/YUV input gain control registers R4, R5, and R6.

Figure 5: Analog Output Waveform (with programmable offset)

4(a) Auxiliary Analog Input with blank pedestal



4(b) Analog Output

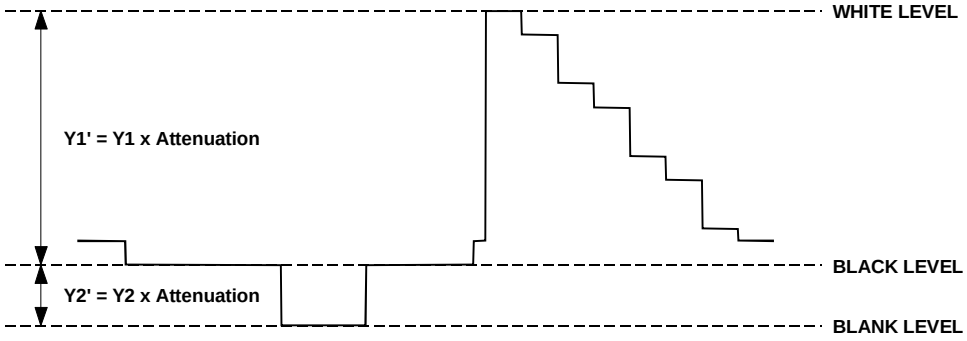
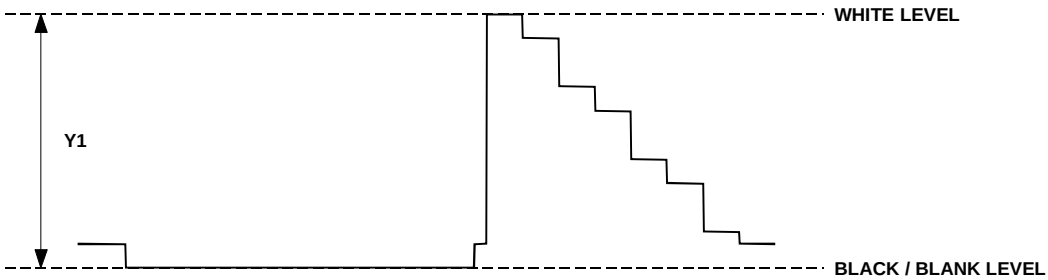


Figure 6: Analog Input and Output Waveforms (with blank pedestal)

5(a) Auxiliary Analog Input without blank pedestal



5(b) Analog Output

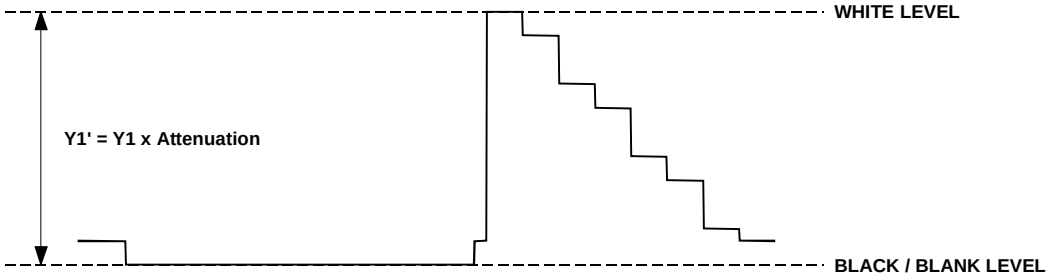


Figure 7: Analog Input and Output Waveforms (without blank pedestal)

Digital Video Input Formats

Chrontel's CH8439 supports six different digital input formats or modes as summarized in **Table 5** below. The six modes include 24-bit True-Color RGB format (RGB output), 4:4:4 YCbCr format (YUV output) and four 4:2:2 YCbCr formats (with color space conversion to provide RGB output).

Table 5 • Digital Video Input Formats

Register R0	MODE	Input Format	Output Format
0	0	RGB	RGB
1	1	4:4:4	YUV
2	2	4:2:2	RGB
3	3	4:2:2	RGB
4	4	4:2:2	RGB
5	5	4:2:2	RGB

In mode 2-5, HREF and P[23:0] are clocked by the rising edge of CLK. The rising edge of CLK that clocks in HREF going high also clocks in the first 16 bits [Y0 and U0(Cb)] of the YUV 4:2:2 data as described in **Table 6**. Note that in Mode 1, the U-data path is identical to the V-data path; therefore, P[23:16] may be used as the "U" inputs and P[7:0] may be used as the "V" inputs and vice versa (with the analog U/V outputs also swapped accordingly). The output is blanked if HREF = 0 in modes 2 - 5.

Table 6 • Pixel Data Organization

MODE	P[23:16]								P[15:8]								P[7:0]							
	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
0	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
1	U7	U6	U5	U4	U3	U2	U1	U0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	V7	V6	V5	V4	V3	V2	V1	V0
2	Y7	Y6	Y5	Y4	Y3				Y2	Y1	Y0	C7	C6	C5			C4	C3	C2	C1	C0			
3	C7	C6	C5	C4	C3				C2	C1	C0	Y7	Y6	Y5			Y4	Y3	Y2	Y1	Y0			
4	C4	C3	C2	C1	C0			Y7	Y1	Y0	C7	C6	C5				Y6	Y5	Y4	Y3	Y2			
5									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	C7	C6	C5	C4	C3	C2	C1	C0

Mode 0

With DIF[2:0] register bits of register R0 set to zero (default value upon power up), the digital input port P[23:0] accepts 24 bit True-Color RGB data with P[23:16], P[15:8], and P[7:0] comprising of the blue, green, and red pixels, respectively. **Table 17, "AC Characteristics,"** on page 34 specifies the timing requirements for the pixel clock CLK and RGB pixel data as illustrated in **Figure 15** on page 35.

Digital Video Input Format (continued)

Mode 1

With register bits DIF[2:0] of register R0 set to 001, the CH8439 provides the ability to support applications that use luminance and chrominance coded signals. P[15:8] represent the luminance signal Y, (output at GOUT - pin 28), while P[23:16] and P[7:0] represent the U and V signals (output at BOUT and ROUT, respectively). Since the U and V data paths are identical in the CH8439, the user can swap the pixel data representation of the U and V signals (the analog outputs will also be swapped accordingly).

The input range of the Y signal is from 0 to 255, while the input range of both the U and V signals is from -128 to +127. A 2's complement coding is applied to the U and V channels on-chip. In this mode, the CH8439 serves as a YUV DAC with analog multiplexer. The timing requirement is the same as that of mode 0 as shown in **Figure 15** on page 35.

Modes 2, 3, 4 and 5

CH8439 supports 4:2:2 YCbCr format with four different data pin assignments as shown in **Table 6**. The 4:2:2 YCbCr input data format sequence is shown in **Table 7**. An on-chip interpolating filter is used to generate the Cb and Cr data as shown in **Table 8**.

Table 7 • 4:2:2 YCbCr Input Data Format Sequence

16-bit Input Data Sequence	0		1		2		3	
Value	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3

Table 8 • Output Pixel Sequence

Output Pixel Sequence	0	1	2	3
Y	Y0	Y1	Y2	Y3
Cr	Cr0	$\frac{Cr0 + Cr2}{2}$	Cr2	$\frac{Cr2 + Cr4}{2}$
Cb	Cb0	$\frac{Cb0 + Cb2}{2}$	Cb2	$\frac{Cb2 + Cb4}{2}$

YCbCr-to-RGB Matrix

YCbCr-to-RGB color space conversion is performed according to the matrix shown below. The matrix converts the YCbCr video data to 24 bits of RGB data (8 bits per channel). The CH8439 YCbCr-to-RGB conversion complies to the CCIR Recommendation 601-1 described as follows:

$$R = 1.164 (Y-16) + 1.596 (Cr - 128)$$
$$G = 1.164 (Y-16) - 0.813 (Cr -128) - 0.391 (Cb - 128)$$
$$B = 1.164 (Y-16) + 2.018 (Cb - 128)$$

Serial Programming Interface

The CH8439 control registers are accessed through the two-wire serial port pins SD and SC. These two pins can be connected directly to the SDB and SCB buses as shown in **Figure 8**. The serial clock line, SC, is an input only pin and is driven by the output buffer of a master device. The CH8439 acts as a slave device, and therefore, relies on the master device to generate the clock signal on the bus. When the bus is free, both lines are pulled high. As a requirement, the output stages of the devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data on the bus can be transferred up to 400 kbit/s.

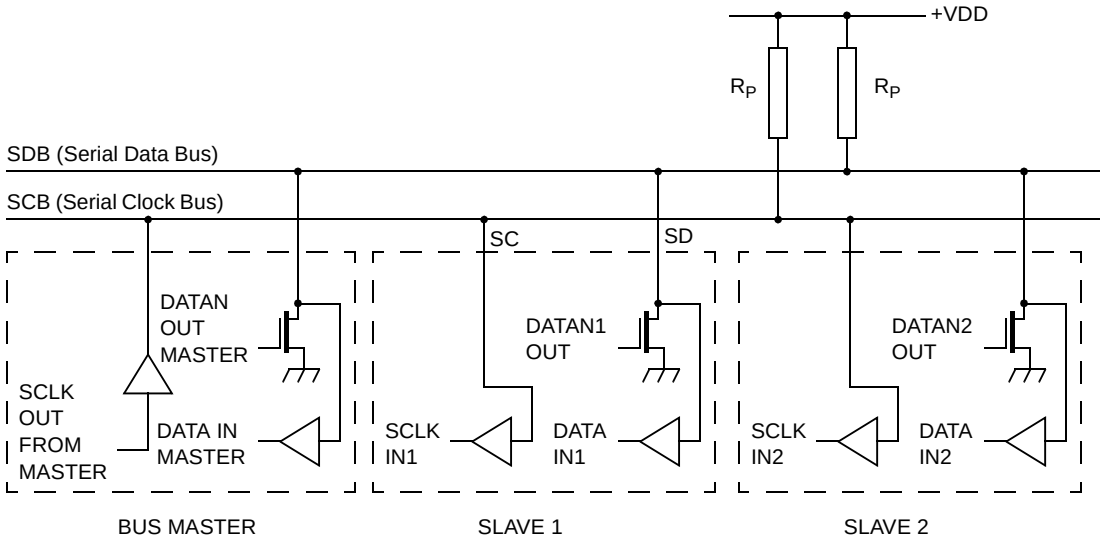


Figure 8: Serial Bus Connection

Serial Port Transfer Protocol

An example of a basic data transfer follows the format shown in **Figure 9** on page 18. The format of this data transfer comprise of the basic components: chip select, start condition, register address byte (RAB), register data, and stop condition.

Chip Select

For a master-transmitter device to communicate with the CH8439, the master-transmitter must assert the chip select signal high (e.g., CS = 1) prior to generating the "start condition." The master-transmitter may assert this signal low (e.g., CS=0) as soon as it is done communicating with the CH8439 and after it has generated the "stop condition."

Start and Stop Conditions

A "start condition" occurs whenever a high-to-low transition of SD occurs while SC is high. On the other hand, a "stop condition" occurs whenever a low-to-high transition of SD occurs while SC is high. Start and stop conditions are always generated by the master-transmitter.

Register Address Byte (RAB)

The register address byte contains the following information: R/W* bit, AutoInc bit, and address register. The address register is used indicate to the CH8439 which register the master-transmitter wishes to communicate to. The R/W* bit indicates whether the master-transmitter wishes to perform a read or a write to the registers. The AutoInc bit is used to indicate a mode of data transfer the master-transmitter wishes to perform. The format and description of the RAB is further elaborated on page 18.

Register Data

This consist of the data the master-transmitter wish to write (or read) to (or from) the CH8439 register specified by the RAB. As with the RAB, the high or low state of SD can only change while SC is low.

Serial Programming Interface (continued)

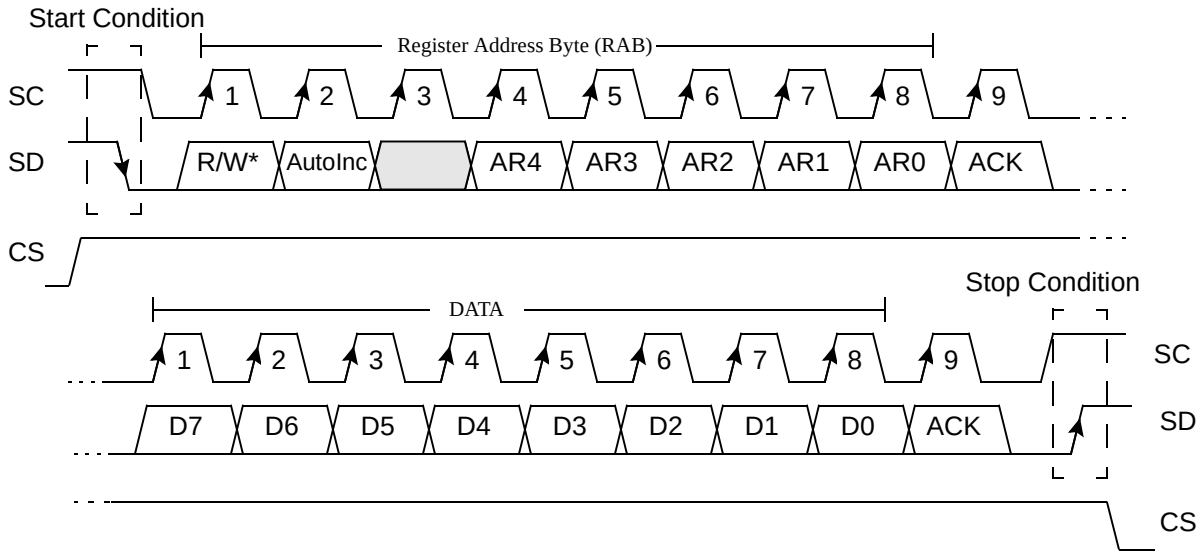


Figure 9: Serial Port Transfer Protocol

Register Address Byte (RAB) Format

R/W* **Read/Write Bit**

This bit indicates whether a read or a write cycle to the CH8439 is being asserted. Read cycle is performed when R/W* = 1, while a write cycle is performed when R/W* =0.

AutoInc **Register Address Auto-Increment Bit (active high)**

When enabled, this bit facilitates the sequential read of or write to the CH8439 registers. Auto-Increment enabled (auto-increment mode)

"1" : Auto-Increment Enabled

Write Mode: The auto-increment is a post-increment. That is, in this mode the address register will be automatically incremented by one after the data has been written into a register.

Read Mode: The auto-increment is a pre-increment. That is, in this mode the address register will be automatically incremented by one before loading the actual data from a register to the temporary register (register where data is serially read from). But for the first read after the RAB, the address register will not be changed.

"0" : Alternating Mode Enabled (Auto-Increment Disabled)

Write Mode: After writing data into a register, the address register will remain unchanged until a new RAB is written.

Read Mode: Before loading data from a register to the temporary register (register where data is serially read from), the address register will remain unchanged.

AR[4:0] **Register Address**

These bits specify the address of the register being accessed.

The following sections will describe the operation of the serial interface for the four combinations of R/W* = 0,1 and AutoInc = 0,1.

Serial Programming Interface (continued)

Serial Programming: Write Cycle Protocols (R/W* = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. The CH8439 always acknowledges for writes as shown in **Figure 10**. Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver.

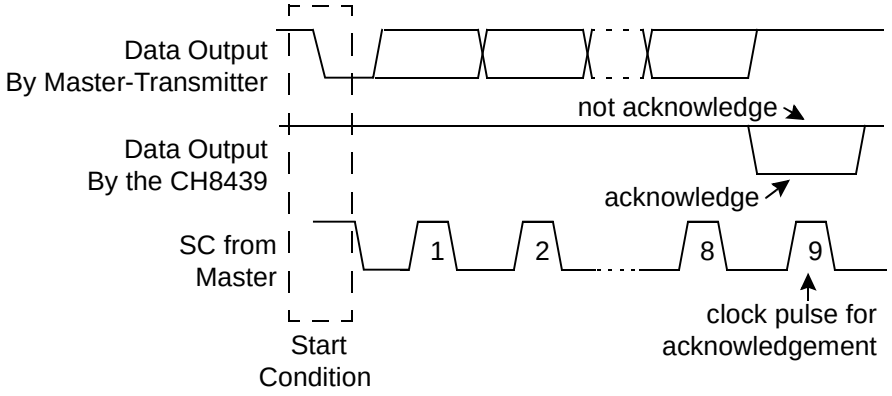


Figure 10: Acknowledge on the Bus

Figure 11 below shows two consecutive Alternating write cycles with AutoInc = 0 and R/W* = 0. The byte of information following the Register Address Byte (RAB) is the data to be written into the register specified by AR[4:0]. If AutoInc = 0 (Alternating mode enabled), then another RAB is expected from the master device followed by another data byte, and so on if necessary. However, if AutoInc = 1 (Auto-Increment mode enabled), then the register address pointer will be incremented automatically and subsequent data bytes will be written into successive registers without providing a RAB between each data byte. **Figure 12** on page 20 shows an example of the Auto-increment write cycle.

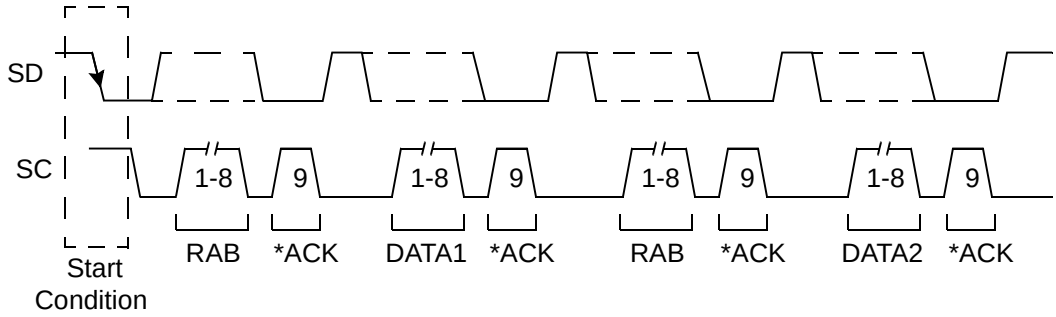


Figure 11: Alternating Write Cycles

Note: * The acknowledge is from the CH8439 (slave).

Serial Programming Interface (continued)

When the auto-increment mode is enabled (AutoInc = 1), the register address pointer will continue to increment for each write cycle until AR[4:0] = 12h (12h is the address of the Address Register). When AR[4:0] = 12h, the next byte of information represents a new auto-sequencing "Starting address", which is the address of the register to receive the next byte. The auto-sequencing will then resume based on this new "Starting address". The auto-increment sequence can be terminated anytime by either a "STOP" or "START" condition. The write operation can be terminated with a "STOP" condition.

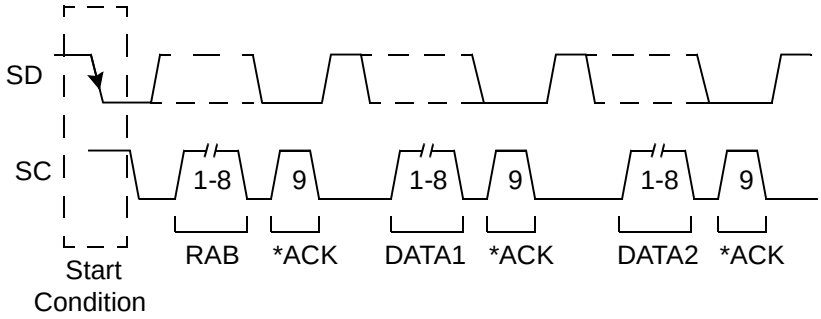


Figure 12: Auto-increment Write Cycle

Note: * The acknowledge is from the CH8439 (slave).

Serial Programming: Read Cycle Protocols (R/W* = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH8439 will release the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device will start by issuing a "START" condition (or a "RESTART" condition). The first byte of data after the START condition is a RAB with R/W* = 1 and with AR[4:0] containing the address of the register the master device intends to read from. The master device should then issue a "RESTART" condition ("RESTART" = "START" without a previous "STOP" condition). The master device then reads the next byte of data (the content of the register specified in the RAB). If AutoInc = 0, then another RESTART condition followed by another RAB with R/W* = 1 is expected from the master device. The master device then issues another RESTART condition after which the data byte can be read and so on. In summary, a "RESTART" condition must be generated before each of the RAB and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 13**.

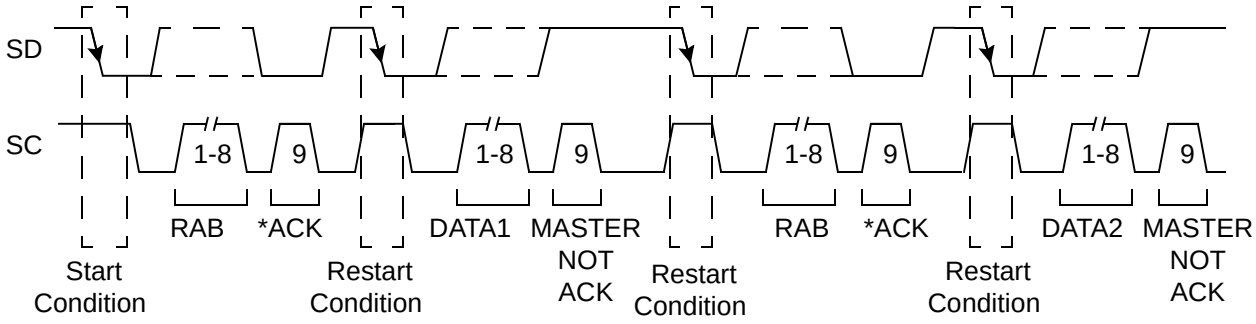


Figure 13: Alternating Read Cycle

Serial Programming Interface (continued)

If AutoInc = 1, then the address register will be incremened automatically and subsequent data bytes can be read from successive registers without providing a RAB each time.

When the auto-increment mode is enabled (AutoInc = 1), the Address Register will continue incrementing for each read cycle. After the count reaches 12h, it will "wrap around" and begin from 00h. The auto increment sequence can be terminated by either a "STOP" or "RESTART" condition. The read operation can be terminated with a "STOP" condition. **Figure 14** shows an auto-increment read cycle terminated by a stop or restart condition.

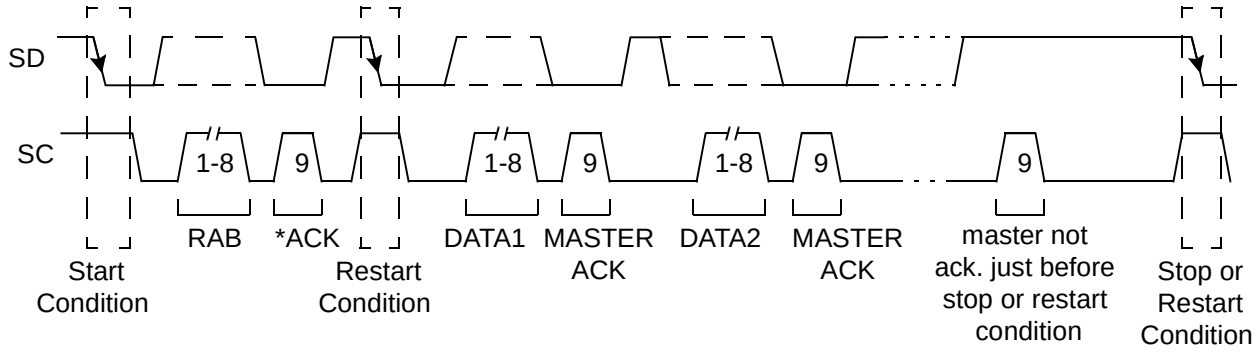


Figure 14: Auto-increment Read Cycle

Serial Programming Interface (continued)

Electrical Characteristics for Bus Devices

The electrical specifications of the bus devices' inputs and outputs and the characteristics of the bus lines connected to them are shown in **Figure 19**. A pull-up resistor (R_P) must be connected to a 5V ± 10% supply as shown in **Figure 8** on page 17. The CH8439 is a device with input levels related to V_{DD}.

Maximum and minimum values of pull-up resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 3mA at V_{OLmax} = 0.4 V for the output stages.

- $R_P \geq (V_{DD} - 0.4) / 3$ (R_P in kΩ)

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for R_P is shown below:

- $R_P \leq 10^3/C$ (where R_P is in kΩ and C, the total capacitance, is in pF)

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_P. The R_P limit depends on V_{DD} and is shown below:

- $R_P \leq (100 \times V_{DD}) / I_{input}$ (where R_P is in kΩ and I_{input} is in µA)

Register Descriptions

The CH8439 contains 19 control registers each with a maximum of eight usable bits to provide access to basic video attribute control functions. These registers are accessible via the two-wire serial bus (SD & SC). The following section describes the functions and the controls available through these registers.

Table 9. Register Map

Register	Address	Default Value	Description
R0	00H	xxxx_x000	Digital Video Input Format Control Register
R1	01H	xxxx_xx00	Analog Input Attenuation Control Register
R2	02H	xxxx_x000	Multiplexer Delay Control Register
R3	03H	xxxx_x000	Digital Video Brightness Control Register
R4	04H	xxxx_1000	Red / V Digital Input Gain Control Reigster
R5	05H	xxxx_1000	Green / Y Digital Input Gain Control Reigster
R6	06H	xxxx_1000	Blue / U Digital Input Gain Control Reigster
R7	07H	x100_0000	Red Color Key Upper Threshold Control Register
R8	08H	x010_0000	Red Color Key Lower Threshold Control Register
R9	09H	x000_0111	Green Color Key Upper Threshold Control Register
R10	0AH	x100_0000	Green Color Key Lower Threshold Control Register
R11	0BH	x100_0000	Blue Color Key Upper Threshold Control Register
R12	0CH	x010_0000	Blue Color Key Lower Threshold Control Register
R13	0DH	0011_0011	PLL Control Register I
R14	0EH	0001_1110	PLL Control Register II
R15	0FH	xxx0_0000	Comparator Adjustment Register
R16	10H	0000_0000	Miscellaneous Control Register
R17	11H	xxxx_0000	Test Register
R18	12H	–	Address Register

Table 10. Control Register Summary

Register	D7	D6	D5	D4	D3	D2	D1	D0
R0	–	–	–	–	–	DIF2	DIF1	DIF0
R1	–	–	–	–	–	–	AA1	AA0
R2	–	–	–	–	–	MDS2	MDS1	MDS0
R3	–	–	–	–	–	DVB2	DVB1	DVB0
R4	–	–	–	–	RV_G3	RV_G2	RV_G1	RV_G0
R5	–	–	–	–	GY_G3	GY_G2	GY_G1	GY_G0
R6	–	–	–	–	BU_G3	BU_G2	BU_G1	BU_G0
R7	–	RCKU_ENB	RCKU5	RCKU4	RCKU3	RCKU2	RCKU1	RCKU0
R8	–	RCKL_ENB	RCKL5	RCKL4	RCKL3	RCKL2	RCKL1	RCKL0
R9	–	GCKU_ENB	GCKU5	GCKU4	GCKU3	GCKU2	GCKU1	GCKU0
R10	–	GCKL_ENB	GCKL5	GCKL4	GCKL3	GCKL2	GCKL1	GCKL1
R11	–	BCKU_ENB	BCKU5	BCKU4	BCKU3	BCKU2	BCKU1	BCKU0
R12	–	BCKL_ENB	BCKL5	BCKL4	BCKL3	BCKL2	BCKL1	BCKL0
R13	CSD1	CSD0	K1	K0	H_INV	N10	N9	N8
R14	N7	N6	N5	N4	N3	N2	N1	N0
R15	–	–	–	CT4	CT3	CT2	CT1	CT0
R16	VGAIN	Reserved	CKEY_EN	ACKEY	OVLY	XKEY_INV	PS	PD
R17	–	–	–	–	Reserved	Reserved	Reserved	Reserved
R18	–	–	–	AR4	AR3	AR2	AR1	AR0

R0: Digital Video Input Format Control Register (Address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	DIF2	DIF1	DIF0

The initial value of this register upon power up is xxxx_x000.

DIF2 - DF0 **Video Input Format Mode Select**

These bits are used to select input format of P[23:0].

DIF2	DIF1	DIF0	MODE	Input Format
0	0	0	0	RGB
0	0	1	1	4:4:4 †
0	1	0	2	4:2:2
0	1	1	3	4:2:2
1	0	0	4	4:2:2
1	0	1	5	4:2:2

† No color space conversion is performed under this mode; therefore, the circuit in the CH8439 act as YUV digital-to-analog converters.

R1: Analog Input Attenuation Control Register (Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	–	AA1	AA0

The initial value of this register upon power up is xxxx_xx00.

A1 - A0 **Analog Input Attenuation Control**

These bits select the level of attenuation applied to the auxiliary analog RGB inputs. For example, Output = Input x Attenuation.

AA1	AA0	Attenuation
0	0	1.000
0	1	0.875
1	0	0.750
1	1	0.500

R2: Multiplexer Delay Control Register (Address 02h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	MDS2	MDS1	MDS0

The initial value of this register upon power up is xxxx_x000.

MDS2 - MDS0 Multiplexer Delay Select Control

These bits select the value of the time delay introduced at the multiplexer.

MDS2	MDS1	MDS0	Nominal Delay Value (ns)
0	0	0	5
0	0	1	10
0	1	0	25
0	1	1	35
1	0	0	45
1	0	1	55
1	1	0	65
1	1	1	75

R3: Digital Video Brightness Control Register (Address 03h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	–	DVB2	DVB1	DVB0

The initial value of this register upon power up is xxxx_x000.

DVB2 - DVB0 Digital Video Brightness Control

These bits control the brightness of the digital video input by selecting the level of the DC offset introduced at the output.

DVB2	DVB1	DVB0	Nominal Offset Value (Volts) †	
			Mode 0,1	Mode 2, 3, 4, 5
0	0	0	0.000	0.000
0	0	1	0.023	0.027
0	1	0	0.047	0.055
0	1	1	0.070	0.082
1	0	0	0.094	0.109
1	0	1	0.117	0.136
1	1	0	0.141	0.164
1	1	1	0.164	0.191

† These values assume a 75Ω-terminated color monitor

R4: Red / V Digital Input Gain Control Register (Address 04h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	RV_G3	RV_G2	RV_G1	RV_G0

The initial value of this register upon power up is xxxx_1000.

RV_G[3:0] **Digital Input Gain Control**

These bits control the gain applied to the Red (Mode 0) or V (Modes 1-5) video inputs. For details, please refer to **Table 11** below.

R5: Green / Y Digital Input Gain Control Register (Address 05h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	GY_G3	GY_G2	GY_G1	GY_G0

The initial value of this register upon power up is xxxx_1000.

GY_G[3:0] **Digital Input Gain Control**

These bits control the gain applied to the Green (Mode 0) or Y (Modes 1-5) video inputs. For details, please refer to **Table 11** below.

R6: Blue / U Digital Input Gain Control Register (Address 06h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	BU_G3	BU_G2	BU_G1	BU_G0

The initial value of this register upon power up is xxxx_1000.

BU_G[3:0] **Digital Input Gain Control**

These bits control the gain applied to the Blue (Mode 0) or V (Modes 1-5) video inputs. For details, please refer to **Table 11** below.

Table 11. Digital RGB/YUV Video Input Gain Control

G3	G2	G1	G0	Full-Scale Output Voltage (Volts) †
0	0	0	0	0.66 – 50%
0	0	0	1	. . .
0	0	1	0	. . .
0	0	1	1	. . .
0	1	0	0	. . .
0	1	0	1	. . .
0	1	1	0	. . .
0	1	1	1	. . .
1	0	0	0	0.66
1	0	0	1	. . .
1	0	1	0	. . .
1	0	1	1	. . .
1	1	0	0	. . .
1	1	0	1	. . .
1	1	1	0	. . .
1	1	1	1	0.66 + 47%

† These values assume a 75Ω-terminated color monitor

R7: Red Color Key Upper Threshold Control Register (Address 07h)

D7	D6	D5	D4	D3	D2	D1	D0
–	RCKU_ENB	RCKU5	RCKU4	RCKU3	RCKU2	RCKU1	RCKU0

The initial value of this register upon power up is x100_0000.

RCKU_ENB **Red Color Key Upper Bound Enable**

"1" : Upper bound criteria is disabled
"0" : Upper bound criteria is enabled

RCKU[5:0] **Red Color Key Upper Bound Threshold**

These bits select the value of the Red color key upper threshold level.
RCKU[5:0] = [111111] = full scale = 0.985V
RCKU[5:0] = [000000] = 0V

R8: Red Color Key Lower Threshold Control Register (Address 08h)

D7	D6	D5	D4	D3	D2	D1	D0
–	RCKL_ENB	RCKL5	RCKL4	RCKL3	RCKL2	RCKL1	RCKL0

The initial value of this register upon power up is x010_0000.

RCKL_ENB **Red Color Key Lower Bound Enable**

"1" : Lower bound criteria is disabled
"0" : Lower bound criteria is enabled

RCKL[5:0] **Red Color Key Lower Bound Threshold**

These bits select the value of the Red color key lower threshold level.
RCKL[5:0] = [111111] = full scale = 0.985V
RCKL[5:0] = [000000] = 0V

R9: Green Color Key Upper Threshold Control Register (Address 09h)

D7	D6	D5	D4	D3	D2	D1	D0
–	GCKU_ENB	GCKU5	GCKU4	GCKU3	GCKU2	GCKU1	GCKU0

The initial value of this register upon power up is x000_0111.

GCKU_ENB **Green Color Key Upper Bound Enable**

"1" : Upper bound criteria is disabled
"0" : Upper bound criteria is enabled

GCKU[5:0] **Green Color Key Upper Bound Threshold**

These bits select the value of the Green color key upper threshold level.
GCKU[5:0] = [111111] = full scale = 0.985V
GCKU[5:0] = [000000] = 0V

R10: Green Color Key Lower Threshold Control Register (Address 0Ah)

D7	D6	D5	D4	D3	D2	D1	D0
–	GCKL_ENB	GCKL5	GCKL4	GCKL3	GCKL2	GCKL1	GCKL0

The initial value of this register upon power up is x100_0000.

GCKL_ENB **Green Color Key Lower Bound Enable**

"1" : Lower bound criteria is disabled
"0" : Lower bound criteria is enabled

GCKL[5:0] **Green Color Key Lower Bound Threshold**

These bits select the value of the Green color key lower threshold level.
GCKL[5:0] = [111111] = full scale = 0.985V
GCKL[5:0] = [000000] = 0V

R11: Blue Color Key Upper Threshold Control Register (Address 0Bh)

D7	D6	D5	D4	D3	D2	D1	D0
–	BCKU_ENB	BCKU5	BCKU4	BCKU3	BCKU2	BCKU1	BCKU0

The initial value of this register upon power up is x100_0000.

BCKU_ENB **Blue Color Key Upper Bound Enable**

"1" : Upper bound criteria is disabled
"0" : Upper bound criteria is enabled

BCKU[5:0] **Blue Color Key Upper Bound Threshold**

These bits select the value of the Blue color key upper threshold level.
BCKU[5:0] = [111111] = full scale = 0.985V
BCKU[5:0] = [000000] = 0V

R12: Blue Color Key Lower Threshold Control Register (Address 0Ch)

D7	D6	D5	D4	D3	D2	D1	D0
–	BCKL_ENB	BCKL5	BCKL4	BCKL3	BCKL2	BCKL1	BCKL0

The initial value of this register upon power up is x010_0000.

BCKL_ENB **Blue Color Key Lower Bound Enable**

"1" : Lower bound criteria is disabled
"0" : Lower bound criteria is enabled

BCKL[5:0] **Blue Color Key Lower Bound Threshold**

These bits select the value of the Blue color key lower threshold level.
BCKL[5:0] = [111111] = full scale = 0.985V
BCKL[5:0] = [000000] = 0V

R13: PLL Control Register I (Address 0Dh)

D7	D6	D5	D4	D3	D2	D1	D0
CSD1	CSD0	K1	K0	H_INV	N10	N9	N8

The initial value of this register upon power up is 00011_0011.

CSD1 - CSD0 **Comparator Strobe Divider Control**

These bits control the divider, at the output of the VCO, that generates the strobing clock for the internal comparators. This feature allows the comparator strobing clock to run faster than the output of the genlock CLKOUT.

CSD1	CSD0	Divider Ratio
0	0	1
0	1	2
1	0	3
1	1	4

K1 - K0 **PLL Clock Output Divider Control**

These bits select the output divider k at the output of the VCO.
The output divider k = K + 1, where K is the value of K[1:0].

K1	K0	Divider Ratio
0	0	1
0	1	2
1	0	3
1	1	4

H_INV **HSYNC Polarity Control Bit**

This bit controls the polarity of the graphics HSYNC input to the CH8439.
"1" : The rising edge of the graphics HSYNC pulse is the leading edge.
"0" : The falling edge of the graphics HSYNC pulse is the leading edge.
This is the default upon power-up.

N10 - N8 **PLL Feedback Divider N**

These bits specify the three MSBs of the 11-bit PLL feedback divider N. The "divide by n" counter is defined such that n = N+2, where N = value of the 11 programmable bits.

R14: PLL Control Register II (Address 0Eh)

D7	D6	D5	D4	D3	D2	D1	D0
N7	N6	N5	N4	N3	N2	N1	N0

The initial value of this register upon power up is 0001_1110.

N7 - N0 **PLL Feedback Divider N**

These bits specify the eight LSBs of the 11-bit PLL feedback divider N. These bits are used in conjunction with the three LSBs of register R13 (bits N10-N8).

R15: Comparator Adjustment Register (Address 0Fh)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	CT4	CT3	CT2	CT1	CT0

The initial value of this register upon power up is xxx0_0000.

CT4 **Comparator Timing Reference Control**

"1" : CLKOUT is enabled as an Input.
Under this mode, the PLL is powered down, allowing an external pixel clock source to provide the timing reference of the CH8439 on-chip comparators.

"0" : CLKOUT is enabled as an Output.
The internal genlock provides the timing reference to the CH8439 on-chip comparators.

CT3 - CT0 **Comparator Timing Adjustment Control**

These bits select the value of the comparator timing with respect to the analog RGB data timing.

CT3	CT2	CT1	CT0	Adjustment (ns)
0	0	0	0	0.00
0	0	0	1	2.50
0	0	1	0	5.00
0	0	1	1	7.50
0	1	0	0	10.0
0	1	0	1	12.5
0	1	1	0	15.0
0	1	1	1	17.5
1	0	0	0	20.0
1	0	0	1	22.5
1	0	1	0	25.0
1	0	1	1	27.5
1	1	0	0	30.0
1	1	0	1	32.5
1	1	1	0	35.0
1	1	1	1	37.5

R16: Miscellaneous Control Register (Address 10h)

D7	D6	D5	D4	D3	D2	D1	D0
VGAIN	Reserved	CKEY_EN	ACKEY	OVLY	XKEY_INV	PS	PD

The initial value of this register upon power up is 0000_0000.

VGAIN **Video Amplifier Gain Adjustment**

"1" : Gain of video amplifiers are set to 1.25
"0" : Gain of video amplifiers are set to unity

Reserved **Reserved bit**

This bit must be set to zero.

CKEY_EN **Analog Color Key Output Enable**

This bit controls whether the state of CKEY match is reflected on the CKEY output pin.
"1" : Analog Color Key output CKEY is enabled.
"0" : Analog Color Key output CKEY is tri-stated.

ACKEY **Analog Color Keying Mode Select**

"1" : Analog Color Keying is enabled regardless XKEY = 0 or 1
"0" : Analog Color Keying is enabled when XKEY = 1

OVLY = **RGB DAC Output Select**

This bit controls the type of analog RGB output coming out of the RGB DAC pins.
"1" : Output Video + Graphics.
The output from the RGB DAC pins will be a duplicate of the RGB OUT pins. That is, under this mode, the ouputs to these pins would consist of the graphics with the digital video overlayed on it.
"0" : Output Video ONLY.
The output from the RGB DAC pins consist of the outputs from the CH8439 DACs.

XKEY_INV = **XKEY (External Key) Polarity Control**

"1" : XKEY input is active LOW
"0" : XKEY input is active HIGH

PS = **Power Saving Mode**

"1" : RGB DAC ouputs are disabled
"0" : RGB DAC ouputs are enabled

PD = **Power Down Mode**

"1" : Power down mode is enabled
"0" : Power down mode is disabled

R17: Test Register (Address 11h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	–	Reserved	Reserved	Reserved	Reserved

The initial value of this register upon power up is xxxx_0000.

Reserved **Reserved bits**

These bits must be set to zero.

R18: Address Register (Address 12h)

D7	D6	D5	D4	D3	D2	D1	D0
–	–	–	AR4	AR3	AR2	AR1	AR0

The initial value of this register upon power up is xxxx_xxxx.

AR4 - AR0 **Address Register bits**

These bits specify the address of the register being accessed.

Electrical Specifications

Table 12 • Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	V_{DD} relative to GND	- 0.5		7.0	V
	Input voltage of all digital pins[1]	GND - 0.5		V_{DD} + 0.5	V
	Analog output short circuit duration			Indefinite	Sec
T_{STOR}	Storage temperature	- 65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (one minute)			220	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1 The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

Table 13 • Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
V_{DD}	Supply voltage	4.75	5.00	5.25	V
T_A	Ambient operating temperature	0	25	70	°C
R_L	Analog output load		75		Ω

Table 14 • DC Characteristics (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ± 5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
	Resolution (each DAC)		8	8	8	Bits
	Accuracy (each DAC)					
L_I	Integral linearity error				±1	LSB
L_D	Differential linearity error				±1	LSB
	Gray scale error				±5	%
	Monotonicity	Guaranteed				
	Coding	Binary				

Table 15 • Digital Inputs / Outputs

Symbol	Description	Test Condition @ T_A = 25°C	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = - 400 µA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	Input high voltage		2.0		V_{DD}+0.5	V
V_{IL}	Input low voltage		GND - 0.5		0.8	V
I_{LK}	Input leakage current		- 10		10	µA
CD_{IN}	Input capacitance	f = 1 MHz, V_{IN} = 2.4V			7	pF
CD_{IN}	Input capacitance	f = 1 MHz, V_{IN} = 2.4V		20		pF
CD_{OUT}	Output capacitance				7	pF

Electrical Specifications (continued)

Table 16 • Analog Outputs (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ± 5%)

Symbol	Description	Test Condition @ T_A = 25°C	Min	Typ	Max	Units
PSRR	Power supply rejection ratio				0.5	% / % VDD

Table 17 • AC Characteristics

Symbol	Description	Min	Typ	Max	Units
t_{SETUP}	CLK to pixel data setup requirement	3			ns
t_{HOLD}	CLK to pixel data hold requirement	1			ns

Table 18 • Serial Port I/O Characteristics

Symbol	Parameter	standard-mode devices		Unit
		Min	Max	
V_{IL}	LOW level input voltage: V_{DD} related input levels	–0.5	$0.3V_{DD}$	V
V_{IH} [1]	HIGH level input voltage: V_{DD} related input levels	$0.7V_{DD}$	1	V
V_{OL}	LOW level output voltage (open drain or open collector) at 3mA sink current	0	0.4	V
t_{OF}	Output fall time from V_{IH} min to V_{IL} max with a bus capacitance from 10pF to 400 pF (with up to 3 mA sink current at V_{OL})	–	250	ns
I_i	Input current at each I/O pin with an input voltage between 0.4 V and 0.9 V_{DD} max	–10	10	µA
C_i	Capacitance for each I/O pin	–	10	pF
f_{SCL}	Maximum clock frequency	0	400	kHz
t_{BUF}	Data change minimum waiting time	4.7	–	µs
t_1	Data transfer start minimum waiting time	4.0	–	µs
t_{LOW}	Low level clock pulse width	4.7	–	µs
t_{HIGH}	High level clock pulse width	4.0	–	µs
t_2	Minimum data hold time	5.0	–	µs
t_3	Minimum data preparation time	250	–	ns
t_4	Minimum start preparation waiting time	4.7	–	µs
t_R	Rise time	–	1	µs
t_F	Fall time	–	300	ns
t_5	Data transfer start minimum waiting time	4.0	–	µs
t_6	Minimum stop preparation waiting time	4.0	–	µs

Note: **1** maximum V_{IH} = V_{DD} max + 0.5V

Timing Diagrams

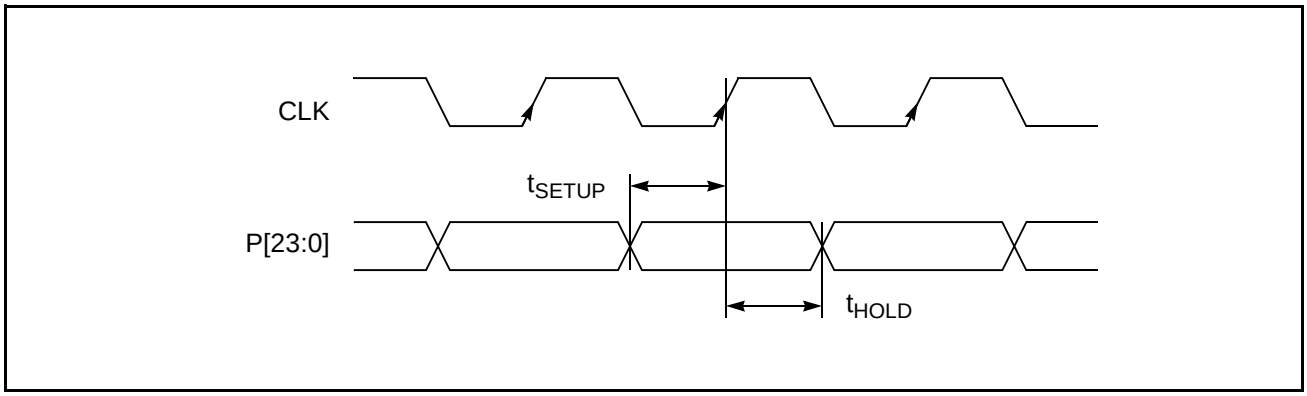


Figure 15: Mode 0 and Mode 1 Input Data Timing

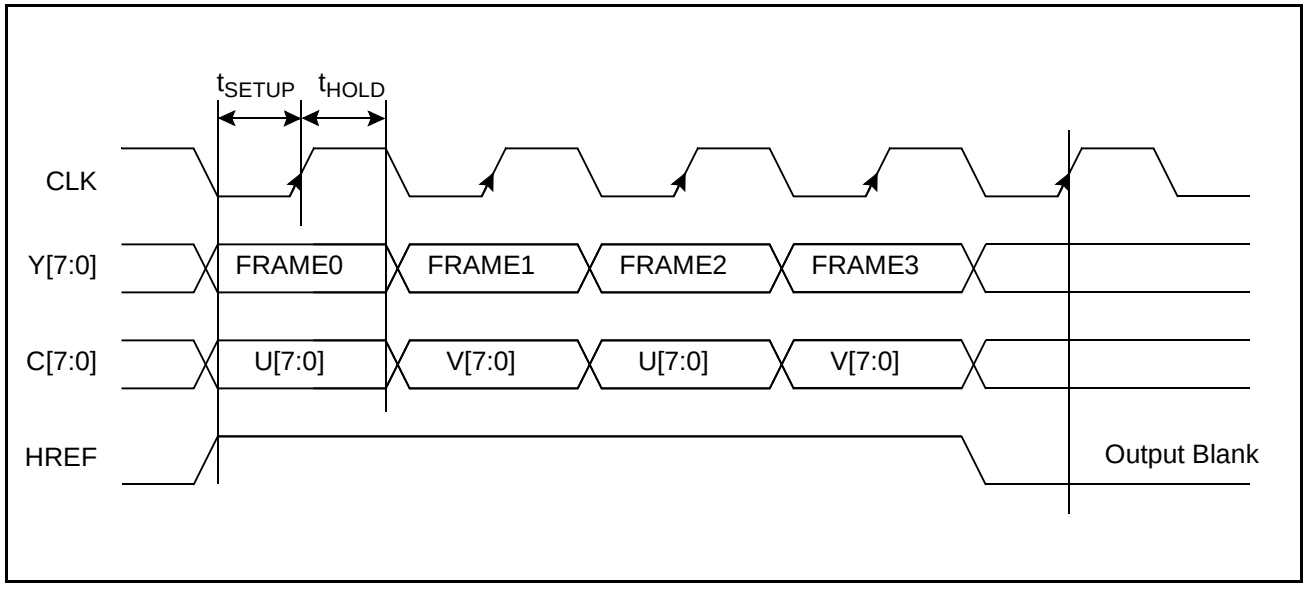


Figure 16: Mode 2 – Mode 5 Input Data Timing

Timing Diagrams (continued)

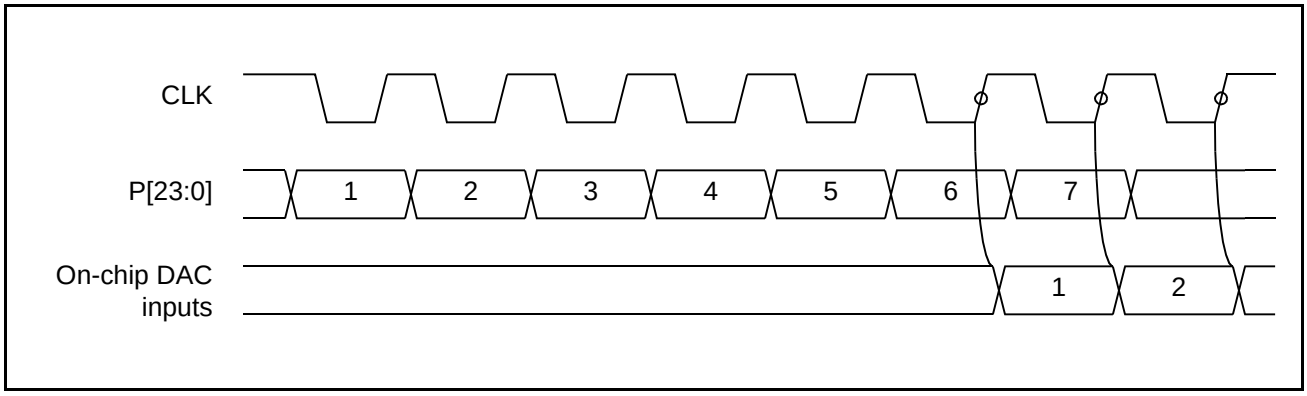


Figure 17: Pipeline Clock Cycles for Modes 2 - 5

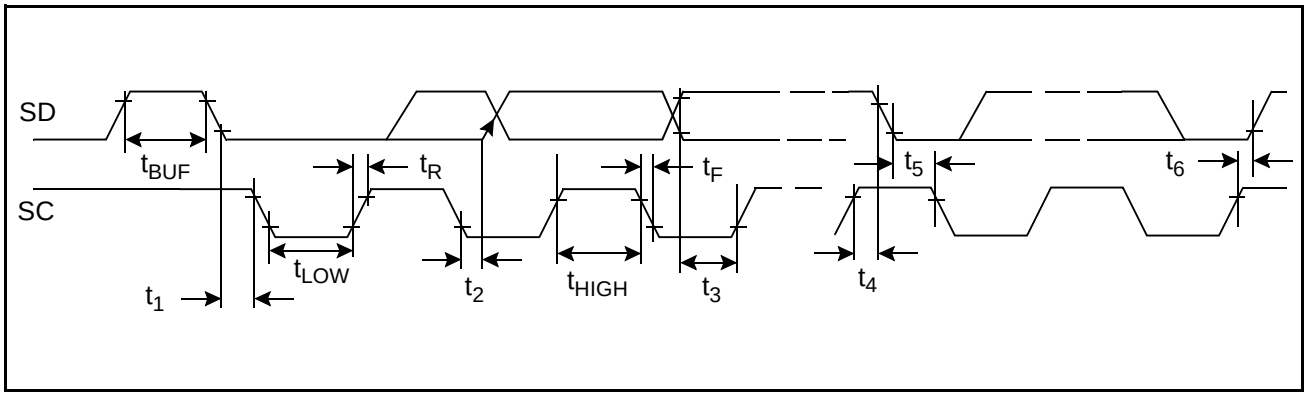


Figure 18: Serial Port Timing

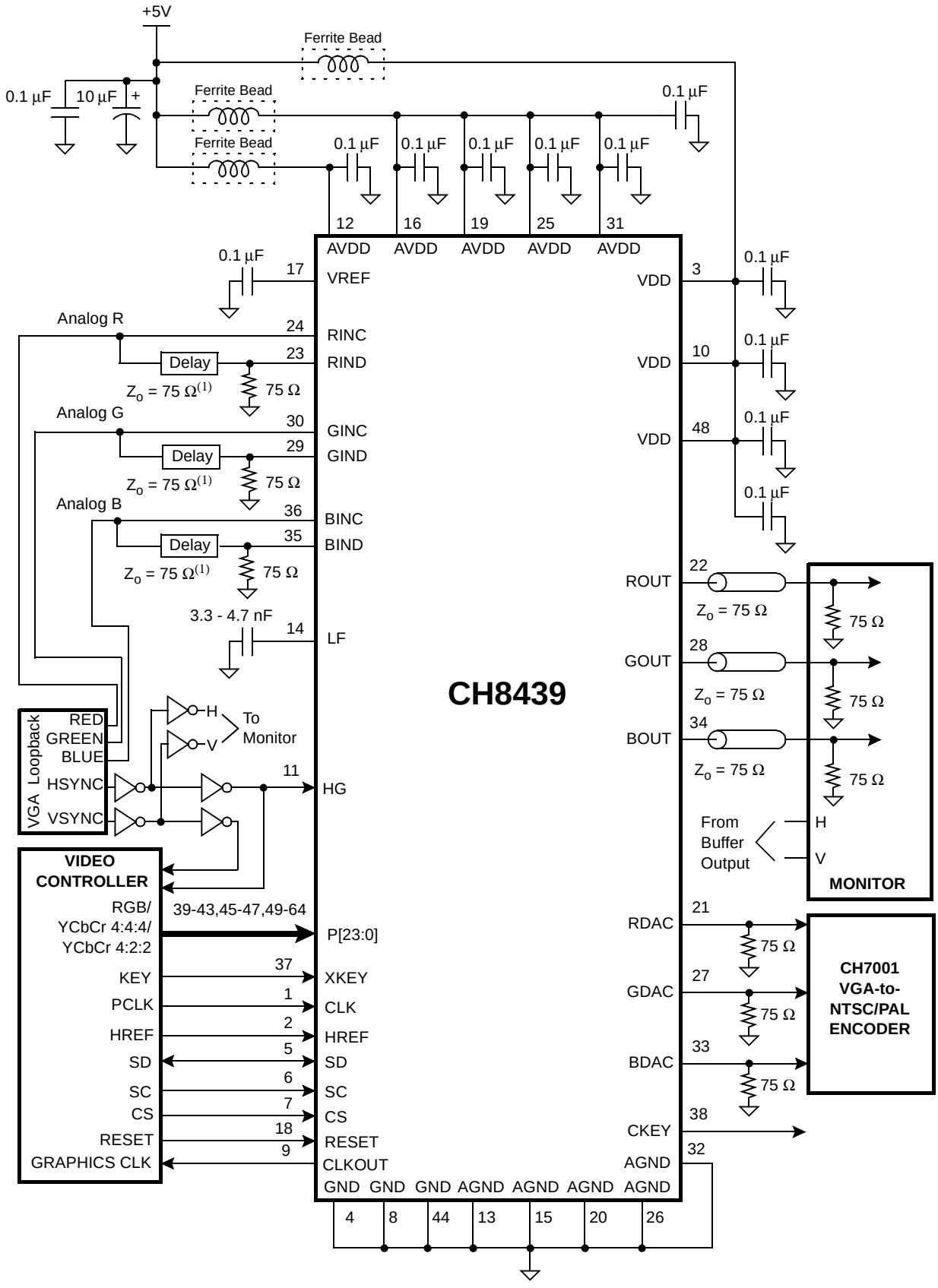


Figure 19: Typical Connection Diagram

Note: 1 Analog delay line with 75Ω characteristic impedance and bandwidth > 100MHz.

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH8439-Q	PQFP	64	5V

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