MC10/100H640 Translator Family I/O SPICE Modeling Kit

Prepared by: Debbie Beckwith
ECL Applications Engineering

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APPLICATION NOTE

This application note provides the SPICE information necessary to accurately model system interconnect situations for designs which utilize the translator circuits of the MC10H600 family. The note includes information on the H600, H601, H602, H603, H604, H605, H606, and H607 translators.

Objective

With the difficulty in designing highspeed controlled impedance PC boards and the expense of reworking those boards, the ability to model circuit behavior prior to committing to a board layout is essential for high speed logic designers. The purpose of this document is to provide the user with enough information to perform basic SPICE model analysis on the interconnect traces being driven or driving the H600, H601, H602, H603, H604, H605, H606 or H607 translator chips. The packet includes schematics of the input and output structures, as well as ESD protection structures and package models which may affect the waveshape of the input and output waveforms. Internal bias regulators and logic circuitry are not included as they have little impact on the I/O characteristics of the device and add a significant amount of time to the standard simulation analysis. In addition, a SPICE parameter set for the devices referenced in the schematics is provided. The remainder of this document will introduce the various input and output stages for the H60x translators, as well as the other structures which affect the I/O characteristics of these devices.

Schematic Overview

There are ten basic schematics which can be used to represent all of the I/O for the H60x family of translator chips. A single TTL input structure can be used to represent all of the TTL inputs, with the exception of the H606s “CLKT” input, which should be modeled using the “H606 TTL Input” structure. All of the ECL inputs can be represented by a single ECL input structure, with the exception of the H601s “data” inputs, the H601s ECL “TRI” and “TRIB” inputs and the H602s “ECLST” input, which should be modeled using the “H601 I/O Gate” structure, the “H601 ECL Input” structure, and the “H602 ECL Input” structure, respectively. Six different output buffers represent all of the output buffers for the H60x series of translators. The rest of the schematics provided represent subcircuit schematics for the above mentioned I/O buffers, ESD protection circuitry and package models. The devices shown in shaded boxes on the I/O buffer schematics are modelled by the subcircuits illustrated on the appropriate subcircuit schematic sheet. This hieracrchical method of schematic representation is used to help simplify and clarify the buffer schematics.

The H600 and H602 utilize the same output buffer. This buffer is represented by the H600 Output schematic of Figure 6. These devices are dual supply devices which means they require +5 V, -5.2 V and ground supplies. The A and AN inputs should be driven differentially with the HIGH level at V_{CC} - 0.85 V and the LOW level equal to V_{CC} - 1.25 V and the B and BN inputs should be driven differentially with a voltage swing from -2.0 V to -2.4 V. Notice the ESD protection circuitry on the output, this circuitry is represented by the FPS009E schematic of Figure 16.

The H601 is also a dual supply device, however, both the input and output buffers are represented by one structure as shown in the H601 I/O Schematic of Figure 7. The H601 requires a single ended input, IN which should be driven from V_{CC} - 0.9 to V_{CC} - 1.75 V. Notice the “ECL in Pad Cell” on the input, this circuitry is represented by the “ECL Input Pad Cell” schematic of Figure 16, and includes the 50KΩ input pull down resistor and the ESD protection circuity for the ECL input. The same ESD structure is used on the output buffer section of the H601 I/O Structure as is used on the H600 output buffer. The H601 I/O buffer also requires one bias supply, CBIAS, and differential tritstate buffer inputs, TRI and TRIB. The CBIAS input should be set at 1.1 V , while the TRI and TRIB inputs should be driven by the “H601 ECL Input” structure of Figure 3.

The H603 Output gate is represented by the schematic of Figure 8. The IN and INB inputs should be driven differentially with voltage swings of V_{CC} to V_{CC} - 0.85 V. The CBIAS input should be forced to 1.1 V and the ENA input should be driven from VCC - 0.85 to VCC - 10.85 V.

The H603 again uses the same ESD protection scheme as the H600.

The H604 and H606 utilize the same output buffer. This buffer is represented by the “H604 Output Schematic” of Figure 11. The IN and INB inputs should be driven differentially with voltage swings from V_{CC} - 0.85 to V_{CC} - 10.85 V. Note, the ESD protection circuitry is the same as the H600.

Figure 12 represents the schematic for the output buffer utilized by the H605. The IN and INB inputs should be driven differentially from V_{CC} - 0.85 to V_{CC} - 10.85 V, while CBIAS is forced to 1.1 V. Again, the same ESD protection scheme is used as on the H600.

The H607 output buffer is represented by the schematic of Figure 13. The IN and INB inputs should be driven differentially from V_{CC} to V_{CC} - 1.8 V. The ESD protection circuitry is the same.

Two input structures can represent most of the inputs for the H60x family of translators, one for TTL inputs and one for ECL inputs. The exceptions were discussed previously and the various inputs and appropriate input models are summarized in Table 1. For the dual supply devices with ECL inputs, the V_{CC} and the V_{EE} on the typical ECL input gates should be tied to ground and -5.2 V respectively. All input pins should have both a package model and ESD protection circuitry connected to them. For TTL inputs, the ESD protection circuitry is represented by the FPS009E schematic of Figure 16. For ECL inputs, the ESD protection circuitry is represented along with a 50KΩ input pull down resistor as part of the “ECL in Pad Cell” represented in Figure 16. The “Package Model” of Figure 16 is self explanatory, the parasitic values provided are worst case numbers. The package capacitance combines with the parasitic transistor capacitance of the input device and the ESD circuitry to comprise the load capacitance of the input. The various input buffer ESD circuits are outlined in Figure 16; notice that the ECL inputs utilize a different structure than the TTL inputs and outputs. The typical ECL input schematic represents a single ended ECL input, the VBB reference should be tied to V_{CC} - 1.3 V and the VCS bias should be tied to V_{EE} + 1.3 V. To simulate a differential ECL input, one simply connects the complimentary input to the “V_{BB}” side of the input gate along with an associated ESD and package model. The differential input does not use the V_{BB} switching reference.

Table 1. Device Type Input Cross Reference

Part Type	ECL Inputs	TTL Inputs	H601 I/O	H606 TTL Inputs	H602 ECL Inputs	H601 ECL Inputs
H600	ECLST	TTLST, D0-D8	None	None	None	None
H601	None	TTLOE	D0-D8	None	None	ECLOE
H602	LEN, RESET	D0-D8	None	None	None	None
H603	All Inputs	None	None	None	None	None
H604	RESET, CLK, CLKN	CLKT, D0-D5	None	None	None	None
H605	All Inputs	None	None	None	None	None
H606	CLK, CLKN, RESET	None	None	CLKT, D0-D5	None	None
H607	All Inputs	None	None	None	None	None

For all of the input and output buffer schematics, the resistors should NOT be simulated as simple SPICE resistors. Because these resistors are realized by a diffusion step in wafer processing, there are parasitic capacitances associated with each. The subcircuit schematic is shown for the resistors in the “Resistor Model” schematic of Figure 16. The value of each subcircuit resistor is one half the value given on the top level schematic and the parasitic capacitance is modelled by a diode back biased to V_{CC}. Also, note that the resistor temperature coefficient (TC) values for both the resistor subcircuit and the resistors in the device subcircuits are provided. For modelling at nominal temperatures only, these TCs can be omitted. If, however, modelling will be performed at the temperature extremes, the TC information should be included.

Table 2 is provided to summarize the various internal voltage swings and bias levels required to run the appropriate SPICE simulations.

Table 2. Input and Bias Levels

Schematic	Input	Level
ECL Input	V_{BB} V_{CS}	V_{CC} - 1.3 V V_{EE} + 1.3 V
H600, H602 Output	A/AN B/BN V_{CS}	V_{CC} - 0.85 V to V_{CC} - 1.25 V V_{CC} - 2.0 V to V_{CC} - 2.4 V V_{EE} + 1.3 V
H601 I/O	IN CBIAS TRI/TRIB V_{CS} V_{BB}	V_{CC} - 0.85 V to V_{CC} - 1.85 V 1.1 V -2.1 V to -2.5 V V_{EE} + 1.3 V V_{CC} - 1.3 V
H603 Output	IN/INB ENA V_{CS} V_{BBP} CBIAS	V_{CC} to V_{CC} - 0.85 V V_{CC} - 0.85 V to V_{CC} - 1.85 V V_{EE} + 1.3 V V_{CC} - 2.1 V 1.1 V
H605 Output	IN/INB CBIAS V_{CS}	V_{CC} - 0.85 V to V_{CC} - 1.29 V 1.1 V V_{EE} + 1.3 V
H604, H606 Output	V_{CS}	V_{EE} + 1.3 V
H607 Output	IN/INB	V_{CC} to V_{CC} - 0.85 V

Handling Power Supplies

It is important to properly apply the power supply voltages to accurately model these circuits. This section will explain the power supply terminology used on the I/O buffer schematics and how to properly apply these supplies with the appropriate package model.

Table 3 lists the voltage supplies referenced on the I/O schematics along with a description of each. The key to proper simulating these power supplies is in the application of the package model. Because the output buffers, to a varying degree, share V_{CC} and ground pins, adjustments need to be made to get a more accurate model if all of the outputs are not simulated at the same time. If for example a single output is to be simulated, the package model for the TVCCI and TGNDI supplies should be scaled based on the number of outputs which normally share the supplies. If the simulated output normally shares its supplies with two other outputs, the package inductance would be tripled to simulate the same inductive glitch seen on the power pin in an actual application. The capacitive value for the package model is not as critical and thus can be left alone. This method will allow users to more accurately model an output behavior without resorting to more complicated and lengthy simulations. The internal power and ground pins are all powered through a single pin and are basically static; as a result, no adjustments are needed for the package models on these supplies. Table 4 outlines the internal power distribution for the H60x translators. This information can be used to determine the scaling factors for the package inductance for the output buffers. To use the table, simply identify the output in question and divide the number of outputs in the group by the number of power pins for that group; this will give the multiplication factor for the inductance.

Table 3. Power Pin Descriptions

Power	Description
EV_{CC}	EV_{CC} is the most positive supply for the ECL input gate (+5 V for the H607 and ground for H600-H606)
V_{EE}	V_{EE} is the most negative supply for an ECL gate. For the H607, it is equal to ground, for the H600-H606 it is equal to -5.2 V
TV_{CCI}	Internal V_{CC} for TTL circuitry
GNDI	Internal ground for TTL circuitry

Table 4. Power Pin versus Outputs

Part Type	Number of Outputs	Number TVCC	Number TGND
H600	9	3	N/A
H601	9	2	3
H602	9	3	N/A
H603	9	2	3
H604	12	3	N/A
H605	6	2	2
H606	3	3	N/A
H607	6	2	2

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk. However, with today's advanced design tools, it will probably be a simpler task to enter the schematics in a good schematic capture package than it will be to manipulate the generic netlists. If, however, the netlists are desired or questions arise about the contents of this document, the user can contact an ECL applications engineer for assistance.

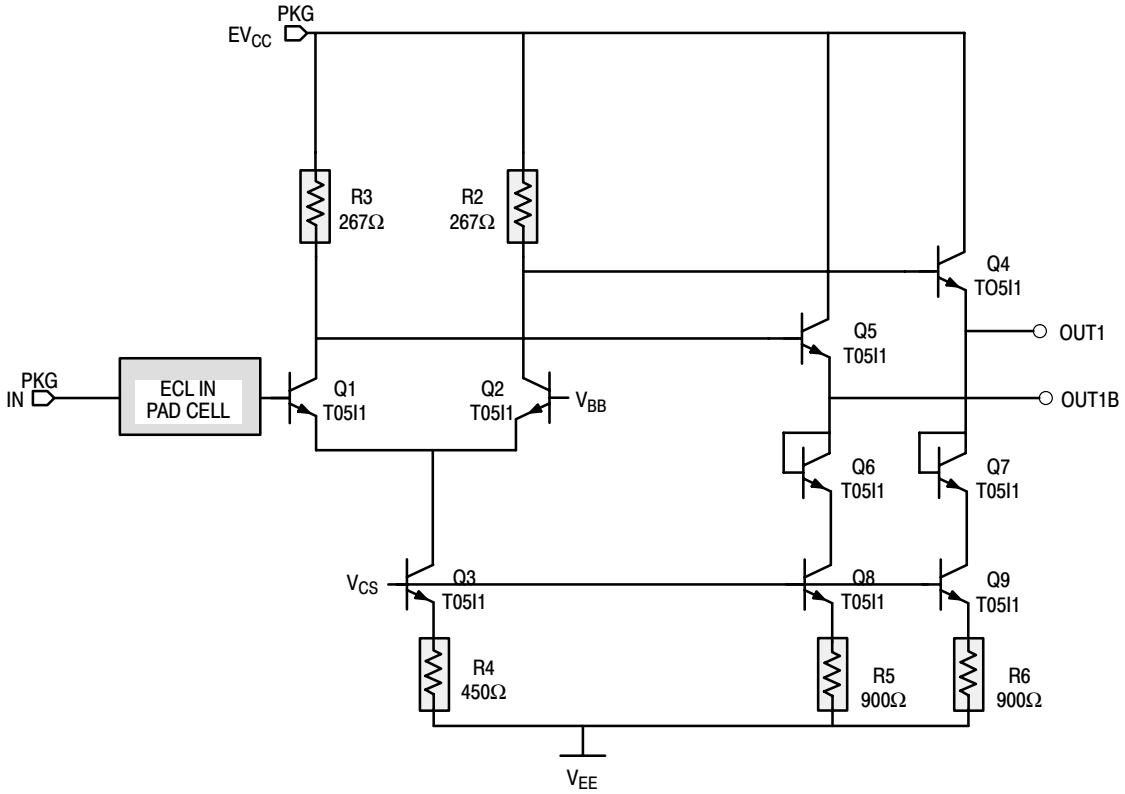


Figure 1. Typical ECL Input Gate

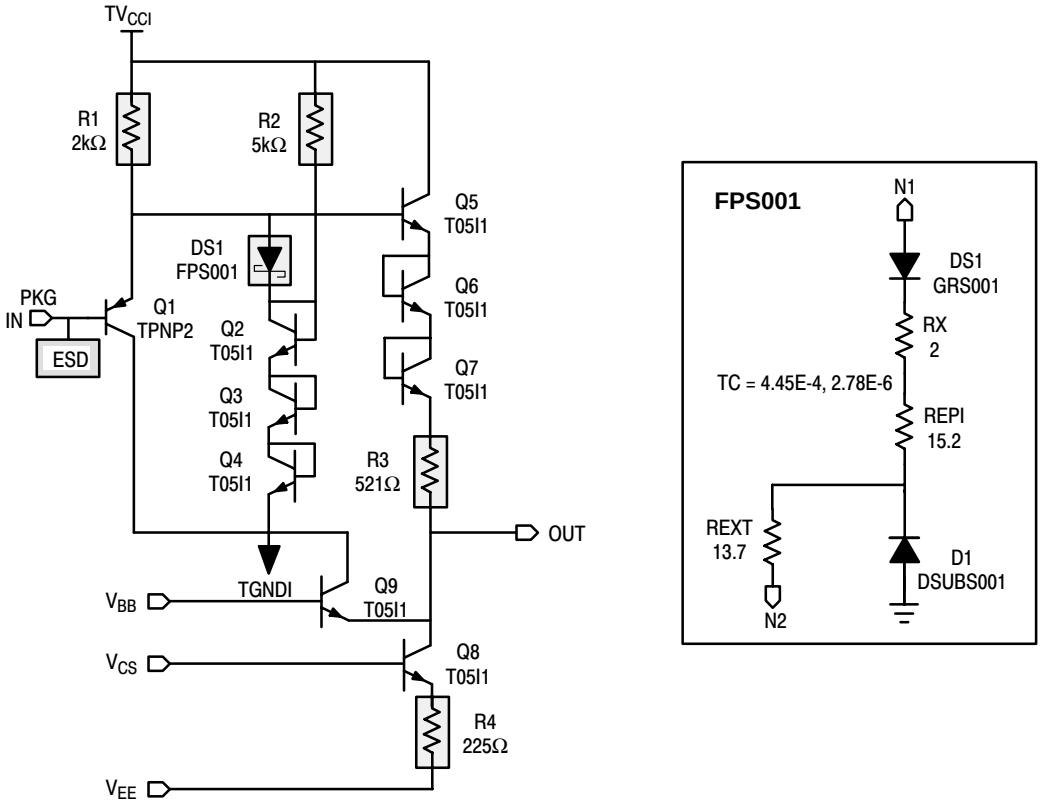


Figure 2. Typical TTL Input Gate

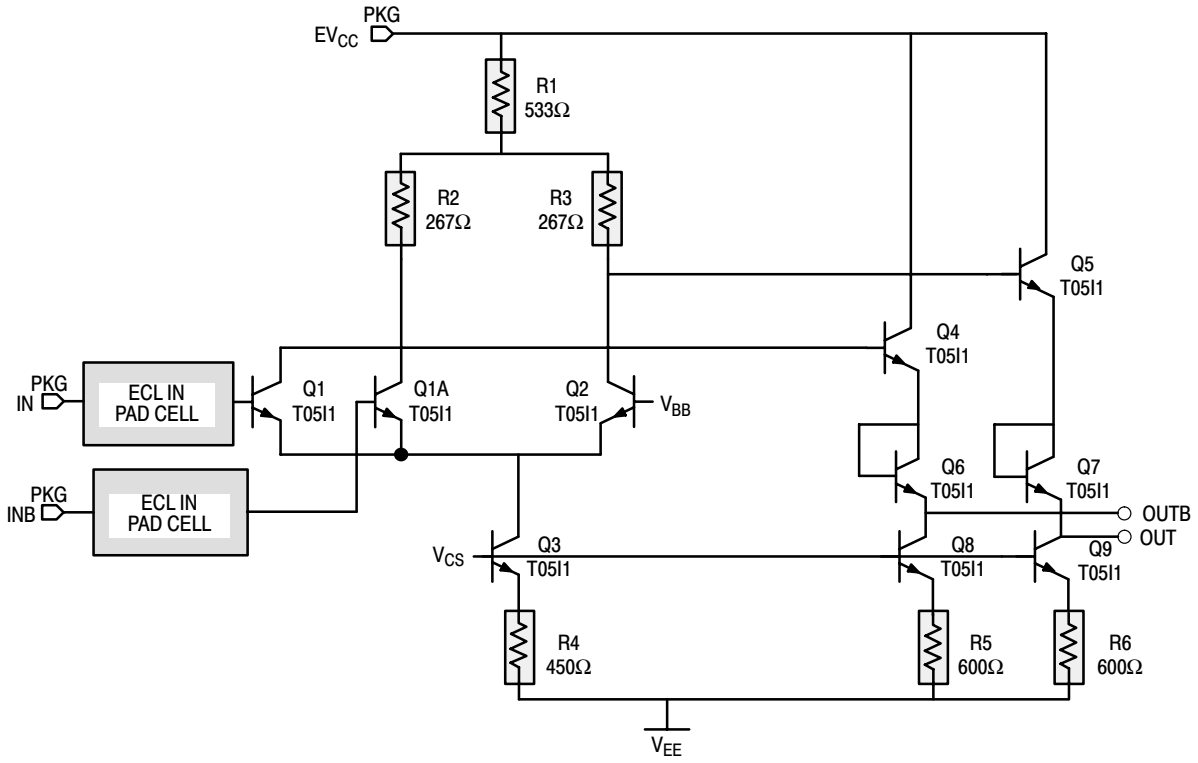


Figure 3. H601 ECL Input Gate

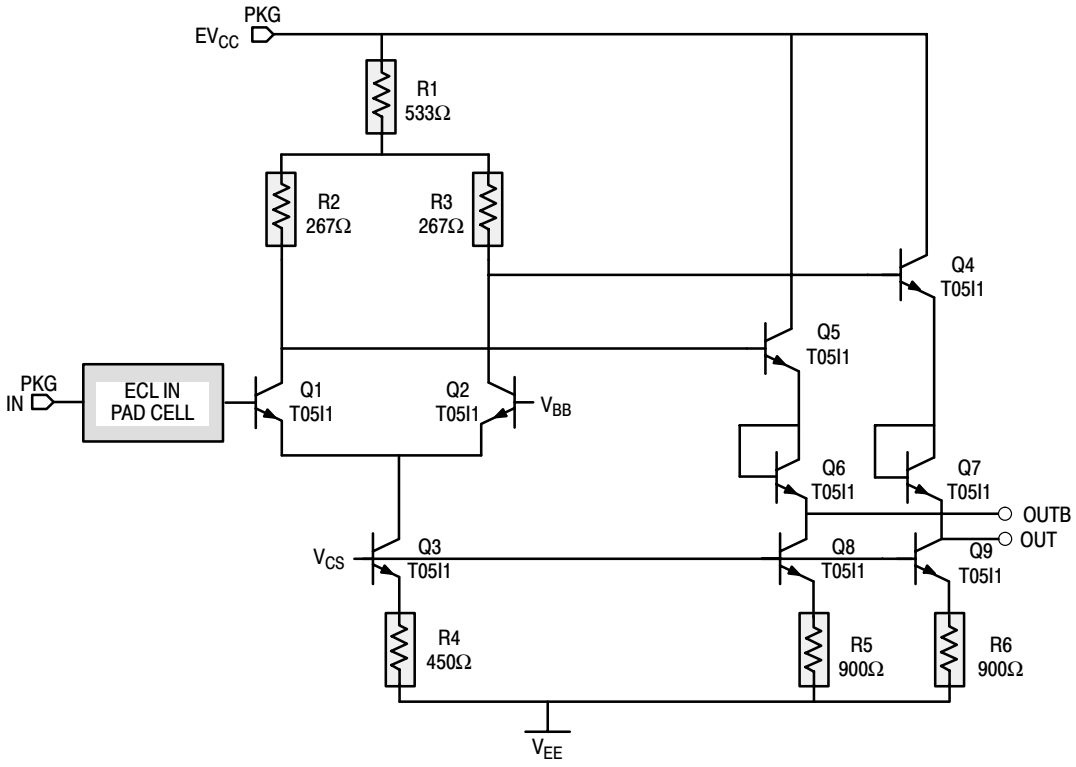


Figure 4. H602 ECL Input Gate

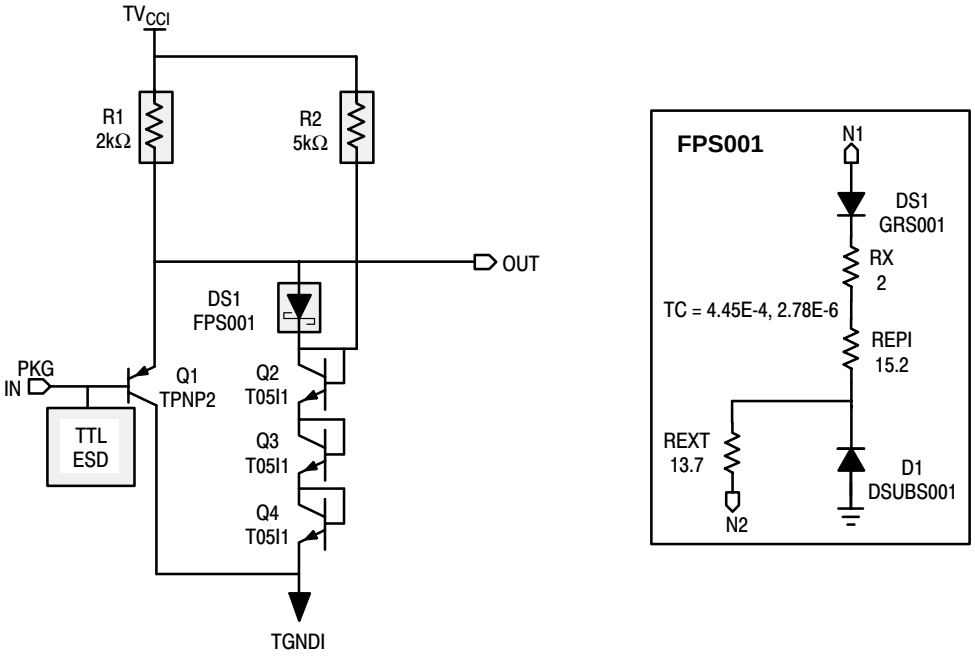


Figure 5. H606 TTL Input Gate

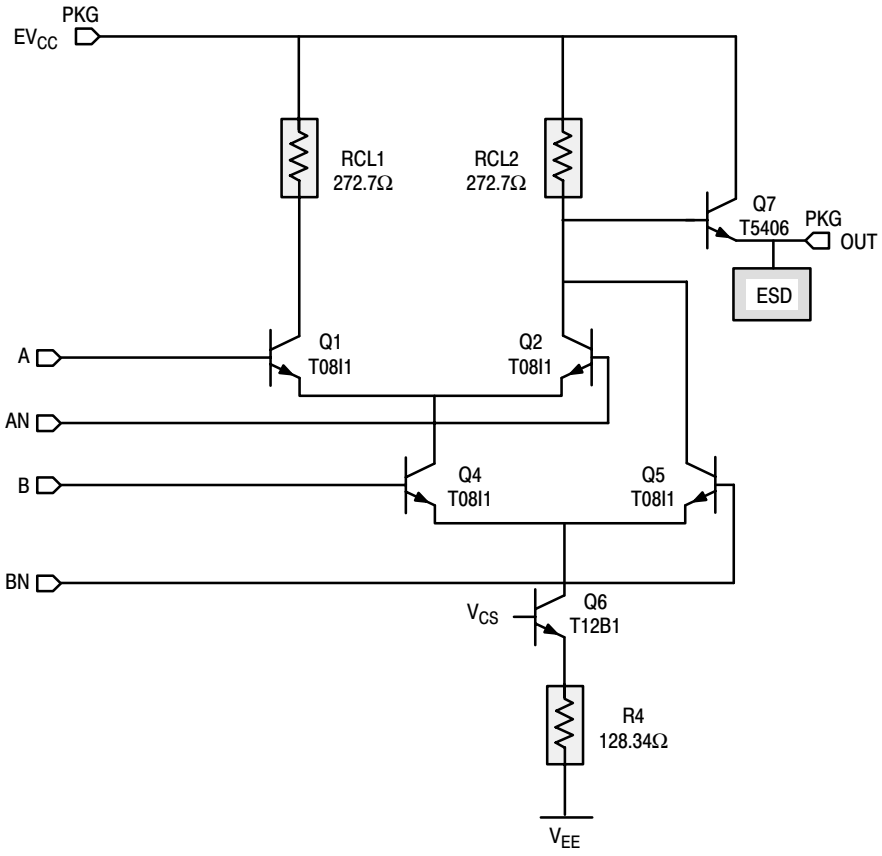


Figure 6. H600, H602 Output Gate

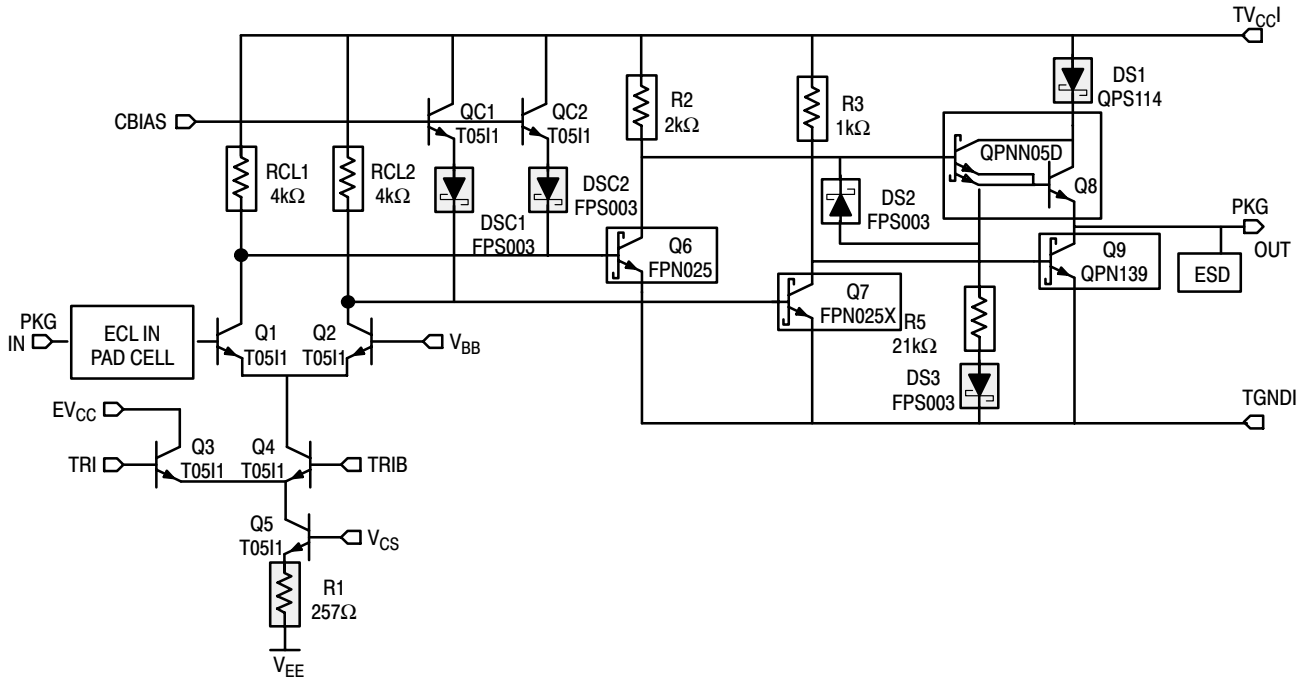


Figure 7. H601 I/O Gate

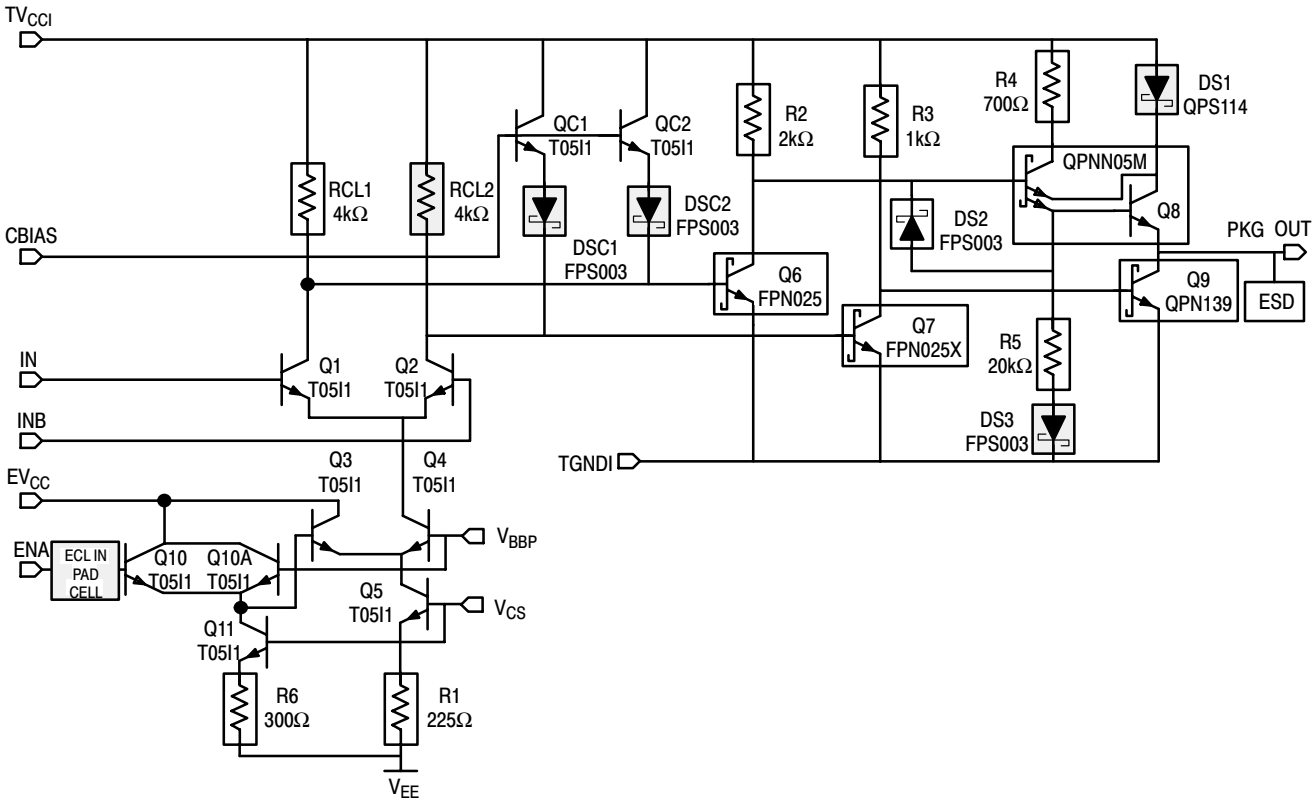
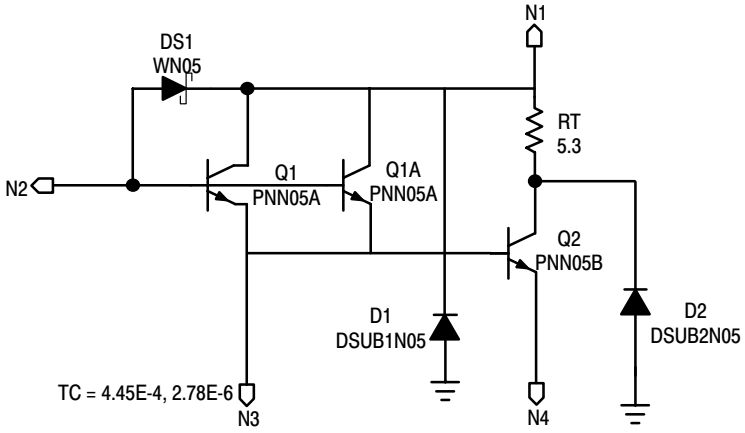


Figure 8. H603 Output Gate



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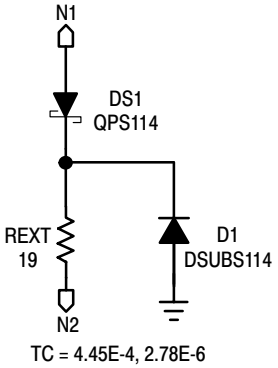
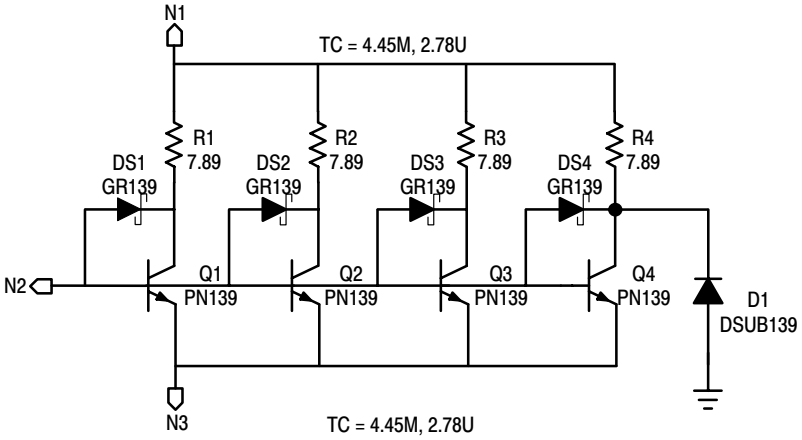
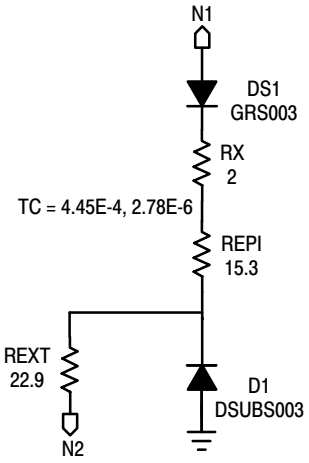


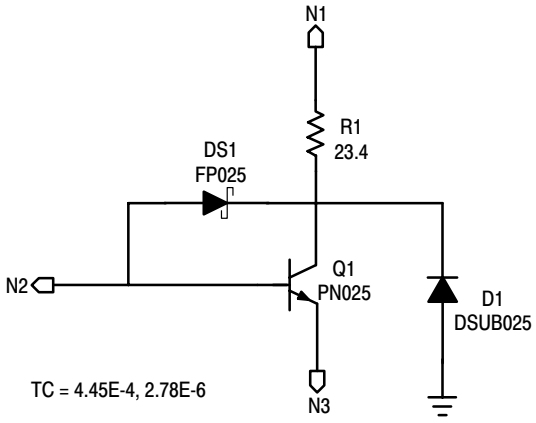
QPS114



QPN139



FPS003



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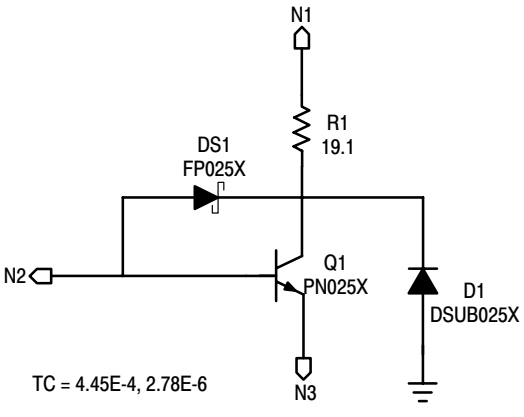
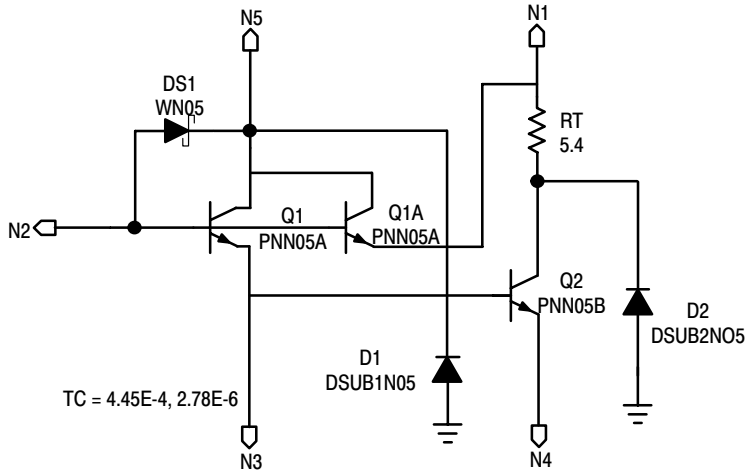


FPN025X

Figure 9. H601 Output Subcircuits



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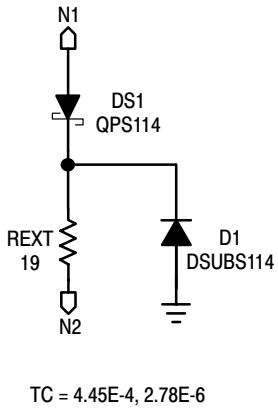

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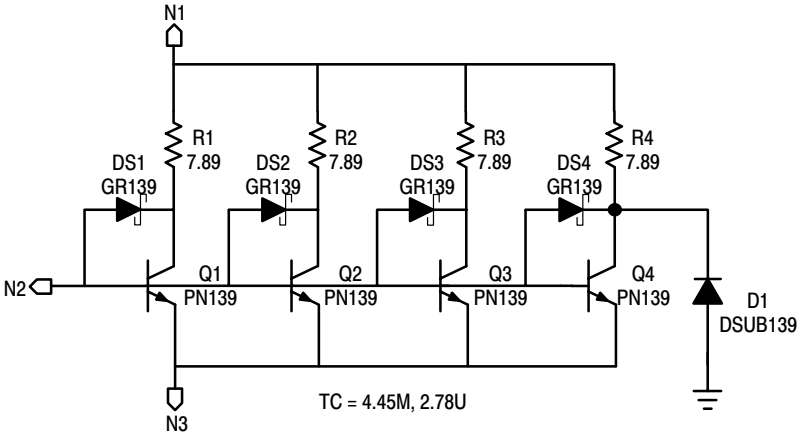

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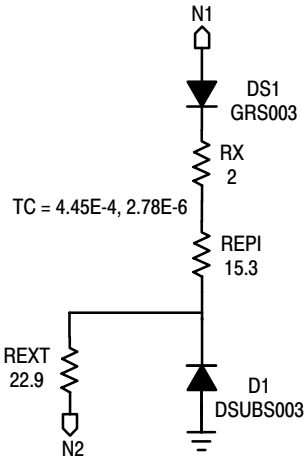

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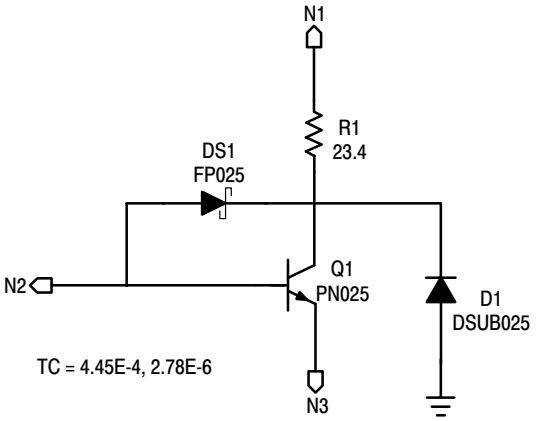

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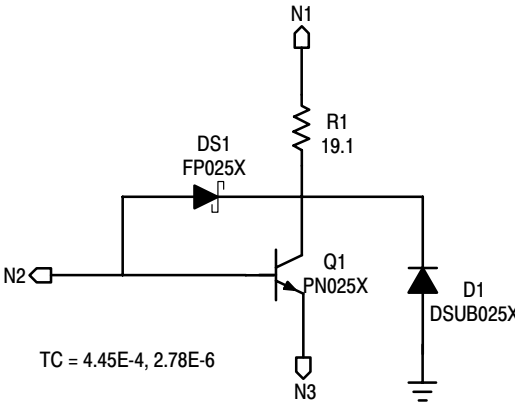

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Figure 10. H603 Output Subcircuits

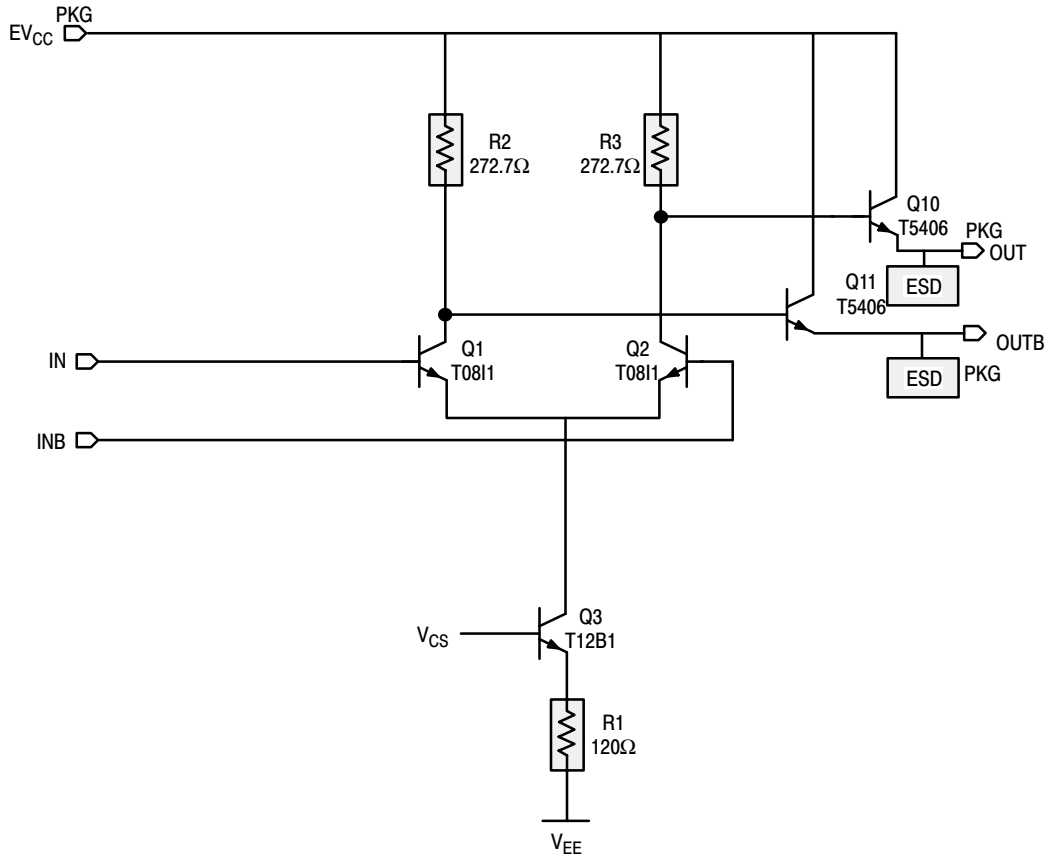


Figure 11. H604, H606 Output Gate

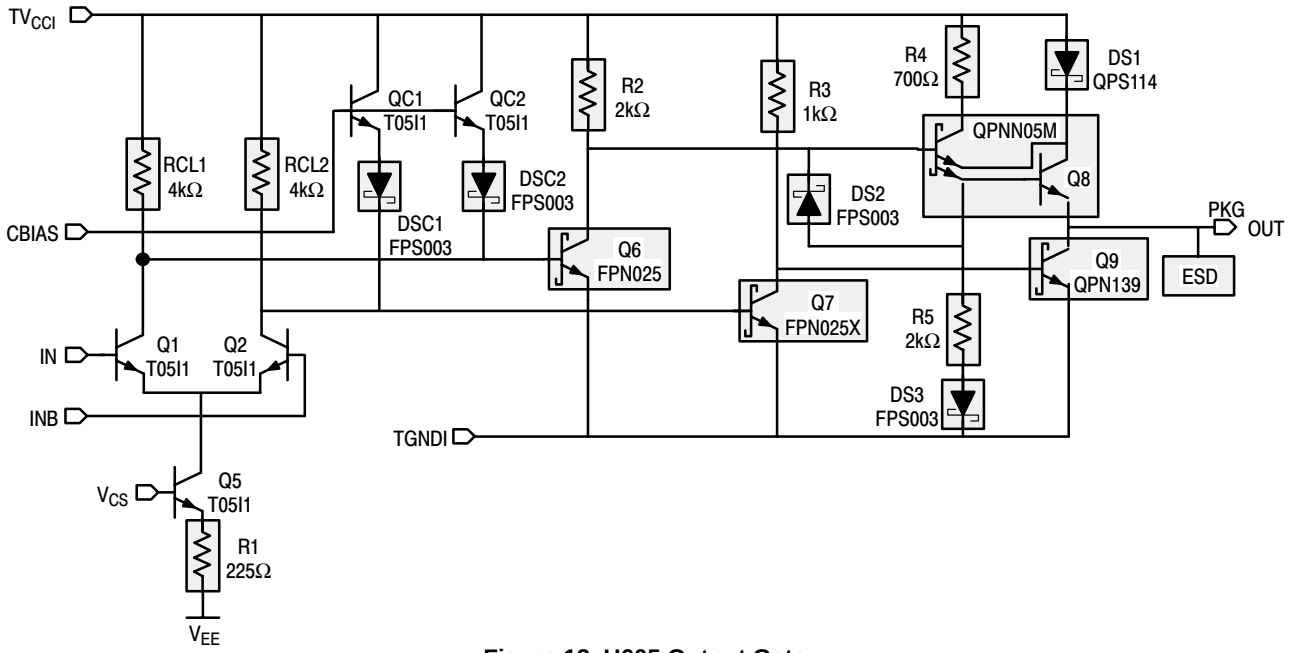


Figure 12. H605 Output Gate

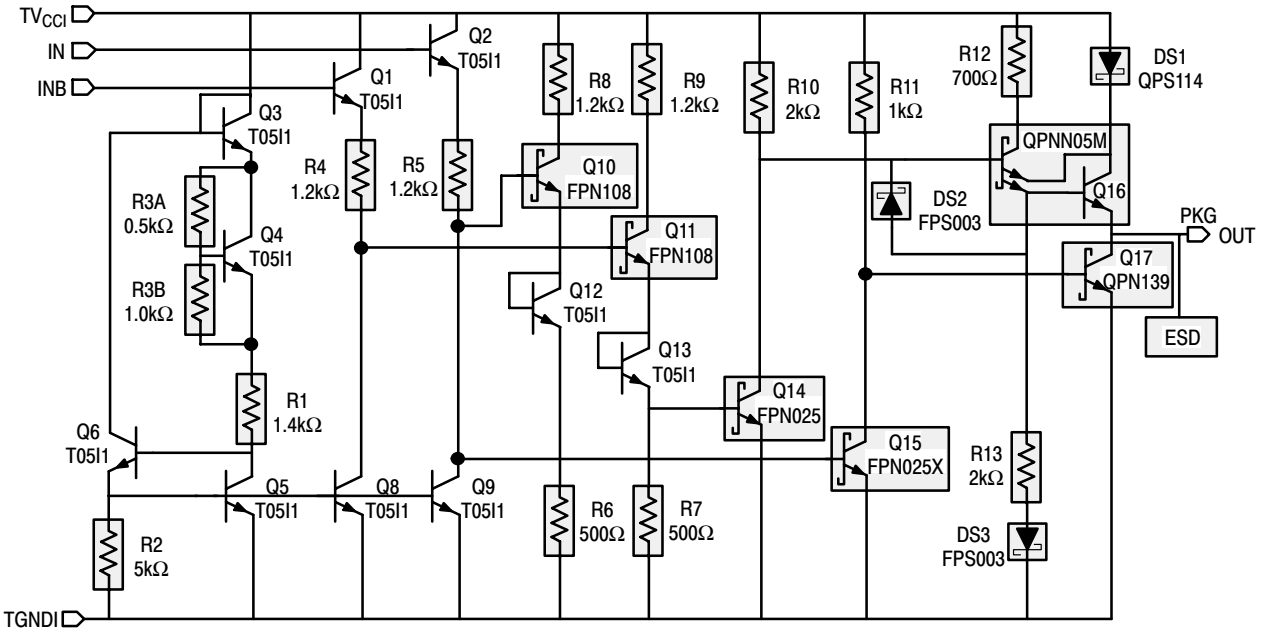


Figure 13. H607 Output Gate

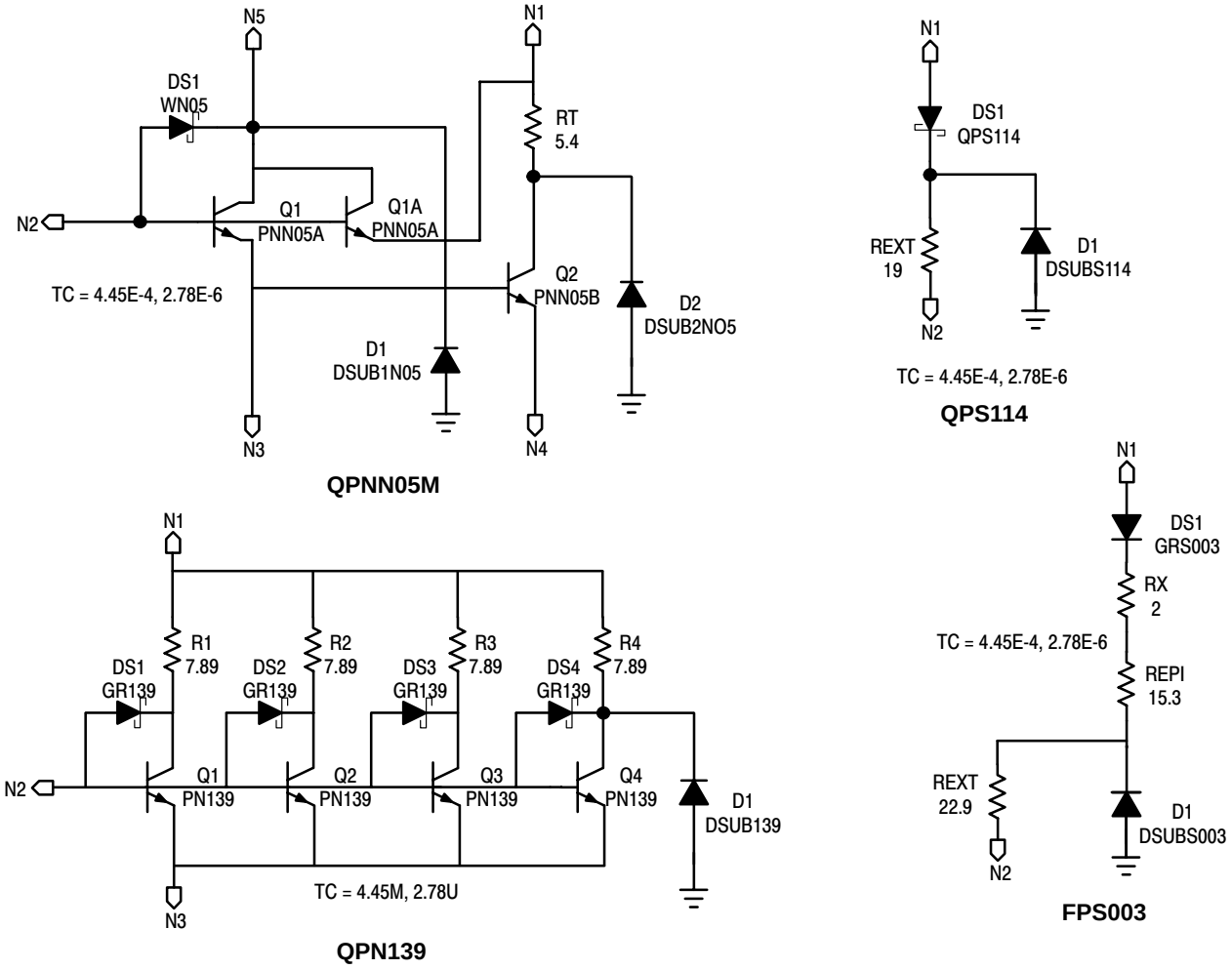
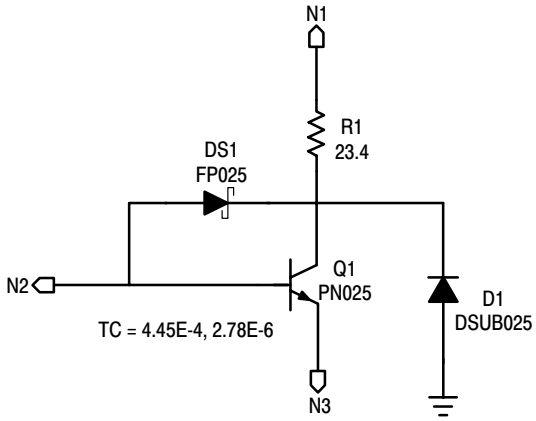


Figure 14. H607 Output Subcircuits



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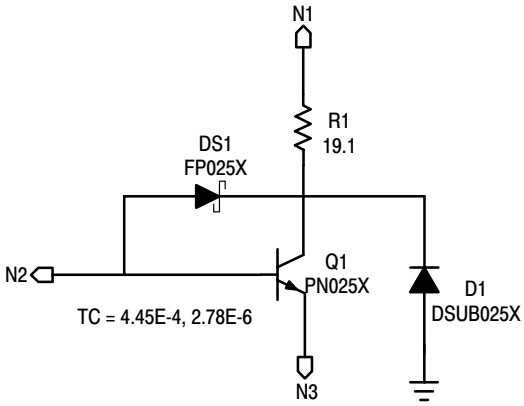

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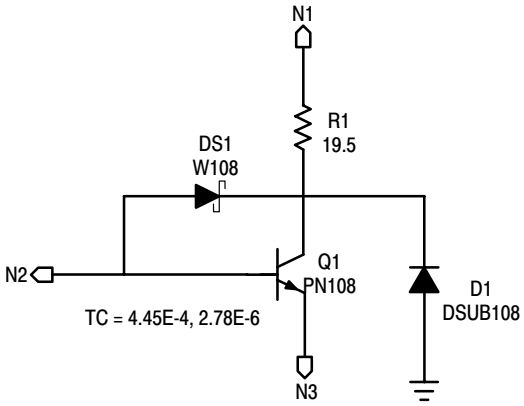

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Figure 15. H607 Output Subcircuits

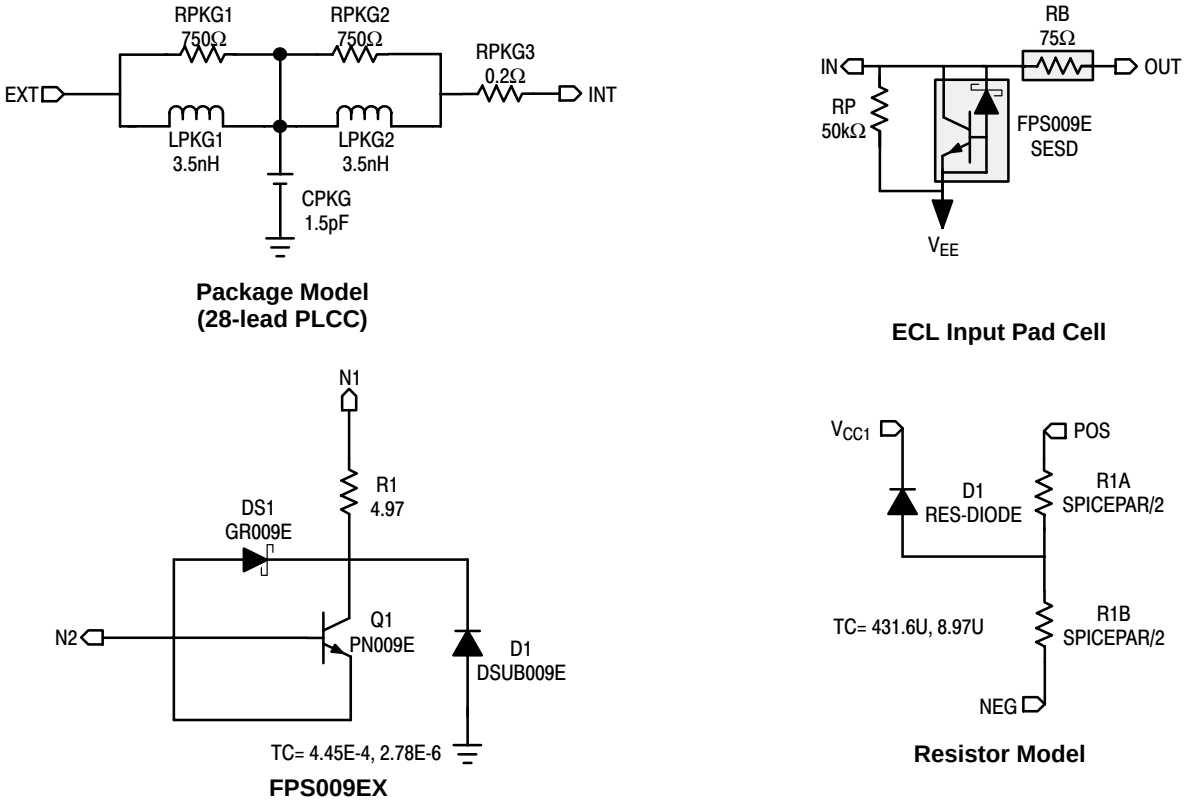

Figure 16. Miscellaneous Subcircuits

SPICE Parameter List

TTL Subcircuit Models

```
.MODEL GRS001 D          (IS=4.27E-14 RS=53 N=1.044 TT=10PS
+                        CJO=54FF VJ=.4 M=.33
+                        EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS001 D        (IS=1E-16 RS=0 N=1TTt=500PS
+                        CJO=87FF VJ=.51 M=.24
+                        EG=1.115 XTI=3 FC=.5 BV=35)
*
.MODEL DSUB1N05 D        (CJO=203FF VJ=.51 M=.24)
.MODEL DSUB2N05 D        (CJO=388FF VJ=.51 M=.24)
.MODEL PNN05A NPN        (IS=1.662E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+                        ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                        IKR=.7125MA ISC=1.803E-16 NC=1 RB=656.7 RBM=218
+                        RE=0 RC=91.62
+                        CJE=86.47FF VJE=.9 MJE=.4
+                        CJC=58.32FF VJC=.53 MJC=.37
+                        TF=40P XTF=0 VTF=100 ITF=3.89MA PTF=0
+                        TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL PNN05B NPN        (IS=1.583E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+                        ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                        IKR=6.78MA ISC=1.717E-15 NC=1 RB=77.29 RBM=31.25
+                        RE=0 RC=9.61
+                        CJE=751.6FF VJE=.9 MJE=.4
+                        CJC=445.2FF VJC=.53 MJC=.37
+                        TF=40P XTF=0 VTF=100 ITF=37.1MA PTF=0
+                        TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL WN05 D            (IS=1.0578E-12 RS=37.6 N=1.044 TT=10PS
+                        CJO=141.75FF VJ=.4 M=.33
+                        EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS114 D        (IS=1E-16 RS=0 N=1 TT=500PS
+                        CJO=2.75PF VJ=.51 M=.24
+                        EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL QPS114 D          (IS=2.52E-12 RS=1.35 N=1.044 TT=10PS
+                        CJO=2.1PF VJ=.4 M=.33
+                        EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB025X D        (CJO=284FF VJ=.51 M=.24)
.MODEL PN025X NPN        (IS=4.32E-17  BF=113 NF=1.008 VAF=30 IKF=10A
+                        ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                        IKR=10.85MA ISC=4.68E-16 NC=1 RB=175 RBM=65
+                        RE=0 RC=35.2
+                        CJE=193FF VJE=.9 MJE=.4
+                        CJC=158FF VJC=.53 MJC=.37
+                        TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
+                        TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025X D          (IS=1.08E-13 RS=48.3 N=1.044 TT=10PS
+                        CJO=90FF VJ=.4 M=.33
+                        EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB025 D         (CJO=284FF VJ=.51 M=.24)
.MODEL PN025 NPN         (IS=2.45E-17  BF=113 NF=1.008 VAF=30 IKF=10A
+                        ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                        IKR=1MA ISC=2.66E-16 NC=1 RB=193 RBM=89
+                        RE=0 RC=62
+                        CJE=123FF VJE=.9 MJE=.4
+                        CJC=108FF VJC=.53 MJC=.37
+                        TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
```

TTL Subcircuit Models - continued

```
+                       TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025 D          (IS=1.4E-13 RS=52 N=1.044 TT=10PS
+                       CJO=117FF VJ=.4 M=.33
+                       EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB139 D        (CJO=2.12PF VJ=.51 M=.24)
.MODEL PN139 NPN        (IS=1.03E-16  BF=113 NF=1.008 VAF=30 IKF=10A
+                       ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                       IKR=4.4MA ISC=1.22E-16 NC=1 RB=117 RBM=47
+                       RE=0 RC=8.41
+                       CJE=493FF VJE=.9 MJE=.4
+                       CJC=244FF VJC=.53 MJC=.37
+                       TF=40P XTF=0 VTF=100 ITF=96.7MA PTF=0
+                       TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR139 D          (IS=7E-14 RS=10 N=1.044 TT=10PS
+                       CJO=88FF VJ=.4 M=.33
+                       EG=.69 XTI=3 FC=.5 BV=30)
.MODEL GRS003 D         (IS=4.27E-14 RS=53 N=1.044 TT=10PS
+                       CJO=54FF VJ=.4 M=.33
+                       EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS003 D       (IS=1E-16 RS=0 N=1 TT=500PS
+                       CJO=127FF VJ=.51 M=.24
+                       EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUB009E D       (CJO=106FF VJ=.51 M=.24)
.MODEL PN009E NPN       (IS=3.92E-16  BF=113 NF=1.008 VAF=30 IKF=10A
+                       ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                       IKR=.3MA ISC=4.25E-15 NC=1 RB=185 RBM=39
+                       RE=0 RC=3.9
+                       CJE=1.37PF VJE=.9 MJE=.4
+                       CJC=609FF VJC=.53 MJC=.37
+                       TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+                       TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR009E D         (IS=5.4E-13 RS=9.57 N=1.044 TT=10PS
+                       CJO=683FF VJ=.4 M=.33
+                       EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB108 D        (CJO=163FF VJ=.51 M=.24)
.MODEL PN108 NPN        (IS=1.75E-17  BF=113 NF=1.008 VAF=30 IKF=10A
+                       ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                       IKR=.75MA ISC=1.9E-16 NC=1 RB=638.8 RBM=222
+                       RE=0 RC=87
+                       CJE=90.6FF VJE=.9 MJE=.4
+                       CJC=50.3FF VJC=.53 MJC=.37
+                       TF=40P XTF=0 VTF=100 ITF=4.1MA PTF=0
+                       TR=200p XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL W108 D           (IS=5.1E-13 RS=58.8 N=1.044 TT=10PS
+                       CJO=68.3FF VJ=.4 M=.33
+                       EG=.69 XTI=3 FC=.5 BV=30)
```

ECL Transistor Models

```
.MODEL T05I1 NPN
+                    IS=21.18E-18  BF=112   BR=5.108  RE=1.533  IKF=.0213 VAF=41.8
+                    ISE=250E-18   RB=52.7  RBM=0    IRB=0    IKR=53E-5 VAR=3.766
+                    ISC=95.62E-18 EG=1.11  RC=26.33  NC=1.141  NR=.997
+                    CJE=67.7E-15  VJE=1.037 MJE=.5718 NF=1.000  XTI=4.7
+                    CJC=99.5E-15  VJC=.603  MJC=.266  NE=2.000  XTB=1.15
+                    CJS=152E-15   VJS=.5052 MJS=.3465 TR=9.92E-9 PTF=20
+                    TF=35E-12     XTF=2.25  VTF=1.67  ITF=.00808 XCJC=.069 FC=.8
.MODEL TPNP2 PNP
+                    IS=7.69E-17 BF=5 BR=1 RB=164 RC=56 CJE=.086E-12
+                    CJC=1.4E-12
.MODEL T08I1 NPN
+                    IS=33.33E-18  BF=114.5  BR=2.029  RE=1.333  IKF=.0336 VAF=42.7
+                    ISE=1.0E-15   RB=56.6   RBM=0     IRB=0     IKR=.115  VAR=3.665
+                    ISC=184.7E-18 EG=1.11   RC=22.86  NC=1.085  NR=.995
+                    CJE=99.3E-15  VJE=1.037 MJE=.5718 NF=1.000  XTI=4.7
+                    CJC=124.4E-15 VJC=.603  MJC=.266  NE=2.000  XTB=1.15
+                    CJS=170.4E-15 VJS=.5052 MJS=.3465 TR=9.92E-9 PTF=40
+                    TF=35E-12     XTF=2.25  VTF=1.67  ITF=.00808 XCJC=.089 FC=.8
.MODEL T12B1 NPN
+                    IS=5.7E-17    BF=113    BR=1.116  RE=1.25    IKF=.0828  VAF=4
+                    ISE=2.4E-15   RB=170    RBM=170   IRB=1.7E-3 IKR=.27    VAR=3.6
+                    ISC=1.01E-16  EG=1.11   RC=13.3   NC=1.028   NR=1.019   XTI=3
+                    CJE=15E-15    VJE=.658  MJE=.273  NF=1.000
+                    CJC=27e-15    VJC=.603  MJC=.369  NE=2.000
+                    CJS=101E-15   VJS=.429  MJS=.259  TR=5E-9
+                    TF=39E-12   XTFf=3    VTF=1.4   ITF=.008  XCJC=.620  FC=.005
.MODEL T5406   NPN
+                    IS=3.3E-16  BF=113   RB=86.6 BR=5
+                    RC=23.6 RE=.833 CJE=.495E-12 CJC=.722E-12 CJS=.576E-12
```

Resistor Diode Model

```
.MODEL RES-DIODE D (IS=1E-16 TT=1NS VJ=.759V M=.333 CJO=50FF )
```

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