

## ECLinPS and ECLinPS Lite™ SPICE Modeling Kit

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### APPLICATION NOTE

#### Objective

The objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modeling for the current devices of the standard ECLinPS and ECLinPS Lite logic line, ON Semiconductor's high performance ECL family. The kit is not intended to provide information necessary to perform circuit level modeling on ECLinPS devices. With packaged gate delays of 300 ps and output edge rates as low as 175 ps, this family defines the state-of-the-art in ECL logic. The ECLinPS line is one of ON Semiconductor's high performance ECL/PECL family of products.

#### Device Input and Output Buffers Schematic Information

The kit contains representative input and output schematics, netlists, and waveform used for the standard ECLinPS and ECLinPS Lite devices. This application note will be modified as new devices are added.

There are four terminals on all transistor models: Emitter, Base, Collector, and Substrate (biased to  $V_{EE}$ ). Table 1 describes the nomenclature used in the schematics and netlists.

**Table 1. Schematics and Netlist Nomenclature**

$V_{CC}$	5 V FOR PECL AND (0 V) FOR ECL
$V_{EE}$	-5 V FOR ECL AND (0 V) FOR PECL
GND	0 V
$V_{TT}^*$	$V_{CC} - 2$ V TERMINATION PLANE*
IN	TRUE INPUT TO CKT
INB or $\overline{IN}$	INVERTED INPUT TO CKT
Q	TRUE OUTPUT OF CKT
QB or $\overline{Q}$	INVERTED OUTPUT OF CKT

\*Except for EL89,  $V_{TT} = V_{CC} - 3$  V

#### Package

A case model for various package types is included to improve the accuracy of the system model (see Table 2). The package model represents the parasitics as they are measured on a pin. The package pin model should be placed on each device input pin connecting to an input model, all device output pins connecting to an output model,  $V_{CC}$ , and

$V_{EE}$ . A model can be used at the  $V_{EE}$  pin: but is not necessary since the current in the  $V_{EE}$  pin is a constant. The Appendix A includes explanation on the package models nodes. For package model CDIP-16 only a center and end pin values are provided. Remaining pins may be ratio values between those two given pins.

**Table 2. Available Packages**

Package Model	Page Number
SO-8	15
TSSOP-8	17
SO-20	19
PLCC-28	25
PLCC-20	32
CDIP-16	33

#### Input Buffer

The typical input buffer schematic is shown in Figure 2 (INBUFTYPICAL), and by netlist to represent the general structure currently in use on the existing devices in this family. The schematics require the addition of ESD models (Figure 9) and package models (see Table 2) to more accurately model behavior of the certain device. The internal input pulldown resistor,  $R_{PD}$ , is shown in Figure 2. Single ended operation is shown although differential operation may be represented by changing  $V_{BB}$  to INB (INVERTED INPUT TO CKT). The INB node will require ESD, package, and  $R_{PD}$  models. Revise the netlist accordingly. It is unnecessary to include an ESD or Package model for the  $V_{BB}$  pins of the models because  $V_{BB}$  is intended as an internal node for most applications. If  $V_{BB}$  is modeled as an external node it is usually bypassed because it is a constant voltage, and adding ESD and Package parameters provide no additional benefit.

#### Output Buffer

The output buffer schematics (see Table 3) and netlists may contain the temperature compensation structure, so only the ESD and package models need to be added. Use the proper ESD structure from Figure 9: for EL series devices use "ECLinPS Lite ESD Circuitry", and for E series devices use "ECLinPS ESD Circuitry". For the EL series Output

modeling, delete the 185 Ω series resistor in the ESD schematic, ECLinPS Lite ESD Circuitry.

Any input or output that is driving or being driven by an off chip signal should include the ESD and package models. The output buffers show differential inputs and outputs. When simulating a single ended output, the termination or load resistor, package model, ESD structure and output emitter follower, of the unused output, should not be eliminated to simplify the system model.

**SPICE Netlists**

The netlists are organized as a group of subcircuits. In each subcircuit model netlist, the model name is followed by a list of node interconnects.

**Temperature Compensation Network for 100 Series**

The output netlists include temperature compensation network circuitry for 100 style output buffers. The temperature compensation circuitry should be placed as pictured in the output buffer schematics with L and R representing left and right of the schematic. The circuit components of the temperature compensation networks are shown in Figure 8. For simulating 10 style outputs these components should either be deleted or commented out of the subcircuit netlists.

**SPICE Parameter Information**

In addition to the schematics and netlists is a listing of the SPICE parameters for the transistors referenced in the schematics and netlists. These parameters represent a typical device of a given transistor. Varying the typical parameters will affect the DC and AC performance of the structures; but for the type of modeling intended by this note, the actual delay times are not necessary and are not modeled, as a result variation of the device parameters are meaningless. The performance levels are more easily varied by other methods and will be discussed in the next section. The resistors referenced in the schematics are polysilicon and have little parasitic capacitance in the real circuit so none is required in the model. The schematics display the only devices needed in the SPICE netlists.

**Modeling Information**

The bias drivers for the devices are not detailed since their circuitry would result in a substantial increase of model complexity and simulation time. Instead, these internal reference voltages (V<sub>BB</sub>, LVCS, Etc.) should be driven with ideal constant voltage sources.

The typical interconnect schematic has been modeled to provide an output waveform of the ECLinPS Line. The

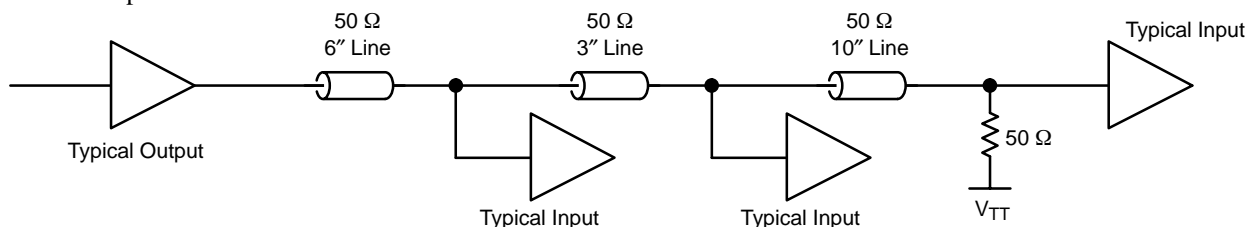


Figure 1. Typical Application for I/O SPICE Modeling Kit

typical input buffer may be driven with output buffer as shown in Figure 10. The schematics and SPICE parameters will provide a typical output waveshape, which can be seen in Figure 11. Simple adjustments can be made to the models allowing output characteristics to simulate conditions at or near the corners of some of the data book specifications. Consistent cross-point voltages need to be maintained.

- To adjust rise and fall times:
 

Produce the desired rise and fall times output slew rates by adjusting collector load resistors to change the gates tail current. The V<sub>CS</sub> voltage will affect the tail current in the output differential, which will interact with the load resistor and collector resistor to determine t<sub>r</sub> and t<sub>f</sub> at the output.
- To adjust the V<sub>OH</sub>:
 

Adjust the V<sub>OH</sub> and V<sub>OL</sub> level by the same amount by varying V<sub>CC</sub>. The output levels will follow changes in V<sub>CC</sub> at a 1:1 ratio.
- To adjust the V<sub>OL</sub> only:
 

Adjust the V<sub>OL</sub> level independently of the V<sub>OH</sub> level by increasing or decreasing the collector load resistance. Note that the V<sub>OH</sub> level will also change slightly due to a I<sub>BASER</sub> drop across the collector load resistor. V<sub>OL</sub> can be changed by varying the V<sub>CS</sub> supply, and therefore the gate current through the current source resistor.

**Summary**

The information included in this kit provides adequate information to run a SPICE level system interconnect simulation. The block diagram in Figure 1 illustrates a typical situation which can be modeled using the information in this kit. Device input or output models are presented in Table 4 and Table 5.

Table 3. Buffer Model Figures

Buffer Model	Figure Number	Page Number
OBUF_A	3	6
OBUF_B	4	7
OBUF_C	5	8
OBUF_D	6	9
OBUF_E	7	10
INBUFTYPICAL	2	5

Table 4. E Input/Output Selection

Device	Function	All Inputs	Output
E016	8 bit Sync. Binary Up Counter	INBUFTYPICAL	OBUF_A
E101	Quad 4 input OR/NOR Gate	INBUFTYPICAL	OBUF_A
E104	Quint 2 input AND/NAND Gate	INBUFTYPICAL	OBUF_A
E107	Quint 2 input XOR/XNOR Gate	INBUFTYPICAL	OBUF_A
E111	1:9 Diff. Clock Driver	INBUFTYPICAL	OBUF_A
E112	Quad Driver	INBUFTYPICAL	OBUF_A
E116	Quint Diff. Line Receiver	INBUFTYPICAL	OBUF_A
E122	9 Bit Buffer	INBUFTYPICAL	OBUF_A
E131	4 Bit D Flip-Flop	INBUFTYPICAL	OBUF_A
E136	6 Bit Universal Up/Down Counter	INBUFTYPICAL	OBUF_A
E137	8 Bit Ripple Counter	INBUFTYPICAL	OBUF_A
E141	8 Bit Shift Register	INBUFTYPICAL	OBUF_A
E142	9 Bit Shift Register	INBUFTYPICAL	OBUF_A
E143	9 Bit Hold Register	INBUFTYPICAL	OBUF_A
E150	6 Bit D Latch	INBUFTYPICAL	OBUF_A
E151	6 Bit D Register	INBUFTYPICAL	OBUF_A
E154	5 Bit 2:1 Mux-Latch	INBUFTYPICAL	OBUF_A
E155	6 Bit 2:1 Mux-Latch	INBUFTYPICAL	OBUF_A
E156	3 Bit 4:1 Mux-Latch	INBUFTYPICAL	OBUF_A
E157	Quad 2:1 Multiplexer	INBUFTYPICAL	OBUF_A
E158	5 Bit 2:1 Multiplexer	INBUFTYPICAL	OBUF_A
E160	12 Bit Parity Generator/Checker	INBUFTYPICAL	OBUF_A
E163	2 Bit 8:1 Multiplexer	INBUFTYPICAL	OBUF_A
E164	16:1 Multiplexer	INBUFTYPICAL	OBUF_A
E166	9 Bit Magnitude Comparator	INBUFTYPICAL	OBUF_A
E167	6 Bit 2:1 Mux-Register	INBUFTYPICAL	OBUF_A
E171	3 Bit 4:1 Multiplexer	INBUFTYPICAL	OBUF_A
E175	9 Bit Latch with Parity	INBUFTYPICAL	OBUF_A
E193	Error Detection/Correction Circuit	INBUFTYPICAL	OBUF_A
E195	Programmable Delay Chip	INBUFTYPICAL	OBUF_B
E196	Programmable Delay Chip	INBUFTYPICAL	OBUF_B
E197	Data Separator	INBUFTYPICAL	OBUF_A
E210	Dual 1:4, 1:5 Diff. Fanout Buffer	INBUFTYPICAL	OBUF_A
E211	1:6 Diff. Clock Distribution Chip	INBUFTYPICAL	OBUF_B
E212	3 Bit Scannable Registered Address Driver	INBUFTYPICAL	OBUF_B
E241	8 Bit Scannable Register	INBUFTYPICAL	OBUF_A
E256	3 Bit 4:1 Mux-Latch	INBUFTYPICAL	OBUF_A
E310	Low Voltage 2:8 Diff. Fanout Buffer	INBUFTYPICAL	OBUF_A
E336	3 Bit Registered Bus Transceiver	INBUFTYPICAL	OBUF_C
E337	3 Bit Scannable Registered Bus Transceiver	INBUFTYPICAL	OBUF_C
E404	Quad Diff. AND/NAND	INBUFTYPICAL	OBUF_B
E411	1:9 Diff. PECL/NECL RAMBus Clock Buffer	INBUFTYPICAL	OBUF_A

Table 4. E Input/Output Selection

E416	Quint Diff. Line Receiver	INBUFTYPICAL	OBUF_D
E431	3 Bit Diff. Flip-Flop	INBUFTYPICAL	OBUF_A
E445	4 Bit Serial/Parallel Converter (pins 17, 18 OBUF_B)	INBUFTYPICAL	OBUF_A
E446	4 Bit Parallel/Serial Converter (pins 14, 15 OBUF_B)	INBUFTYPICAL	OBUF_A
E451	6 Bit D Register Diff. Data and Clock	INBUFTYPICAL	OBUF_A
E452	5 Bit Diff. Register	INBUFTYPICAL	OBUF_A
E457	Triple Diff. 2:1 Multiplexer	INBUFTYPICAL	OBUF_B
E1651	Dual ECL Output Comparator with Latch	INBUFTYPICAL	OBUF_A
E1652	Dual ECL Output Comparator with Latch	INBUFTYPICAL	OBUF_A

Table 5. EL Input/Output Selection

Device	Function	All Inputs	Output
EL01	4 input OR/NOR	INBUFTYPICAL	OBUF_B
EL04	2 input Diff. AND/NAND	INBUFTYPICAL	OBUF_B
EL05	3 input AND/NAND	INBUFTYPICAL	OBUF_B
EL07	3 input XOR/XNOR	INBUFTYPICAL	OBUF_B
EL11	1:2 Diff. Fanout Buffer	INBUFTYPICAL	OBUF_B
EL12	Low Impedance Driver	INBUFTYPICAL	OBUF_B
EL13	Dual 1:3 Fanout Buffer	INBUFTYPICAL	OBUF_A
EL14	1:5 Clock Distribution Chip	INBUFTYPICAL	OBUF_A
EL15	1:4 Clock Distribution Chip	INBUFTYPICAL	OBUF_A
EL16	Diff. Receiver	INBUFTYPICAL	OBUF_B
EL17	Quad Diff. Receiver	INBUFTYPICAL	OBUF_A
EL29	Dual Diff. Data and Clock D Flip-Flop with Set&Reset	INBUFTYPICAL	OBUF_A
EL30	D Flip-Flop with Set&Reset	INBUFTYPICAL	OBUF_A
EL31	Triple D Flip-Flop with Set&Reset	INBUFTYPICAL	OBUF_B
EL32	2 Divider	INBUFTYPICAL	OBUF_B
EL33	4 Divider	INBUFTYPICAL	OBUF_B
EL34	2, 4, 8 Clock Generation Chip	INBUFTYPICAL	OBUF_A
EL35	JK Flip-Flop	INBUFTYPICAL	OBUF_B
EL38	2, 4/6 Clock Generation Chip	INBUFTYPICAL	OBUF_A
EL39	2/4, 4/6 Clock Generation Chip	INBUFTYPICAL	OBUF_A
EL51	Diff. Clock D Flip-Flop	INBUFTYPICAL	OBUF_B
EL52	Diff. Data and Clock D Flip-Flop	INBUFTYPICAL	OBUF_B
EL56	Dual Diff. 2:1 Multiplexer	INBUFTYPICAL	OBUF_A
EL57	4:1 Diff. Multiplexer	INBUFTYPICAL	OBUF_B
EL58	2:1 Multiplexer	INBUFTYPICAL	OBUF_A
EL59	Triple 2:1 Multiplexer	INBUFTYPICAL	OBUF_A
EL89 *	Coaxial Cable Driver *	INBUFTYPICAL	OBUF_E
EL90	Triple ECL Input to PECL Output Translator	INBUFTYPICAL	OBUF_A
EL91	Triple LVPECL/PECL Input to -5V ECL Output Translator	INBUFTYPICAL	OBUF_A

\*EL89 has an output swing of 1.6 V and it is terminated 50  $\Omega$  to  $V_{CC} - 3 V$  (see Figure 7)

Netlists and Schematics

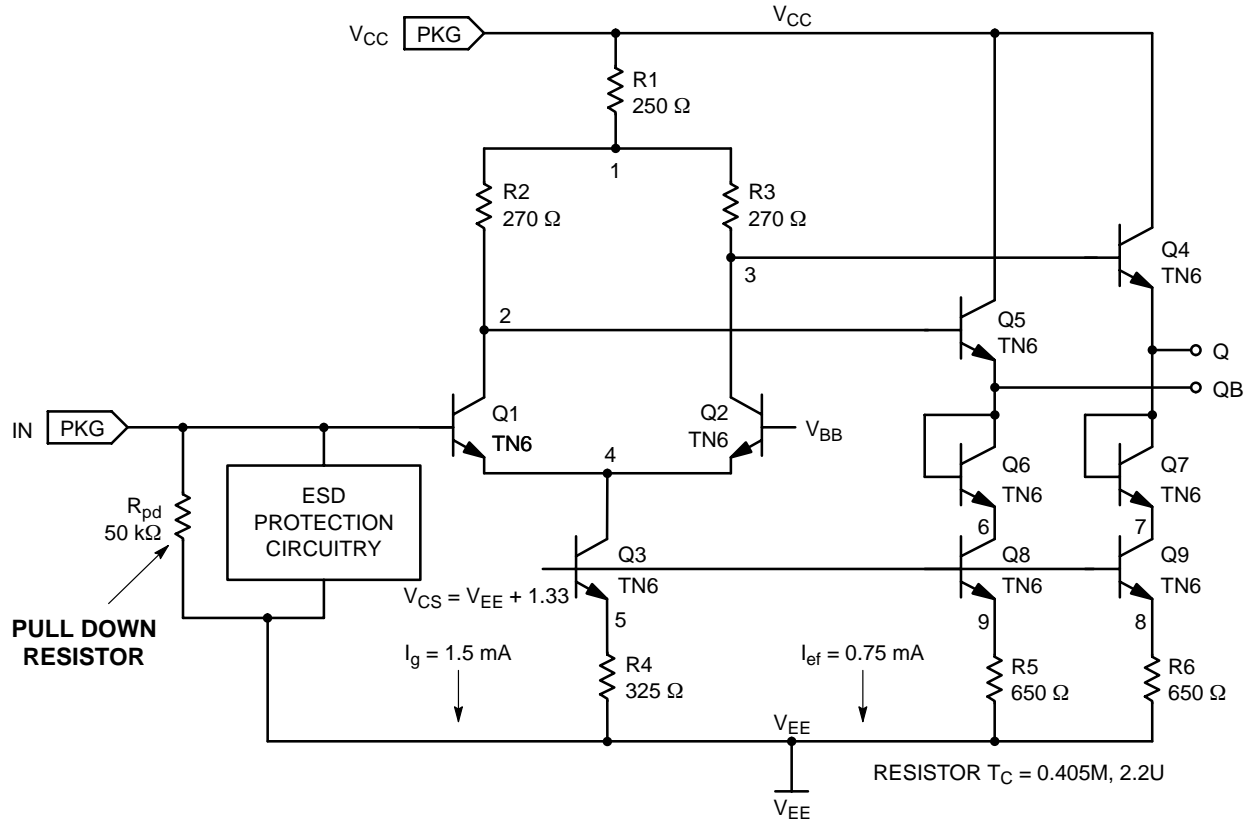


Figure 2. Typical Input Buffer (INBUFTYPICAL)

```
.SUBCKT INBUFTYPICAL
Q1      2 IN 4 TN6
Q2      3 VBB 4 TN6
Q3      4 VCS 5 TN6
Q4      VCC 3 Q TN6
Q5      VCC 2 QB TN6
Q6      QB QB 6 TN6
Q7      Q  Q 7 TN6
Q8      6 VCS 9 TN6
Q9      7 VCS 8 TN6
R1      VCC 1 250
R2      1 2 270
R3      1 3 270
R4      5 VEE 325
R5      9 VEE 650
R6      8 VEE 650
RPD     IN VEE 50K
.ENDS INBUFTYPICAL
```

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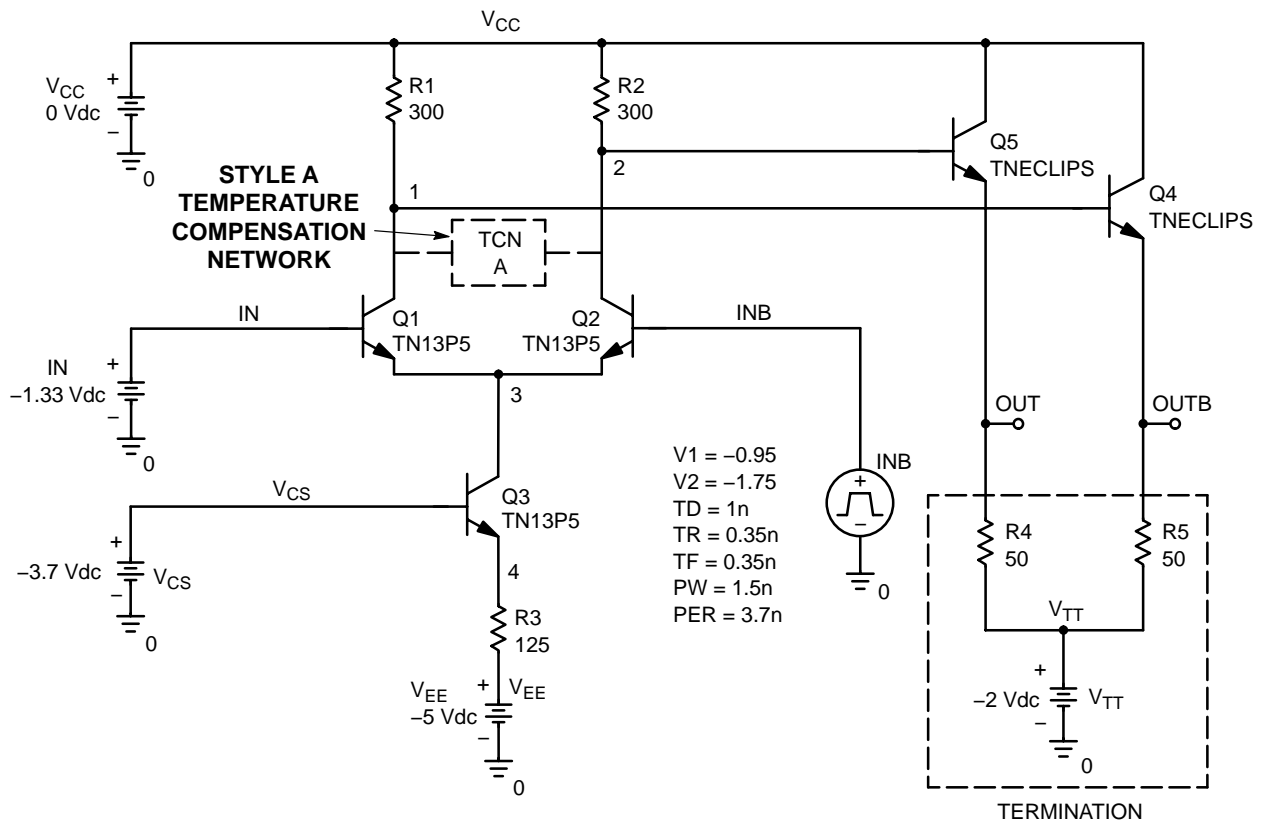


Figure 3. Output Buffer (OBUF\_A)

```
.SUBCKT OBUF_A
Q_Q1      1 IN 3 TN13P5
Q_Q2      2 INB 3 TN13P5
Q_Q3      3 VCS 4 TN13P5
Q_Q4      VCC 1 OUTB TNECLIPS
Q_Q5      VCC 2 OUT TNECLIPS
R_R1      1 VCC 300
R_R2      2 VCC 300
R_R3      VEE 4 125
R_R4      VTT OUT 50
R_R5      VTT OUTB 50
V_IN      IN 0 -1.33Vdc
V_INB     INB 0
V_VCC     VCC 0 0Vdc
V_VEE     VEE 0 -5Vdc
V_VTT     VTT 0 -2Vdc
V_VCS     VCS 0 -3.7Vdc
+PULSE -0.95 -1.75 1n 0.35n 0.35n 1.5n 3.7n
.END OBUF_A
```

# AN1503/D

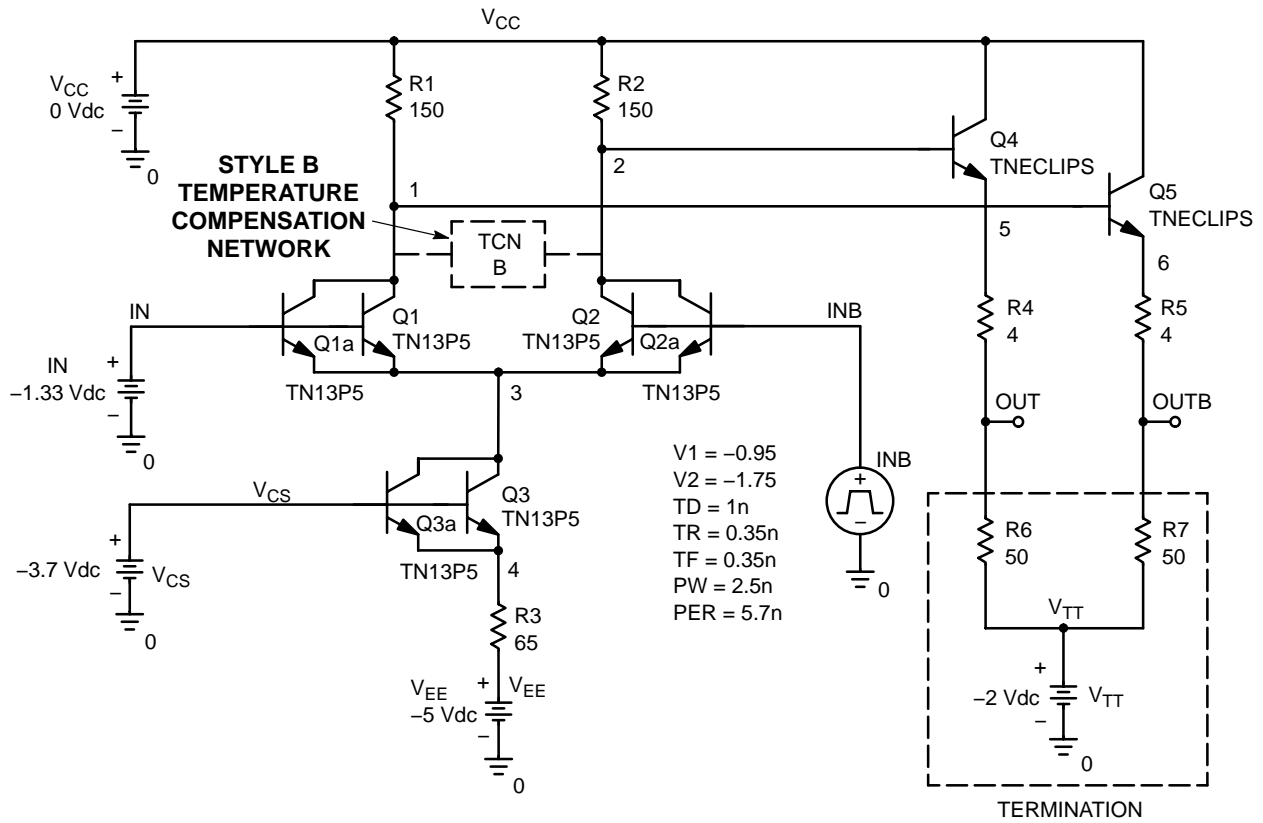


Figure 4. Output Buffer (OBUF\_B)

```
.SUBCKT OBUF_B
Q_Q1      1 IN 3 TN13P5
Q_Q1a     1 IN 3 TN13P5
Q_Q2      2 INB 3 TN13P5
Q_Q2a     2 INB 3 TN13P5
Q_Q3      3 VCS 4 TN13P5
Q_Q3a     3 VCS 4 TN13P5
Q_Q4      VCC 2 5 TNECLIPS
Q_Q5      VCC 1 6 TNECLIPS
R_R1      1 VCC 150
R_R2      2 VCC 150
R_R3      VEE 4 65
R_R4      OUT 5 4
R_R5      OUTB 6 4
R_R6      VTT OUT 50
R_R7      VTT OUTB 50
V_IN      IN 0 -1.33Vdc
V_INB     INB 0
V_VCC     VCC 0 0Vdc
V_VEE     VEE 0 -5Vdc
V_VCS     VCS 0 -3.7Vdc
V_VTT     VTT 0 -2Vdc
+PULSE -0.95 -1.75 1n 0.35n 0.35n 2.5n 5.7n
.END OBUF_B
```

# AN1503/D

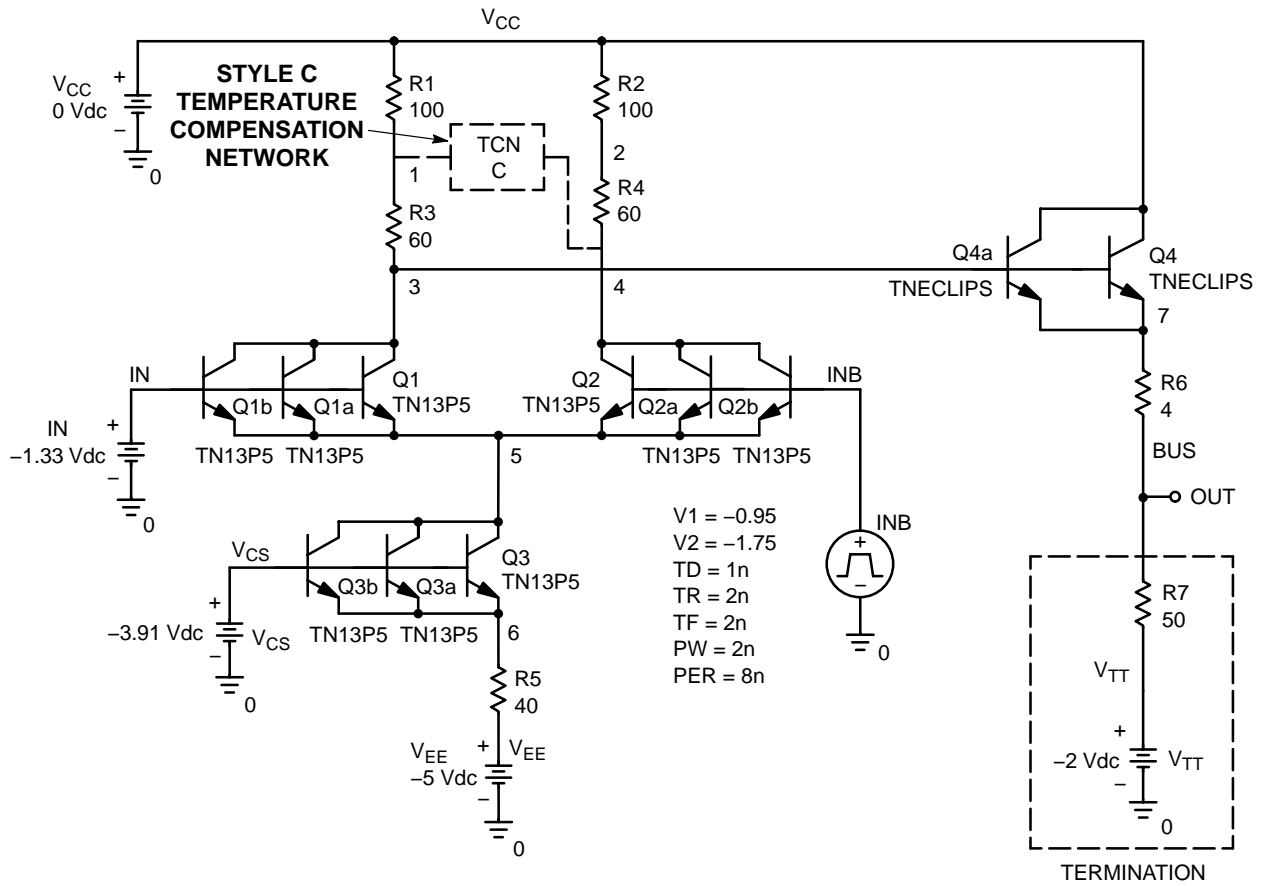


Figure 5. Output Buffer (OBUF\_C)

```
.SUBCKT OBUF_C
Q_Q1      3 IN 5 TN13P5
Q_Q1a     3 IN 5 TN13P5
Q_Q1b     3 IN 5 TN13P5
Q_Q2      4 INB 5 TN13P5
Q_Q2a     4 INB 5 TN13P5
Q_Q2b     4 INB 5 TN13P5
Q_Q3      5 VCS 6 TN13P5
Q_Q3a     5 VCS 6 TN13P5
Q_Q3b     5 VCS 6 TN13P5
Q_Q4      VCC 3 7 TNECLIPS
Q_Q4a     VCC 3 7 TNECLIPS
R_R1      1 VCC 100
R_R2      2 VCC 100
R_R3      3 1 60
R_R4      4 2 60
R_R5      VEE 6 40
R_R6      BUS 7 4
R_R7      VTT BUS 50
V_IN      IN 0 -1.33Vdc
V_INB     INB 0
V_VCC     VCC 0 0Vdc
V_VEE     VEE 0 -5Vdc
V_VCS     VCS 0 -3.91Vdc
V_VTT     VTT 0 -2Vdc
+PULSE -0.95 -1.75 1n 2n 2n 2n 8n
.END OBUF_C
```



# AN1503/D

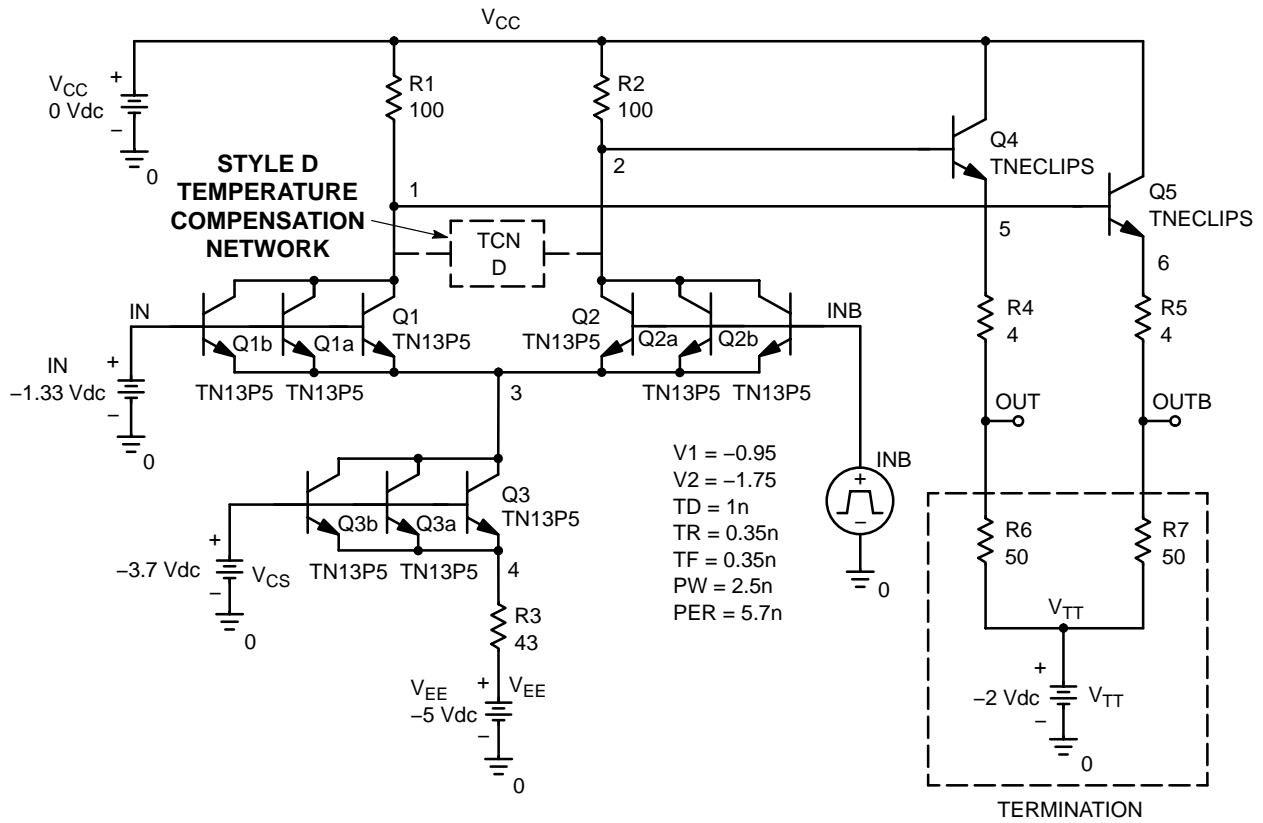


Figure 6. Output Buffer (OBUF\_D)

**.SUBCKT OBUF\_D**

```

Q_Q1      1  IN  3  TN13P5
Q_Q1a     1  IN  3  TN13P5
Q_Q1b     1  IN  3  TN13P5
Q_Q2      2  INB 3  TN13P5
Q_Q2a     2  INB 3  TN13P5
Q_Q2b     2  INB 3  TN13P5
Q_Q3      3  N19458 4  TN13P5
Q_Q3a     3  N19458 4  TN13P5
Q_Q3b     3  N19458 4  TN13P5
Q_Q4      VCC 2  5  TNECLIPS
Q_Q5      VCC 1  6  TNECLIPS
R_R1      1  VCC 100
R_R2      2  VCC 100
R_R3      VEE 4  43
R_R4      OUT 5  4
R_R5      OUTB 6  4
R_R6      VTT OUT 50
R_R7      VTT OUTB 50
V_INB     INB 0
V_IN      IN 0  -1.33Vdc
V_VCC     VCC 0  0Vdc
V_VEE     VEE 0  -5Vdc
V_VCS     N19458 0  -3.7Vdc
V_VTT     VTT 0  -2Vdc
+PULSE    -0.95 -1.75 1n 0.35n 0.35n 2.5n 5.7n
.END OBUF_D

```

# AN1503/D

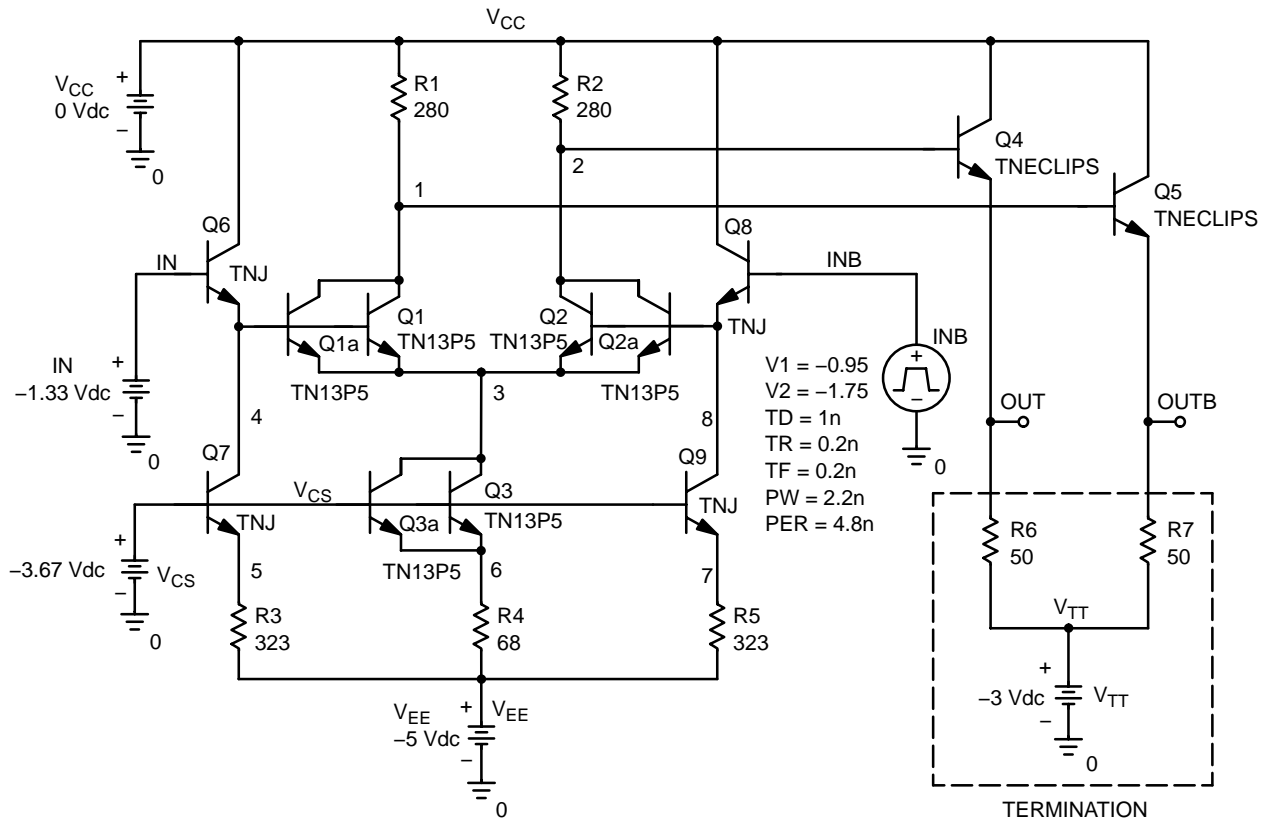


Figure 7. Output Buffer (OBUF\_E)

**.SUBCKT OBUF\_E**

```

Q_Q1      1 4 3 TN13P5
Q_Q1a     1 4 3 TN13P5
Q_Q2      2 8 3 TN13P5
Q_Q2a     2 8 3 TN13P5
Q_Q3      3 VCS 6 TN13P5
Q_Q3a     3 VCS 6 TN13P5
Q_Q4      VCC 2 OUT TNECLIPS
Q_Q5      VCC 1 OUTB TNECLIPS
Q_Q6      VCC IN 4 TN8
Q_Q7      4 VCS 5 TN8
Q_Q8      VCC INB 8 TN8
Q_Q9      8 VCS 7 TN8
R_R1      1 VCC 280
R_R2      2 VCC 280
R_R3      VEE 5 323
R_R4      VEE 6 68
R_R5      VEE 7 323
R_R6      VTT OUT 50
R_R7      VTT OUTB 50
V_IN      IN 0 -1.33Vdc
V_INB     INB 0
V_VCC     VCC 0 0Vdc
V_VEE     VEE 0 -5Vdc
V_VTT     VTT 0 -3Vdc
V_VCS     VCS 0 -3.67Vdc
+PULSE   -0.95 -1.75 1n 0.2n 0.2n 2.2n 4.8n
.END OBUF_E

```

# AN1503/D

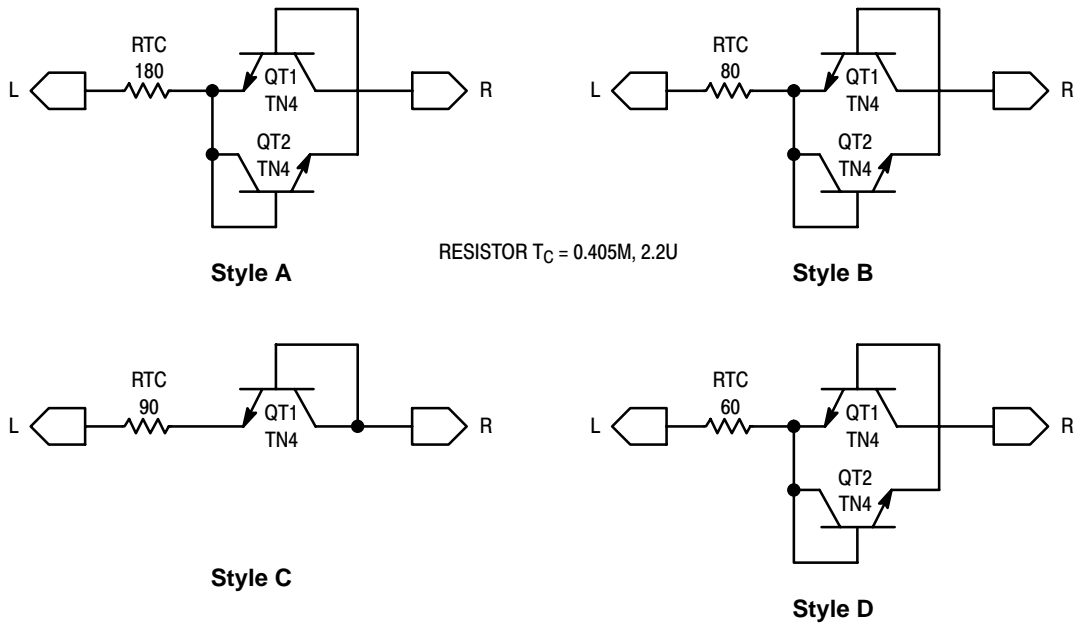


Figure 8. Temperature Compensation Networks

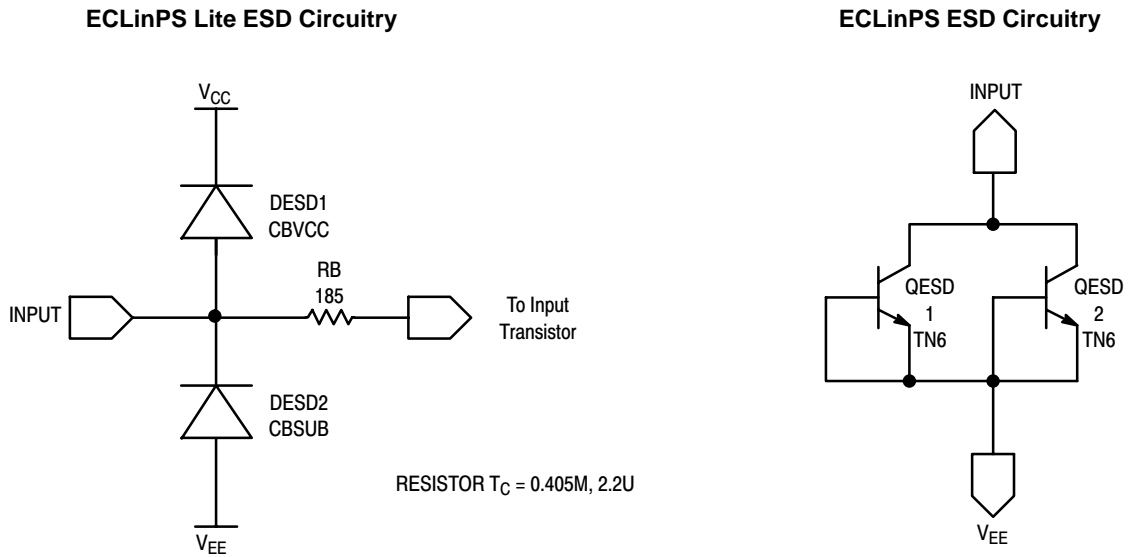


Figure 9. ESD Protection Circuitry

# AN1503/D

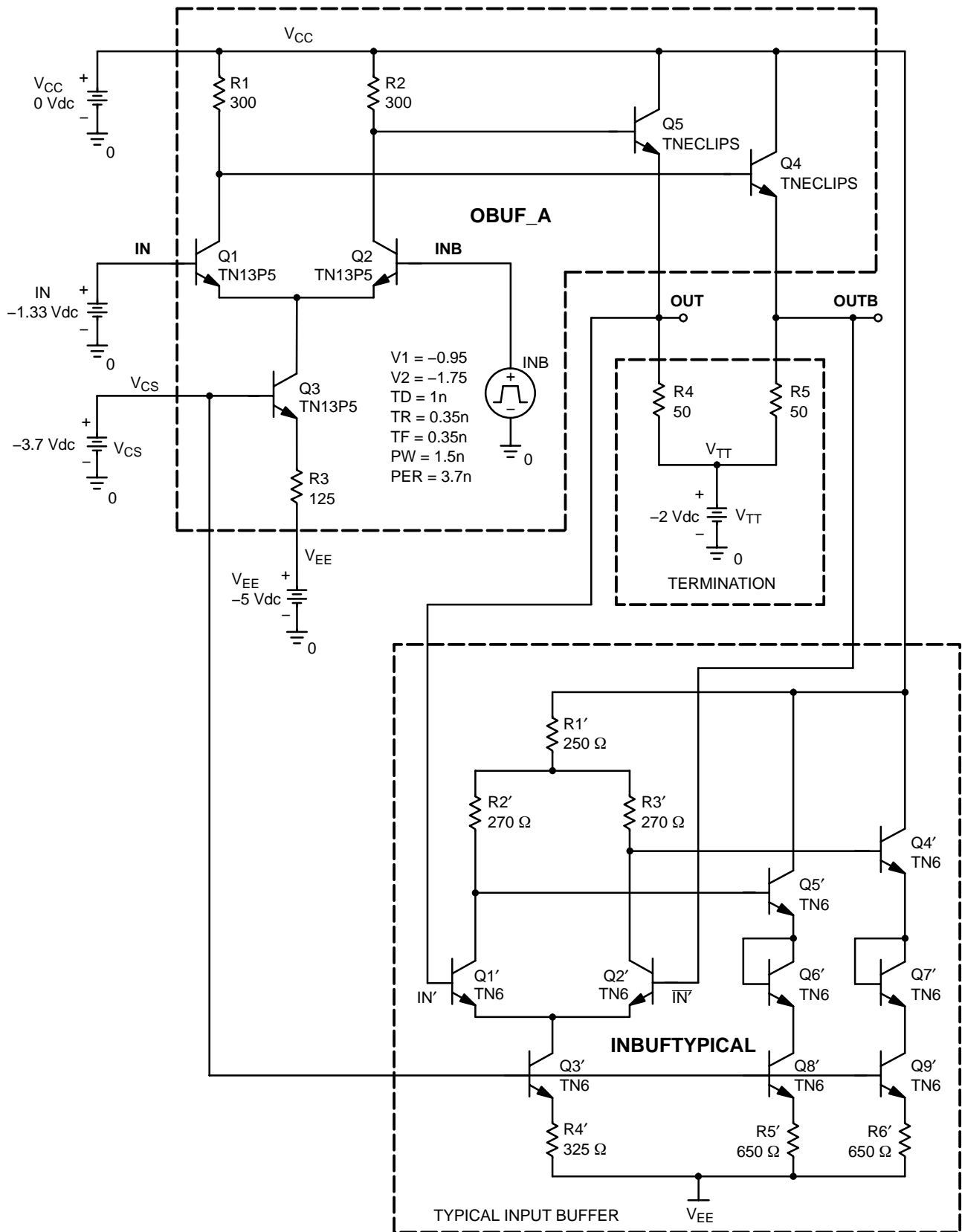


Figure 10. Typical Interconnect Schematic

# AN1503/D

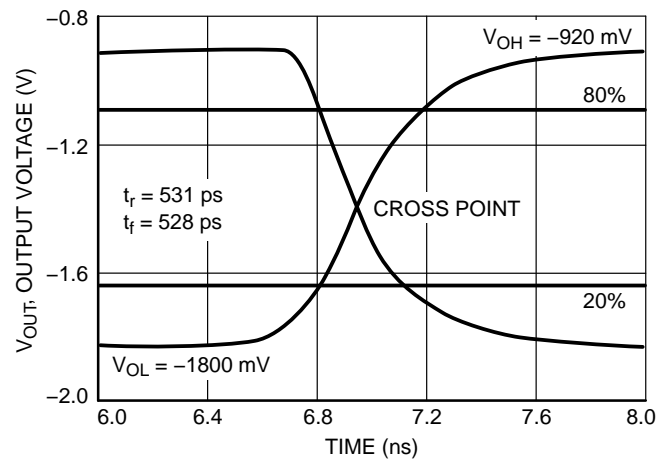


Figure 11. Typical Output Waveform

# AN1503/D

\*\*\*\*\* Transistor and Diodes Nominal SPICE Models \*\*\*\*\*

```
*****
.MODEL TN4 NPN (IS=5.27E-18 BF=120 NF=1 VAF=30 IKF=6.48mA
+ ISE=2.75E-16 BR=10 NE=2 VAR=5 IKR=567uA
+ IRB=8.1uA RB=461.6 RBM=142.5 RE=21.6 RC=83.1
+ CJE=19.9fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=25.1fF VJC=0.67 MJC=0.32 XCJC=0.3
+ CJS=49.6fF VJS=0.6 MJS=0.4 FC=0.9
+ TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=17.0mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
*****
.MODEL TN6 NPN (IS=8.56E-18 BF=120 NF=1 VAF=30 IKF=10.5mA
+ ISE=4.48E-16 BR=10 NE=2 VAR=5 IKR=922uA
+ IRB=13.2uA RB=291.4 RBM=95.0 RE=13.3 RC=62.7
+ CJE=29.9fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=31.2fF VJC=0.67 MJC=0.32 XCJC=0.3
+ CJS=60.9fF VJS=0.6 MJS=0.4 FC=0.9
+ TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=27.6mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
*****
.MODEL TN13P5 NPN (IS=2.09E-17 BF=120 NF=1 VAF=30 IKF=25.7mA
+ ISE=1.09E-15 BR=10 NE=2 VAR=5 IKR=2.25mA
+ IRB=32.2uA RB=122.6 RBM=42.2 RE=5.44 RC=32.8
+ CJE=67.4fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=53.8fF VJC=0.67 MJC=0.32 XCJC=0.3
+ CJS=103fF VJS=0.6 MJS=0.4 FC=0.9
+ TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=67.5mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
*****
.MODEL TN8 NPN (IS=1.18E-17 BF=120 NF=1 VAF=30 IKF=14.6mA
+ ISE=6.20E-16 BR=10 NE=2 VAR=5 IKR=1.28mA
+ IRB=18.2uA RB=213.1 RBM=71.2 RE=9.60 RC=50.4
+ CJE=39.9fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=37.2fF VJC=0.67 MJC=0.32 XCJC=0.3
+ CJS=72.2fF VJS=0.6 MJS=0.4 FC=0.9
+ TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=38.3mA
+ ISC=0 EG=1.11 XTI=5.2 PTF=0 KF=0 AF=1 NR=1 NC=2)
*****
.MODEL TNECLIPS NPN (IS=2.27E-16 BF=120 NF=1 VAF=30 IKF=279mA
+ ISE=1.19E-14 BR=10 NE=2 VAR=5 IKR=24.4mA
+ IRB=349uA RB=15.98 RBM=4.17 RE=0.501 RC=11.1
+ CJE=611fF VJE=0.9 MJE=0.4 XTB=0.73
+ CJC=440fF VJC=0.67 MJC=0.32 XCJC=0.3
+ CJS=668fF VJS=0.6 MJS=0.4 FC=0.9
+ TF=8pS TR=1nS XTF=10 VTF=1.4V ITF=733mA
+ ISC=0 EG=1.11 XTI=4.0 PTF=0 KF=0 AF=1 NR=1 NC=2)
*****
.MODEL CBVCC (IS=1.00E-15 CJO=527fF Vj=0.545 M=0.32 BV=14.5 IBV=0.1E-6 XTI=5 TT=1nS)
*****
.MODEL CBSUB (IS=1.00E-15 CJO=453fF TT=1nS)
*****
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**Package: SO-8**

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* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor      Pin
*     1             1
*     2             2
*     3             3
*     4             4
*     5             5
*     6             6
*     7             7
*     8             8
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:      0.076 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
* Connect chip side to N**I and board side to N**O
*
.SUBCKT LINES N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O
L01WB  N01I  N01M  1.367e-09
L01     N01M  N01O  7.794e-10
C01     N01M  0     2.445e-13
L02WB  N02I  N02M  1.287e-09
L02     N02M  N02O  5.473e-10
C02     N02M  0     1.888e-13
L03WB  N03I  N03M  1.287e-09
L03     N03M  N03O  5.473e-10
C03     N03M  0     1.901e-13
L04WB  N04I  N04M  1.367e-09
L04     N04M  N04O  7.723e-10
C04     N04M  0     2.443e-13
L05WB  N05I  N05M  1.367e-09
L05     N05M  N05O  7.710e-10
C05     N05M  0     2.478e-13
L06WB  N06I  N06M  1.287e-09
L06     N06M  N06O  5.489e-10
C06     N06M  0     1.916e-13
L07WB  N07I  N07M  1.287e-09
L07     N07M  N07O  5.495e-10
C07     N07M  0     1.930e-13
L08WB  N08I  N08M  1.367e-09
L08     N08M  N08O  7.786e-10
C08     N08M  0     2.451e-13
K0102  L01   L02   0.1687
K0102WB L01WB L02WB 0.3400
C0102  N01O  N02O  3.674e-14
K0103  L01   L03   0.0702
K0103WB L01WB L03WB 0.1847
K0203  L02   L03   0.1822
K0203WB L02WB L03WB 0.3505
C0203  N02O  N03O  3.521e-14
K0204  L02   L04   0.0682
K0204WB L02WB L04WB 0.1847
K0304  L03   L04   0.1694
K0304WB L03WB L04WB 0.3400

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## AN1503/D

C0304	N030	N040	3.675e-14
K0305WB	L03WB	L05WB	0.1847
K0405WB	L04WB	L05WB	0.3455
K0406WB	L04WB	L06WB	0.1847
K0506	L05	L06	0.1697
K0506WB	L05WB	L06WB	0.3400
C0506	N050	N060	3.720e-14
K0507	L05	L07	0.0682
K0507WB	L05WB	L07WB	0.1847
K0607	L06	L07	0.1824
K0607WB	L06WB	L07WB	0.3505
C0607	N060	N070	3.570e-14
K0608	L06	L08	0.0702
K0608WB	L06WB	L08WB	0.1847
K0708	L07	L08	0.1691
K0708WB	L07WB	L08WB	0.3400
C0708	N070	N080	3.632e-14

.ENDS LINES

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**Package: TSSOP-8**

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* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
* counter-clockwise
*   Conductor   Pin
*     1         1
*     2         2
*     3         3
*     4         4
*     5         5
*     6         6
*     7         7
*     8         8
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:      0.048 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
R_SHORT 0 GND 0.0001
*
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O GND PACKAGE
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O GND
R01WB  N01I  N01W  4.727e-02
L01WB  N01W  N01R  1.158e-09
R01    N01R  N01C  9.680e-04
C01    N01C  GND   8.978e-14
L01    N01C  N01O  7.466e-10
R02WB  N02I  N02W  3.815e-02
L02WB  N02W  N02R  9.835e-10
R02    N02R  N02C  9.680e-04
C02    N02C  GND   7.711e-14
L02    N02C  N02O  7.466e-10
R03WB  N03I  N03W  3.815e-02
L03WB  N03W  N03R  9.835e-10
R03    N03R  N03C  9.680e-04
C03    N03C  GND   7.704e-14
L03    N03C  N03O  7.465e-10
R04WB  N04I  N04W  4.727e-02
L04WB  N04W  N04R  1.158e-09
R04    N04R  N04C  9.680e-04
C04    N04C  GND   8.983e-14
L04    N04C  N04O  7.460e-10
R05WB  N05I  N05W  4.727e-02
L05WB  N05W  N05R  1.158e-09
R05    N05R  N05C  9.680e-04
C05    N05C  GND   8.983e-14
L05    N05C  N05O  7.460e-10
R06WB  N06I  N06W  3.815e-02
L06WB  N06W  N06R  9.835e-10
R06    N06R  N06C  9.680e-04
C06    N06C  GND   7.704e-14
L06    N06C  N06O  7.465e-10
R07WB  N07I  N07W  3.815e-02

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# AN1503/D

L07WB	N07W	N07R	9.835e-10
R07	N07R	N07C	9.680e-04
C07	N07C	GND	7.711e-14
L07	N07C	N07O	7.466e-10
R08WB	N08I	N08W	4.727e-02
L08WB	N08W	N08R	1.158e-09
R08	N08R	N08C	9.680e-04
C08	N08C	GND	8.978e-14
L08	N08C	N08O	7.466e-10
K0102	L01	L02	0.2481
K0102WB	L01WB	L02WB	0.1729
C0102	N01C	N02C	2.283e-14
K0103	L01	L03	0.1067
K0103WB	L01WB	L03WB	0.0598
K0104	L01	L04	0.0593
K0203	L02	L03	0.2479
K0203WB	L02WB	L03WB	0.1463
C0203	N02C	N03C	2.136e-14
K0204	L02	L04	0.1068
K0204WB	L02WB	L04WB	0.0598
K0304	L03	L04	0.2481
K0304WB	L03WB	L04WB	0.1729
C0304	N03C	N04C	2.279e-14
K0506	L05	L06	0.2481
K0506WB	L05WB	L06WB	0.1513
C0506	N05C	N06C	2.279e-14
K0507	L05	L07	0.1068
K0507WB	L05WB	L07WB	0.0615
K0508	L05	L08	0.0593
K0607	L06	L07	0.2479
K0607WB	L06WB	L07WB	0.1729
C0607	N06C	N07C	2.136e-14
K0608	L06	L08	0.1067
K0608WB	L06WB	L08WB	0.0615
K0708	L07	L08	0.2481
K0708WB	L07WB	L08WB	0.1513
C0708	N07C	N08C	2.283e-14

.ENDS PACKAGE

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**Package: SO-20**

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* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Conductor number-pin designation cross reference:
*   Conductor      Pin
*     1             1
*     2             2
*     3             3
*     4             4
*     5             5
*     6             6
*     7             7
*     8             8
*     9             9
*    10            10
*    11            11
*    12            12
*    13            13
*    14            14
*    15            15
*    16            16
*    17            17
*    18            18
*    19            19
*    20            20
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:      0.275 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
.SUBCKT PACKAGE N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O
+ N10I N10O N11I N11O N12I N12O N13I N13O N14I N14O
+ N15I N15O N16I N16O N17I N17O N18I N18O N19I N19O
+ N20I N20O BD_GND
R01WB  N01I  N01W  3.732e-02
L01WB  N01W  N01R  9.678e-10
R01    N01R  N01C  1.700e-02
C01    N01C  BD_GND 4.680e-13
L01    N01C  N01O  3.814e-09
R02WB  N02I  N02W  8.086e-02
L02WB  N02W  N02R  1.822e-09
R02    N02R  N02C  1.300e-02
C02    N02C  BD_GND 1.924e-13
L02    N02C  N02O  2.724e-09
R03WB  N03I  N03W  9.122e-02
L03WB  N03W  N03R  2.033e-09
R03    N03R  N03C  9.000e-02
C03    N03C  BD_GND 1.377e-13
L03    N03C  N03O  1.814e-09
R04WB  N04I  N04W  7.878e-02
L04WB  N04W  N04R  1.780e-09
R04    N04R  N04C  8.000e-02
C04    N04C  BD_GND 1.484e-13
L04    N04C  N04O  1.551e-09
R05WB  N05I  N05W  6.634e-02
L05WB  N05W  N05R  1.531e-09
R05    N05R  N05C  7.000e-02

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## AN1503/D

C05	N05C	BD_GND	1.635e-13
L05	N05C	N05O	1.508e-09
R06WB	N06I	N06W	6.634e-02
L06WB	N06W	N06R	1.531e-09
R06	N06R	N06C	7.000e-02
C06	N06C	BD_GND	1.584e-13
L06	N06C	N06O	1.508e-09
R07WB	N07I	N07W	7.878e-02
L07WB	N07W	N07R	1.780e-09
R07	N07R	N07C	8.000e-02
C07	N07C	BD_GND	1.476e-13
L07	N07C	N07O	1.553e-09
R08WB	N08I	N08W	4.976e-02
L08WB	N08W	N08R	1.206e-09
R08	N08R	N08C	9.000e-02
C08	N08C	BD_GND	1.322e-13
L08	N08C	N08O	1.820e-09
R09WB	N09I	N09W	8.086e-02
L09WB	N09W	N09R	1.822e-09
R09	N09R	N09C	1.300e-02
C09	N09C	BD_GND	1.864e-13
L09	N09C	N09O	2.725e-09
R10WB	N10I	N10W	7.256e-02
L10WB	N10W	N10R	1.655e-09
R10	N10R	N10C	1.700e-02
C10	N10C	BD_GND	4.681e-13
L10	N10C	N10O	3.814e-09
R11WB	N11I	N11W	3.732e-02
L11WB	N11W	N11R	9.678e-10
R11	N11R	N11C	1.700e-02
C11	N11C	BD_GND	4.761e-13
L11	N11C	N11O	3.795e-09
R12WB	N12I	N12W	8.086e-02
L12WB	N12W	N12R	1.822e-09
R12	N12R	N12C	1.300e-02
C12	N12C	BD_GND	1.888e-13
L12	N12C	N12O	2.745e-09
R13WB	N13I	N13W	9.122e-02
L13WB	N13W	N13R	2.033e-09
R13	N13R	N13C	9.000e-02
C13	N13C	BD_GND	1.346e-13
L13	N13C	N13O	1.879e-09
R14WB	N14I	N14W	7.878e-02
L14WB	N14W	N14R	1.780e-09
R14	N14R	N14C	8.000e-02
C14	N14C	BD_GND	1.496e-13
L14	N14C	N14O	1.436e-09
R15WB	N15I	N15W	6.634e-02
L15WB	N15W	N15R	1.531e-09
R15	N15R	N15C	7.000e-02
C15	N15C	BD_GND	1.550e-13
L15	N15C	N15O	1.464e-09
R16WB	N16I	N16W	6.634e-02
L16WB	N16W	N16R	1.531e-09
R16	N16R	N16C	7.000e-02
C16	N16C	BD_GND	1.568e-13
L16	N16C	N16O	1.465e-09
R17WB	N17I	N17W	7.878e-02
L17WB	N17W	N17R	1.780e-09
R17	N17R	N17C	8.000e-02
C17	N17C	BD_GND	1.492e-13
L17	N17C	N17O	1.437e-09

# AN1503/D

R18WB	N18I	N18W	9.122e-02
L18WB	N18W	N18R	2.033e-09
R18	N18R	N18C	9.000e-02
C18	N18C	BD_GND	1.346e-13
L18	N18C	N18O	1.892e-09
R19WB	N19I	N19W	8.086e-02
L19WB	N19W	N19R	1.822e-09
R19	N19R	N19C	1.300e-02
C19	N19C	BD_GND	1.880e-13
L19	N19C	N19O	2.767e-09
R20WB	N20I	N20W	7.256e-02
L20WB	N20W	N20R	1.655e-09
R20	N20R	N20C	1.700e-02
C20	N20C	BD_GND	4.712e-13
L20	N20C	N20O	3.825e-09
K0102	L01	L02	0.4539
K0102WB	L01WB	L02WB	0.1239
C0102	N01C	N02C	2.674e-13
K0103	L01	L03	0.2557
K0104	L01	L04	0.1742
K0105	L01	L05	0.1290
K0106	L01	L06	0.1011
K0107	L01	L07	0.0834
K0108	L01	L08	0.0636
K0111	L01	L11	-0.0789
K0112	L01	L12	-0.0755
K0113	L01	L13	-0.0716
K0114	L01	L14	-0.0594
K0115	L01	L15	-0.0669
K0116	L01	L16	-0.0657
K0117	L01	L17	-0.0672
K0118	L01	L18	-0.0625
K0203	L02	L03	0.3964
K0203WB	L02WB	L03WB	0.1239
C0203	N02C	N03C	1.529e-13
K0204	L02	L04	0.2341
K0205	L02	L05	0.1587
K0206	L02	L06	0.1206
K0207	L02	L07	0.0974
K0208	L02	L08	0.0760
K0209	L02	L09	0.0554
K0211	L02	L11	-0.0743
K0212	L02	L12	-0.0723
K0213	L02	L13	-0.0707
K0214	L02	L14	-0.0604
K0215	L02	L15	-0.0678
K0216	L02	L16	-0.0677
K0217	L02	L17	-0.0685
K0218	L02	L18	-0.0682
K0304	L03	L04	0.3767
K0304WB	L03WB	L04WB	0.1239
C0304	N03C	N04C	1.006e-13
K0305	L03	L05	0.2211
K0306	L03	L06	0.1564
K0307	L03	L07	0.1219
K0308	L03	L08	0.0956
K0309	L03	L09	0.0762
K0310	L03	L10	0.0639
K0311	L03	L11	-0.0654
K0312	L03	L12	-0.0662
K0313	L03	L13	-0.0688
K0314	L03	L14	-0.0614

## AN1503/D

K0315	L03	L15	-0.0683
K0316	L03	L16	-0.0692
K0317	L03	L17	-0.0684
K0318	L03	L18	-0.0730
K0319	L03	L19	-0.0609
K0320	L03	L20	-0.0501
K0405	L04	L05	0.3731
K0405WB	L04WB	L05WB	0.1239
C0405	N04C	N05C	8.137e-14
K0406	L04	L06	0.2290
K0407	L04	L07	0.1637
K0408	L04	L08	0.1218
K0409	L04	L09	0.0976
K0410	L04	L10	0.0836
K0411	L04	L11	-0.0645
K0412	L04	L12	-0.0673
K0413	L04	L13	-0.0722
K0414	L04	L14	-0.0658
K0415	L04	L15	-0.0724
K0416	L04	L16	-0.0733
K0417	L04	L17	-0.0708
K0418	L04	L18	-0.0763
K0419	L04	L19	-0.0673
K0420	L04	L20	-0.0597
K0506	L05	L06	0.3775
K0506WB	L05WB	L06WB	0.1239
C0506	N05C	N06C	8.844e-14
K0507	L05	L07	0.2293
K0508	L05	L08	0.1565
K0509	L05	L09	0.1208
K0510	L05	L10	0.1013
K0511	L05	L11	-0.0636
K0512	L05	L12	-0.0679
K0513	L05	L13	-0.0742
K0514	L05	L14	-0.0683
K0515	L05	L15	-0.0737
K0516	L05	L16	-0.0741
K0517	L05	L17	-0.0704
K0518	L05	L18	-0.0760
K0519	L05	L19	-0.0684
K0520	L05	L20	-0.0622
K0607	L06	L07	0.3743
K0607WB	L06WB	L07WB	0.1239
C0607	N06C	N07C	7.898e-14
K0608	L06	L08	0.2214
K0609	L06	L09	0.1591
K0610	L06	L10	0.1293
K0611	L06	L11	-0.0607
K0612	L06	L12	-0.0668
K0613	L06	L13	-0.0752
K0614	L06	L14	-0.0700
K0615	L06	L15	-0.0741
K0616	L06	L16	-0.0742
K0617	L06	L17	-0.0690
K0618	L06	L18	-0.0754
K0619	L06	L19	-0.0697
K0620	L06	L20	-0.0652
K0708	L07	L08	0.3762
K0708WB	L07WB	L08WB	0.1239
C0708	N07C	N08C	1.016e-13
K0709	L07	L09	0.2343
K0710	L07	L10	0.1746

# AN1503/D

K0711	L07	L11	-0.0581
K0712	L07	L12	-0.0657
K0713	L07	L13	-0.0756
K0714	L07	L14	-0.0707
K0715	L07	L15	-0.0736
K0716	L07	L16	-0.0730
K0717	L07	L17	-0.0667
K0718	L07	L18	-0.0735
K0719	L07	L19	-0.0692
K0720	L07	L20	-0.0661
K0809	L08	L09	0.3970
K0809WB	L08WB	L09WB	0.1239
C0809	N08C	N09C	1.545e-13
K0810	L08	L10	0.2564
K0812	L08	L12	-0.0591
K0813	L08	L13	-0.0723
K0814	L08	L14	-0.0685
K0815	L08	L15	-0.0698
K0816	L08	L16	-0.0693
K0817	L08	L17	-0.0624
K0818	L08	L18	-0.0702
K0819	L08	L19	-0.0681
K0820	L08	L20	-0.0670
K0910	L09	L10	0.4542
K0910WB	L09WB	L10WB	0.1239
C0910	N09C	N10C	2.677e-13
K0913	L09	L13	-0.0675
K0914	L09	L14	-0.0688
K0915	L09	L15	-0.0687
K0916	L09	L16	-0.0693
K0917	L09	L17	-0.0618
K0918	L09	L18	-0.0723
K0919	L09	L19	-0.0742
K0920	L09	L20	-0.0759
K1011WB	L10WB	L11WB	0.1239
K1013	L10	L13	-0.0616
K1014	L10	L14	-0.0675
K1015	L10	L15	-0.0668
K1016	L10	L16	-0.0685
K1017	L10	L17	-0.0609
K1018	L10	L18	-0.0731
K1019	L10	L19	-0.0773
K1020	L10	L20	-0.0803
K1112	L11	L12	0.4562
K1112WB	L11WB	L12WB	0.1239
C1112	N11C	N12C	2.679e-13
K1113	L11	L13	0.2725
K1114	L11	L14	0.1533
K1115	L11	L15	0.1161
K1116	L11	L16	0.0901
K1117	L11	L17	0.0702
K1118	L11	L18	0.0567
K1213	L12	L13	0.4103
K1213WB	L12WB	L13WB	0.1239
C1213	N12C	N13C	1.538e-13
K1214	L12	L14	0.2091
K1215	L12	L15	0.1398
K1216	L12	L16	0.1055
K1217	L12	L17	0.0812
K1218	L12	L18	0.0684
K1314	L13	L14	0.3577
K1314WB	L13WB	L14WB	0.1239

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C1314	N13C	N14C	1.026e-13
K1315	L13	L15	0.2088
K1316	L13	L16	0.1474
K1317	L13	L17	0.1074
K1318	L13	L18	0.0930
K1319	L13	L19	0.0693
K1320	L13	L20	0.0578
K1415	L14	L15	0.3383
K1415WB	L14WB	L15WB	0.1239
C1415	N14C	N15C	7.843e-14
K1416	L14	L16	0.1987
K1417	L14	L17	0.1302
K1418	L14	L18	0.1078
K1419	L14	L19	0.0825
K1420	L14	L20	0.0715
K1516	L15	L16	0.3631
K1516WB	L15WB	L16WB	0.1239
C1516	N15C	N16C	9.179e-14
K1517	L15	L17	0.1988
K1518	L15	L18	0.1480
K1519	L15	L19	0.1072
K1520	L15	L20	0.0918
K1617	L16	L17	0.3380
K1617WB	L16WB	L17WB	0.1239
C1617	N16C	N17C	7.810e-14
K1618	L16	L18	0.2096
K1619	L16	L19	0.1419
K1620	L16	L20	0.1183
K1718	L17	L18	0.3595
K1718WB	L17WB	L18WB	0.1239
C1718	N17C	N18C	1.034e-13
K1719	L17	L19	0.2122
K1720	L17	L20	0.1565
K1819	L18	L19	0.4140
K1819WB	L18WB	L19WB	0.1239
C1819	N18C	N19C	1.536e-13
K1820	L18	L20	0.2766
K1920	L19	L20	0.4603
K1920WB	L19WB	L20WB	0.1239
C1920	N19C	N20C	2.679e-13

.ENDS PACKAGE

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**Package: PLCC-28**

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* SPICE subcircuit file of coupled transmission lines
*
* Transmission line model
*
* Note:
* 1. The model assume ground plane is 15 mil below package
* 2. The model assume flag is floating
* 3. The flag is 170 x 170 mil square, pin 1 starts from up left corner
* 4. The lead sequence is counter clockwise
*
* Conductor number-pin designation cross reference:
*   Conductor      Pin
*       1           1
*       2           2
*       3           3
*       4           4
*       5           5
*       6           6
*       7           7
*       8           8
*       9           9
*      10          10
*      11          11
*      12          12
*      13          13
*      14          14
*      15          15
*      16          16
*      17          17
*      18          18
*      19          19
*      20          20
*      21          21
*      22          22
*      23          23
*      24          24
*      25          25
*      26          26
*      27          27
*      28          28
*
* number of lumps:      1
* FASTEST APPLICABLE EDGE RATE:      0.209 ns
* COMPRESSION OF SUBCIRCUITS PERFORMED: discard ratio is 0.050
*
* ECLinPS usage requires the input nodes used in the subcircuit call
* statement (X_777) that are tied to global ports(VCC, VCC0, and VEE internal
* to the die) to have the same global names in the subcircuit call statement(X_777).
* For example, if VCC is wirebonded to pin 20 for a certain design, then N20I
* should be relabeled to VCC. Again, the change needs only to be incorporated
* in the X_777 subcircuit callout statement. Since this requires a change to
* the netlist below, it is necessary for each design to have a copy of this file with
* the appropriate changes made that are required for that design.
*
* R_SHORT 0 ground 0.0001
*
X_777 N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O N09I N09O

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+ N10I N100 N11I N110 N12I N120 N13I N130 N14I N140  
+ N15I N150 N16I N160 N17I N170 N18I N180 N19I N190  
+ N20I N200 N21I N210 N22I N220 N23I N230 N24I N240  
+ N25I N250 N26I N260 N27I N270 N28I N280 ground PACKAGE

\*

.SUBCKT PACKAGE N01I N010 N02I N020 N03I N030 N04I N040

+ N05I N050 N06I N060 N07I N070 N08I N080 N09I N090  
+ N10I N100 N11I N110 N12I N120 N13I N130 N14I N140  
+ N15I N150 N16I N160 N17I N170 N18I N180 N19I N190  
+ N20I N200 N21I N210 N22I N220 N23I N230 N24I N240  
+ N25I N250 N26I N260 N27I N270 N28I N280 ground

R01WB N01I N01W 1.124e-01  
L01WB N01W N01R 2.474e-09  
R01 N01R N01C 1.120e-02  
C01 N01C ground 3.919e-13  
L01 N01C N010 2.346e-09  
R02WB N02I N02W 9.952e-02  
L02WB N02W N02R 2.204e-09  
R02 N02R N02C 1.120e-02  
C02 N02C ground 1.950e-13  
L02 N02C N020 2.180e-09  
R03WB N03I N03W 9.164e-02  
L03WB N03W N03R 2.042e-09  
R03 N03R N03C 1.100e-02  
C03 N03C ground 1.789e-13  
L03 N03C N030 2.050e-09  
R04WB N04I N04W 9.039e-02  
L04WB N04W N04R 2.016e-09  
R04 N04R N04C 1.100e-02  
C04 N04C ground 1.748e-13  
L04 N04C N040 2.030e-09  
R05WB N05I N05W 9.164e-02  
L05WB N05W N05R 2.042e-09  
R05 N05R N05C 1.100e-02  
C05 N05C ground 1.800e-13  
L05 N05C N050 2.049e-09  
R06WB N06I N06W 9.952e-02  
L06WB N06W N06R 2.204e-09  
R06 N06R N06C 1.120e-02  
C06 N06C ground 1.936e-13  
L06 N06C N060 2.184e-09  
R07WB N07I N07W 1.124e-01  
L07WB N07W N07R 2.474e-09  
R07 N07R N07C 1.120e-02  
C07 N07C ground 3.916e-13  
L07 N07C N070 2.341e-09  
R08WB N08I N08W 1.124e-01  
L08WB N08W N08R 2.474e-09  
R08 N08R N08C 1.120e-02  
C08 N08C ground 3.916e-13  
L08 N08C N080 2.341e-09  
R09WB N09I N09W 9.952e-02  
L09WB N09W N09R 2.204e-09  
R09 N09R N09C 1.120e-02  
C09 N09C ground 1.936e-13  
L09 N09C N090 2.184e-09  
R10WB N10I N10W 9.164e-02  
L10WB N10W N10R 2.042e-09  
R10 N10R N10C 1.100e-02  
C10 N10C ground 1.800e-13  
L10 N10C N100 2.049e-09  
R11WB N11I N11W 9.039e-02

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L11WB	N11W	N11R	2.016e-09
R11	N11R	N11C	1.100e-02
C11	N11C	ground	1.748e-13
L11	N11C	N11O	2.030e-09
R12WB	N12I	N12W	9.164e-02
L12WB	N12W	N12R	2.042e-09
R12	N12R	N12C	1.100e-02
C12	N12C	ground	1.789e-13
L12	N12C	N12O	2.050e-09
R13WB	N13I	N13W	9.952e-02
L13WB	N13W	N13R	2.204e-09
R13	N13R	N13C	1.120e-02
C13	N13C	ground	1.950e-13
L13	N13C	N13O	2.180e-09
R14WB	N14I	N14W	1.124e-01
L14WB	N14W	N14R	2.474e-09
R14	N14R	N14C	1.120e-02
C14	N14C	ground	3.919e-13
L14	N14C	N14O	2.346e-09
R15WB	N15I	N15W	1.124e-01
L15WB	N15W	N15R	2.474e-09
R15	N15R	N15C	1.120e-02
C15	N15C	ground	3.919e-13
L15	N15C	N15O	2.346e-09
R16WB	N16I	N16W	9.952e-02
L16WB	N16W	N16R	2.204e-09
R16	N16R	N16C	1.120e-02
C16	N16C	ground	1.950e-13
L16	N16C	N16O	2.180e-09
R17WB	N17I	N17W	9.164e-02
L17WB	N17W	N17R	2.042e-09
R17	N17R	N17C	1.100e-02
C17	N17C	ground	1.789e-13
L17	N17C	N17O	2.050e-09
R18WB	N18I	N18W	9.039e-02
L18WB	N18W	N18R	2.016e-09
R18	N18R	N18C	1.100e-02
C18	N18C	ground	1.748e-13
L18	N18C	N18O	2.030e-09
R19WB	N19I	N19W	9.164e-02
L19WB	N19W	N19R	2.042e-09
R19	N19R	N19C	1.100e-02
C19	N19C	ground	1.800e-13
L19	N19C	N19O	2.049e-09
R20WB	N20I	N20W	9.952e-02
L20WB	N20W	N20R	2.204e-09
R20	N20R	N20C	1.120e-02
C20	N20C	ground	1.936e-13
L20	N20C	N20O	2.184e-09
R21WB	N21I	N21W	1.124e-01
L21WB	N21W	N21R	2.474e-09
R21	N21R	N21C	1.120e-02
C21	N21C	ground	3.916e-13
L21	N21C	N21O	2.341e-09
R22WB	N22I	N22W	1.124e-01
L22WB	N22W	N22R	2.474e-09
R22	N22R	N22C	1.120e-02
C22	N22C	ground	3.916e-13
L22	N22C	N22O	2.341e-09
R23WB	N23I	N23W	9.952e-02
L23WB	N23W	N23R	2.204e-09
R23	N23R	N23C	1.120e-02

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C23	N23C	ground	1.936e-13
L23	N23C	N23O	2.184e-09
R24WB	N24I	N24W	9.164e-02
L24WB	N24W	N24R	2.042e-09
R24	N24R	N24C	1.100e-02
C24	N24C	ground	1.800e-13
L24	N24C	N24O	2.049e-09
R25WB	N25I	N25W	9.039e-02
L25WB	N25W	N25R	2.016e-09
R25	N25R	N25C	1.100e-02
C25	N25C	ground	1.748e-13
L25	N25C	N25O	2.030e-09
R26WB	N26I	N26W	9.164e-02
L26WB	N26W	N26R	2.042e-09
R26	N26R	N26C	1.100e-02
C26	N26C	ground	1.789e-13
L26	N26C	N26O	2.050e-09
R27WB	N27I	N27W	9.952e-02
L27WB	N27W	N27R	2.204e-09
R27	N27R	N27C	1.120e-02
C27	N27C	ground	1.950e-13
L27	N27C	N27O	2.180e-09
R28WB	N28I	N28W	1.124e-01
L28WB	N28W	N28R	2.474e-09
R28	N28R	N28C	1.120e-02
C28	N28C	ground	3.919e-13
L28	N28C	N28O	2.346e-09
K0102	L01	L02	0.4380
K0102WB	L01WB	L02WB	0.1463
C0102	N01C	N02C	2.394e-13
K0103	L01	L03	0.2472
K0103WB	L01WB	L03WB	0.0501
K0104	L01	L04	0.1557
K0105	L01	L05	0.1083
K0106	L01	L06	0.0742
K0107	L01	L07	0.0543
K0124	L01	L24	0.0506
K0125	L01	L25	0.0745
K0126	L01	L26	0.1092
K0127	L01	L27	0.1565
K0128	L01	L28	0.2194
C0128	N01C	N28C	5.401e-14
K0203	L02	L03	0.4331
K0203WB	L02WB	L03WB	0.1463
C0203	N02C	N03C	2.332e-13
K0204	L02	L04	0.2413
K0204WB	L02WB	L04WB	0.0708
K0205	L02	L05	0.1554
K0206	L02	L06	0.1051
K0207	L02	L07	0.0741
K0225	L02	L25	0.0619
K0226	L02	L26	0.0898
K0227	L02	L27	0.1237
K0228	L02	L28	0.1565
K0304	L03	L04	0.4342
K0304WB	L03WB	L04WB	0.2238
C0304	N03C	N04C	2.254e-13
K0305	L03	L05	0.2434
K0305WB	L03WB	L05WB	0.0853
K0306	L03	L06	0.1552
K0307	L03	L07	0.1083
K0308	L03	L08	0.0506

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K0327	L03	L27	0.0898
K0328	L03	L28	0.1092
K0405	L04	L05	0.4355
K0405WB	L04WB	L05WB	0.2238
C0405	N04C	N05C	2.282e-13
K0406	L04	L06	0.2418
K0406WB	L04WB	L06WB	0.0708
K0407	L04	L07	0.1558
K0408	L04	L08	0.0742
K0409	L04	L09	0.0613
K0427	L04	L27	0.0619
K0428	L04	L28	0.0745
K0506	L05	L06	0.4330
K0506WB	L05WB	L06WB	0.1463
C0506	N05C	N06C	2.324e-13
K0507	L05	L07	0.2474
K0507WB	L05WB	L07WB	0.0501
K0508	L05	L08	0.1087
K0509	L05	L09	0.0889
K0528	L05	L28	0.0506
K0607	L06	L07	0.4383
K0607WB	L06WB	L07WB	0.1463
C0607	N06C	N07C	2.402e-13
K0608	L06	L08	0.1558
K0609	L06	L09	0.1228
K0610	L06	L10	0.0889
K0611	L06	L11	0.0613
K0708	L07	L08	0.2174
K0708WB	L07WB	L08WB	0.0811
C0708	N07C	N08C	5.266e-14
K0709	L07	L09	0.1558
K0710	L07	L10	0.1087
K0711	L07	L11	0.0742
K0712	L07	L12	0.0506
K0809	L08	L09	0.4383
K0809WB	L08WB	L09WB	0.1463
C0809	N08C	N09C	2.402e-13
K0810	L08	L10	0.2474
K0810WB	L08WB	L10WB	0.0501
K0811	L08	L11	0.1558
K0812	L08	L12	0.1083
K0813	L08	L13	0.0741
K0814	L08	L14	0.0543
K0910	L09	L10	0.4330
K0910WB	L09WB	L10WB	0.1463
K0910	N09C	N10C	2.324e-13
K0911	L09	L11	0.2418
K0911WB	L09WB	L11WB	0.0708
K0912	L09	L12	0.1552
K0913	L09	L13	0.1051
K0914	L09	L14	0.0742
K1011	L10	L11	0.4355
K1011WB	L10WB	L11WB	0.2238
C1011	N10C	N11C	2.282e-13
K1012	L10	L12	0.2434
K1012WB	L10WB	L12WB	0.0853
K1013	L10	L13	0.1554
K1014	L10	L14	0.1083
K1015	L10	L15	0.0506
K1112	L11	L12	0.4342
K1112WB	L11WB	L12WB	0.2238
C1112	N11C	N12C	2.254e-13

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K1113	L11	L13	0.2413
K1113WB	L11WB	L13WB	0.0708
K1114	L11	L14	0.1557
K1115	L11	L15	0.0745
K1116	L11	L16	0.0619
K1213	L12	L13	0.4331
K1213WB	L12WB	L13WB	0.1463
C1213	N12C	N13C	2.332e-13
K1214	L12	L14	0.2472
K1214WB	L12WB	L14WB	0.0501
K1215	L12	L15	0.1092
K1216	L12	L16	0.0898
K1314	L13	L14	0.4380
K1314WB	L13WB	L14WB	0.1463
C1314	N13C	N14C	2.394e-13
K1315	L13	L15	0.1565
K1316	L13	L16	0.1237
K1317	L13	L17	0.0898
K1318	L13	L18	0.0619
K1415	L14	L15	0.2194
K1415WB	L14WB	L15WB	0.0811
C1415	N14C	N15C	5.401e-14
K1416	L14	L16	0.1565
K1417	L14	L17	0.1092
K1418	L14	L18	0.0745
K1419	L14	L19	0.0506
K1516	L15	L16	0.4380
K1516WB	L15WB	L16WB	0.1463
C1516	N15C	N16C	2.394e-13
K1517	L15	L17	0.2472
K1517WB	L15WB	L17WB	0.0501
K1518	L15	L18	0.1557
K1519	L15	L19	0.1083
K1520	L15	L20	0.0742
K1521	L15	L21	0.0543
K1617	L16	L17	0.4331
K1617WB	L16WB	L17WB	0.1463
C1617	N16C	N17C	2.332e-13
K1618	L16	L18	0.2413
K1618WB	L16WB	L18WB	0.0708
K1619	L16	L19	0.1554
K1620	L16	L20	0.1051
K1621	L16	L21	0.0741
K1718	L17	L18	0.4342
K1718WB	L17WB	L18WB	0.2238
C1718	N17C	N18C	2.254e-13
K1719	L17	L19	0.2434
K1719WB	L17WB	L19WB	0.0853
K1720	L17	L20	0.1552
K1721	L17	L21	0.1083
K1722	L17	L22	0.0506
K1819	L18	L19	0.4355
K1819WB	L18WB	L19WB	0.2238
C1819	N18C	N19C	2.282e-13
K1820	L18	L20	0.2418
K1820WB	L18WB	L20WB	0.0708
K1821	L18	L21	0.1558
K1822	L18	L22	0.0742
K1823	L18	L23	0.0613
K1920	L19	L20	0.4330
K1920WB	L19WB	L20WB	0.1463
C1920	N19C	N20C	2.324e-13

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K1921	L19	L21	0.2474
K1921WB	L19WB	L21WB	0.0501
K1922	L19	L22	0.1087
K1923	L19	L23	0.0889
K2021	L20	L21	0.4383
K2021WB	L20WB	L21WB	0.1463
C2021	N20C	N21C	2.402e-13
K2022	L20	L22	0.1558
K2023	L20	L23	0.1228
K2024	L20	L24	0.0889
K2025	L20	L25	0.0613
K2122	L21	L22	0.2174
K2122WB	L21WB	L22WB	0.0811
C2122	N21C	N22C	5.266e-14
K2123	L21	L23	0.1558
K2124	L21	L24	0.1087
K2125	L21	L25	0.0742
K2126	L21	L26	0.0506
K2223	L22	L23	0.4383
K2223WB	L22WB	L23WB	0.1463
C2223	N22C	N23C	2.402e-13
K2224	L22	L24	0.2474
K2224WB	L22WB	L24WB	0.0501
K2225	L22	L25	0.1558
K2226	L22	L26	0.1083
K2227	L22	L27	0.0741
K2228	L22	L28	0.0543
K2324	L23	L24	0.4330
K2324WB	L23WB	L24WB	0.1463
C2324	N23C	N24C	2.324e-13
K2325	L23	L25	0.2418
K2325WB	L23WB	L25WB	0.0708
K2326	L23	L26	0.1552
K2327	L23	L27	0.1051
K2328	L23	L28	0.0742
K2425	L24	L25	0.4355
K2425WB	L24WB	L25WB	0.2238
C2425	N24C	N25C	2.282e-13
K2426	L24	L26	0.2434
K2426WB	L24WB	L26WB	0.0853
K2427	L24	L27	0.1554
K2428	L24	L28	0.1083
K2526	L25	L26	0.4342
K2526WB	L25WB	L26WB	0.2238
C2526	N25C	N26C	2.254e-13
K2527	L25	L27	0.2413
K2527WB	L25WB	L27WB	0.0708
K2528	L25	L28	0.1557
K2627	L26	L27	0.4331
K2627WB	L26WB	L27WB	0.1463
C2627	N26C	N27C	2.332e-13
K2628	L26	L28	0.2472
K2628WB	L26WB	L28WB	0.0501
K2728	L27	L28	0.4380
K2728WB	L27WB	L28WB	0.1463
C2728	N27C	N28C	2.394e-13

.ENDS PACKAGE

\*

\*

-----

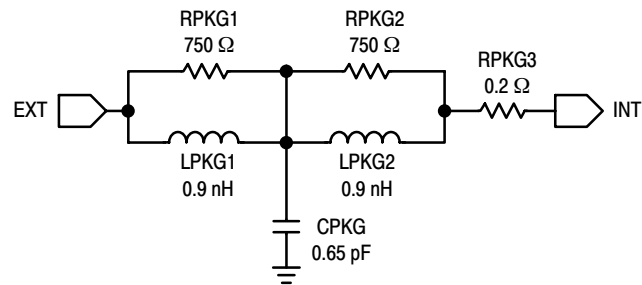
# AN1503/D

---

**Package: PLCC-20**

```
* ECLinPS Package Model (20-lead PLCC)
* GND = 0V
*
* EXT = (External Input to Pin)
* INT = (Internal Output of the Pin)
*
.SUBCKT PKG20 EXT INT GND
CPKG      82      GND      0.65PF
RPKG1     EXT     82       750
RPKG2     82      83       750
RPKG3     83      INT      0.2
LPKG1     EXT     82       0.9NH
LPKG2     82      83       0.9NH
.ENDS PKG20
```

---





## AN1503/D

-----  
**Package: CDIP-16**  
-----

\* ECLinPS Package Model (16-lead CERDIP END PIN)  
\* EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)  
\*  
-----

```
.SUBCKT PKG16EP EXT INT GND
CPKG 82 GND 1.3PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.1
LPKG1 EXT 82 5.5NH
LPKG2 82 83 5.5NH
.ENDS PKG16EP
```

-----

\* ECLinPS Package Model (16-lead CERDIP CENTER PIN)  
\* EXT = (External Input to Pin) INT = (Internal Output of the Pin) GND = (0V)  
\*  
-----

```
.SUBCKT PKG16CP EXT INT GND
CPKG 82 GND 0.7PF
RPKG1 EXT 82 750
RPKG2 82 83 750
RPKG3 83 INT 0.1
LPKG1 EXT 82 2.5NH
LPKG2 82 83 2.5NH
.ENDS PKG16CP
```

-----

APPENDIX A

Package Models Help

In the SPICE netlist, X\_777 is a circuit element (black box) with connections to a subcircuit:

```

circuit element  connections                                     subcircuit
X_777          N01I N01O N02I N02O N03I N03O N04I N04O
               +N05I N05O N06I N06O N07I N07O N08I N08O GND   PACKAGE
    
```

The defined connection nodes of the circuit element are declared as:

```

N01I N01O N02I N02O N03I N03O N04I N04O
N05I N05O N06I N06O N07I N07O N08I N08O GND
    
```

The subcircuit PACKAGE is connected to these same nodes:

```

.SUBCKT PACKAGE  N01I N01O N02I N02O N03I N03O N04I N04O
                 +N05I N05O N06I N06O N07I N07O N08I N08O GND
    
```

where:

```

N01I is the PACKAGE pin #1 internal node connection to the chip pad
N01O is the PACKAGE pin #1 external node connecting to the lead
    
```

Internal to the subcircuit PACKAGE are several nodes for each pin (See Figure 7). For pin 2, of the 8 pin TSSOP, the netlist:

```

R02WB  N02I  N02W  3.815e-02
L02WB  N02W  N02R  9.835e-10
R02    N02R  N02C  9.680e-04
C02    N02C  GND   7.711e-14
L02    N02C  N02O  7.466e-10
    
```

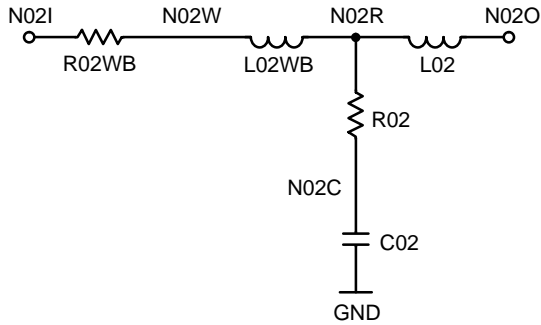


Figure 12.

Parasitic Mutual inductance, K, and capacitance, C, is also represented. Such as “K0102”, where inductance from Lead #1 (L01) to Lead #2 (L02) is indicated.

```

K0102  L01  L02  0.2481
K0102WB L01WB L02WB 0.1729
C0102  N01C  N02C  2.283e-14
K0103  L01  L03  0.1067
K0103WB L01WB L03WB 0.0598
K0104  L01  L04  0.0593
K0203  L02  L03  0.2479
K0203WB L02WB L03WB 0.1463
C0203  N02C  N03C  2.136e-14
K0204  L02  L04  0.1068
K0204WB L02WB L04WB 0.0598
    
```

# AN1503/D

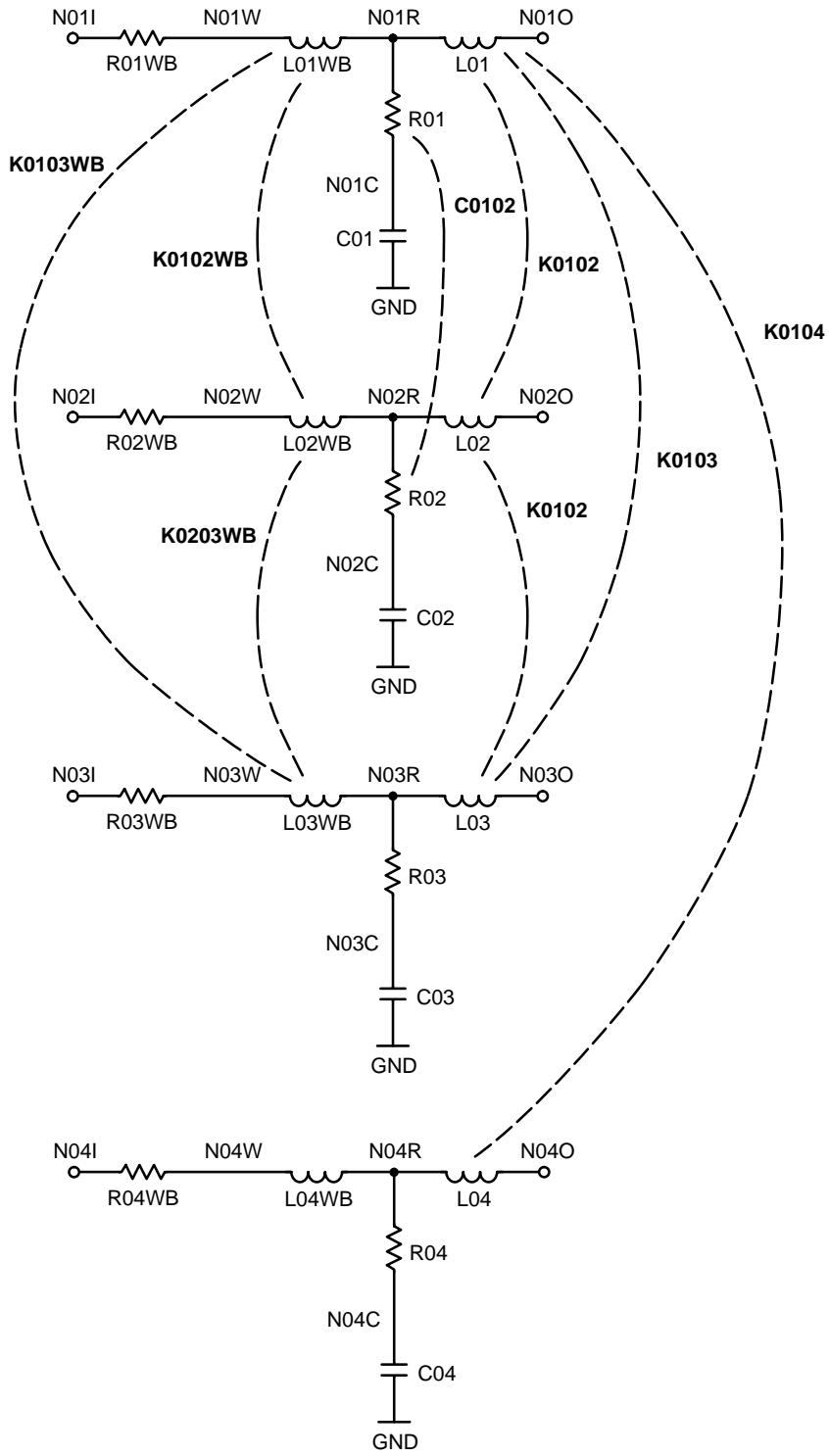



Figure 13.

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