AND8010/D

ECLinPS Lite™ MC100LVELT22 SPICE Model Kit

Prepared by
Paul Shockman

ON Semiconductor Logic Applications Engineering

ON Semiconductor®

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APPLICATION NOTE

Introduction

The objective of this kit is to provide schematic and SPICE parameter information for performing system level interconnect modeling with the Low Voltage ECLinPS Lite Translator TTL to PECL "LVELT22" device. The LVELT22 device is a dual 1 Bit translator from LVTTL/LVCMOS levels to PECL levels. This kit contains model netlists and transistor parameter descriptions for the Input and Output buffers, package models, and ESD protection networks for Input and Output circuits used by the LVELT22 device. These may be interconnected as subcircuits to simulate buffer signals.

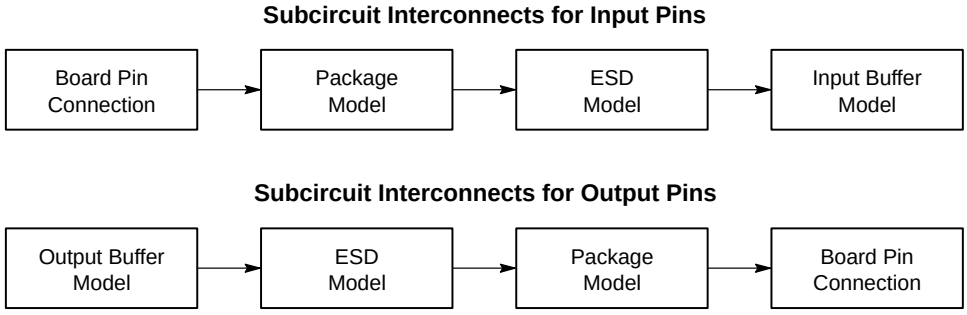

Figure 1. Input and Output Models

Input and Output Buffers

The LVTTL–LVPECL Translator subcircuits use SPICE level 3 netlists in circuit buffer models LVTTLIN and LVTTLOUT. All inputs and outputs are protected by ESD "Electro Static Discharge" protection circuitry. If the user would like to just simulate the output behavior, LVTTLOUT circuit can be stimulated with internal signals levels:

Voltage Internal Input Low	VIIL	VCC–1.1
Voltage Internal Input High	VIIH	VCC–0.8

Package

The MC100LVELT22 is only packaged in the 8 pin SOIC case outline. The coupled transmission line package model, LINES, may to be added to all external pins. In this subcircuit model, all external board side connections of input, output, and supply pins are called N**O and all internal chip side connections of input, output, and supply pins are referred to as N**I as shown in Table 1.

Table 1.

8 Pin SOIC Package Model		
Pin Connection	**Outside to Board**	**Internal to Chip**
1	N01O	N01I
2	N02O	N02I
3	N03O	N03I
4	N04O	N04I
5	N05O	N05I
6	N06O	N06I
7	N07O	N07I
8	N08O	N08I

The LINES model considers the capacitance to be lumped. Minimum (fastest) useable edge rate is 0.076 NS.

April, 2002– Rev. 1

Publication Order Number:
AND8010/D

Modeling

The bias driver schematics for VCS and V1 generation are not included in this kit, as they are unnecessary for interconnection simulation. In addition their detailed netlist modeling would result in a relatively large increase in simulation time. Alternatively the internal reference voltages should be driven with ideal constant voltage sources. This model kit is intended for simulations within the specified power supply range. If supply voltages drop below minimum specification, VCS and V1 can no longer be assumed to be constant. Thus, this model kit should not be used for power up or power down simulations. LVPECL outputs should be terminated properly, such as through ohms to VTT=VCC–2V.

The common global nodes are as follows:

```
*100 VCC
*200 VEE
*300 VCS internal TTL reference = VEE+1.3V
*400 V1 internal TTL reference = 1.5
*10  IN
*5  QI  VCC–1.1 TO VCC–0.8
*6  QIB VCC–0.8 TO VCC–1.1
*20 D
*21 DB
*60 Q
*62 QB
*1  to external PIN
*2  to internal chip CKT
*3  external PIN and internal chip CKT node
```

```
*LVTTLIN
.SUBCKT LVTTLIN 100 200 300 400 10 5 6
Q1  1    10   3   200  TN6
Q2  2    400  3   200  TN6
Q3  100  1    6   200  TN6
Q4  100  2    5   200  TN6
Q5  3    300  7   200  TN6
Q6  6    300  8   200  TN6
Q7  5    300  9   200  TN6
R1  100  1    266
* TC=0.26M, 0.9U
R2  100  1    266
* TC=0.26M, 0.9U
R3  7    200  42
* TC=0.26M, 0.9U
R4  8    200  42
* TC=0.26M, 0.9U
R5   9   200  42
* TC=0.26M, 0.9U
.ENDS LVTTLIN
```

```
.SUBCKT LVTTLOUT 100 200 300 20 21 60 62
Q1   62   20  1  200 TRANA
Q2   60   21  1  200 TRANA
Q3   1    300 2  200 TRANA
R1   100  60  269
* TC=0.26M, 0.9U
R2   100  62  269
* TC=0.26M, 0.9U
R3   2    200  112
* TC=0.26M, 0.9U
.ENDS LVTTLOUT
```

ESD

The ESD protection for the inputs pins D0 and D1 uses the subcircuit model ESDIN. In the ESDIN model, a diode (CBVCC) goes to V_{CC} with a parallel resistor of high value (75 kΩ) and a diode pair (CBSUB devices) go to V_{EE}. The input has a series resistor.

```
.SUBCKT ESDIN 100 200 1 2
D1 1 100 CBVCC
D2 1 200 CBSUB
```

```
D3 1 200 CBSUB
R1 1 VCC 75K
* TC=0.26M, 0.9U
R2 1 2 93
.END ESDIN
```

The ESD model for the PECL output pins (Q0, Q0bar, Q1, Q1bar) use subcircuit model ESDOUT. The ESDOUT is modeled as diode (CBVCC) to V_{CC} and a diode pair (CBSUB devices) to V_{EE}.

```
.SUBCKT ESDOUT 100 200 1
D1 1 100 CBVCC
D2 1 200 CBSUB
D3 1 200 CBSUB
.END ESDOUT
```

```
.MODEL CBVCC D
+ ( IS = 1.00E15 CJO = 527fF Vj = 0.545 M = 0.32 BV = 14.5
+ IBV = 0.1E6 XTI = 5 TT = 1nS )
.MODEL CBSUB D
+ ( IS = 1.00E15 CJO = 453fF TT = 1nS )
```

```
.MODEL TN6   NPN
+(IS  = 8.56E–18  BF  = 120   NF  = 1    VAF = 30   IKF = 10.5mA
+ ISE = 4.48E–16  BR  = 10    NE  = 2    VAR =  5   IKR = 922uA
+ IRB = 13.2uA    RB  = 291.4 RBM = 95.0 RE  = 13.3 RC  = 62.7
+ CJE = 29.9fF    VJE = .9    MJE = .4   XTB = 0.73
+ CJC = 31.2fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 60.9fF    VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 27.6mA
+ ISC=0   EG=1.11   XTI=5.2  PTF=0   KF=0   AF=1   NR=1   NC=2)
*

.MODEL TRANA   NPN
+(IS  = 2.09E–17  BF  = 120   NF  = 1    VAF = 30   IKF = 25.7mA
+ ISE = 1.09E–15  BR  = 10    NE  = 2    VAR =  5   IKR = 2.25mA
+ IRB = 32.2uA    RB  = 122.6 RBM = 42.2 RE  = 5.44 RC  = 32.8
+ CJE = 67.4fF    VJE = .9    MJE = .4   XTB = 0.73
+ CJC = 53.8fF    VJC = .67   MJC = .32  XCJC= .3
+ CJS = 103fF     VJS = .6    MJS = .4   FC  = .9
+ TF  = 8pS       TR  = 1nS   XTF = 10   VTF = 1.4V ITF = 67.5mA
+ ISC=0   EG=1.11   XTI=5.2  PTF=0   KF=0   AF=1   NR=1   NC=2)
*   1.75 x 13.50 emitter (2 emitters)
```

PACKAGE MODEL TRANSMISSION LINES

```
* CONNECT CHIP SIDE TO N**I AND BOARD SIDE TO N**O
*
.SUBCKT LINES N01I N01O N02I N02O N03I N03O N04I N04O
+ N05I N05O N06I N06O N07I N07O N08I N08O
L01WB   N01I    N01M    1.367E–09
L01     N01M    N01O    7.794E–10
C01     N01M    0       2.445E–13
L02WB   N02I    N02M    1.287E–09
L02     N02M    N02O    5.473E–10
C02     N02M    0       1.888E–13
L03WB   N03I    N03M    1.287E–09
L03     N03M    N03O    5.473E–10
C03     N03M    0       1.901E–13
L04WB   N04I    N04M    1.367E–09
L04     N04M    N04O    7.723E–10
C04     N04M    0       2.443E–13
L05WB   N05I    N05M    1.367E–09
L05     N05M    N05O    7.710E–10
C05     N05M    0       2.478E–13
L06WB   N06I    N06M    1.287E–09
L06     N06M    N06O    5.489E–10
C06     N06M    0       1.916E–13
```

```
L07WB   N07I    N07M    1.287E−09
L07     N07M    N07O    5.495E−10
C07     N07M    0       1.930E−13
L08WB   N08I    N08M    1.367E−09
L08     N08M    N08O    7.786E−10
C08     N08M    0       2.451E−13
K0102   L01     L02     0.1687
K0102WB L01WB   L02WB   0.3400
C0102   N01O    N02O    3.674E−14
K0103   L01     L03     0.0702
K0103WB L01WB   L03WB   0.1847
K0203   L02     L03     0.1822
K0203WB L02WB   L03WB   0.3505
C0203   N02O    N03O    3.521E−14
K0204   L02     L04     0.0682
K0204WB L02WB   L04WB   0.1847
K0304   L03     L04     0.1694
K0304WB L03WB   L04WB   0.3400
C0304   N03O    N04O    3.675E−14
K0305WB L03WB   L05WB   0.1847
K0405WB L04WB   L05WB   0.3455
K0406WB L04WB   L06WB   0.1847
K0506   L05     L06     0.1697
K0506WB L05WB   L06WB   0.3400
C0506   N05O    N06O    3.720E−14
K0507   L05     L07     0.0682
K0507WB L05WB   L07WB   0.1847
K0607   L06     L07     0.1824
K0607WB L06WB   L07WB   0.3505
C0607   N06O    N07O    3.570E−14
K0608   L06     L08     0.0702
K0608WB L06WB   L08WB   0.1847
K0708   L07     L08     0.1691
K0708WB L07WB   L08WB   0.3400
C0708   N07O    N08O    3.632E−14
.ENDS LINES
```


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