

AN1400

Application Note

MC10/100H640 Clock Driver Family I/O SPICE Modelling Kit

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This application note provides the SPICE information necessary to accurately model system interconnect situations for designs which utilize the clock driver circuits of the MC10H600 family. The note includes information on the MC10H640, H641, H642, H643, H644 and H645 clock drivers.



MOTOROLA

MC10/100H64 Clock Driver Family I/O SPICE Modelling Kit

Objective

With the difficulty in designing highspeed controlled impedance PC boards and the expense of reworking those boards the ability to model circuit behavior prior to committing to a board layout is essential for high speed logic designers. The purpose of this document is to provide the user with enough information to perform basic SPICE model analysis on the interconnect traces being driven or driving the H640, H641, H642, H643, H644 or H645 clock distribution chips. The packet includes schematics of the input and output structures as well as ESD protection structures and package models which may affect the waveshape of the input and output waveforms. Internal bias regulators and logic circuitry are not included as they have little impact on the I/O characteristics of the device and add a significant amount of time to the standard simulation analysis. In addition a SPICE parameter set for the devices referenced in the schematics is provided. The remainder of this document will introduce the various input and output stages for the H64x clock drivers as well as the other structures which affect the I/O characteristics of these devices.

Schematic Overview

There are five basic schematics which can be used to represent all of the I/O for the H64x family of clock distribution chips. A single ECL input structure, a single TTL input structure and three different output buffers are all that is needed to represent all of the I/O for the six devices. The rest of the schematics provided represent subcircuit schematics for the above mentioned I/O buffers, ESD protection circuitry and package models. The devices shown in shaded boxes on the I/O buffer schematics are modelled by the subcircuits illustrated on the appropriate subcircuit schematic sheet. This hierarchical method of schematic representation is used to help simplify and clarify the buffer schematics.

The H640, H641, H642 and H645 all utilize the same output buffer. This buffer is represented by the H641 Output schematic of Figure 3. These devices are all single supply devices which mean they use +5 volt and ground supplies only. The schematic shows a current mirror used to translate upper rail referenced ECL levels down to ground referenced TTL levels. The output of the current mirror drives a saturating TTL buffer stage. The IN and INB inputs should be driven differentially with the HIGH level at $VCC - 0.85V$ and the LOW level equal to $VCC - 1.85V$. Notice the ESD protection circuitry on the output, this circuitry is represented by the FPS009EX schematic of Figure 9.

The H644 output buffer is represented by the schematic of Figure 7. The H644 is also a single supply device however the output buffer has been enhanced to minimize the delay sensitivity to power supply variation. In addition to the IN and INB inputs the H644 output buffer also requires two bias supplies; BIAS1 and BIAS2. The IN and INB inputs should be driven differentially from VCC to $VCC - 1.6V$, while the BIAS1 and BIAS2 should be set at 4.0V and 3.2V respectively. The

same ESD structure is used on the H644 output buffer as is used on the H641 output buffer.

The H643 is the only dual supply translating clock driver available in the H64x family of devices. Because it is a dual supply part (requires +5V, -5.2V and Ground) the output buffer differs from those for the rest of the family. Figure 4 represents the schematic for the output buffer utilized by the H643. The IN and INB inputs should again be driven differentially; this time with voltage swings of $-1.3V$ to $-1.7V$. The CBIAS input should be forced to 1.1V, the BIAS3 to 3.8V and the VCS current source bias should be set at $VEE + 1.3V$. Notice the separate TTL VCC's and TTL grounds used in the buffer. To best simulate the device it will be necessary to supply the different power supplies through separate package models. The VEE on the front end differential amplifier should be connected to $-5.2V$. The H643 again uses the same ESD protection scheme as the H641.

Table 1. Device Type Input Cross Reference

Part Type	ECL Inputs	TTL Inputs
H640, H642, H644	DE/DE	DT, SEL, R
H641, H643	D/D, LEN, EN	None
H645	None	D0, D1, SEL

Two input structures can represent all of the inputs for the H64x family of clock drivers, one for TTL inputs and one for ECL inputs. The following table outlines the various inputs and the appropriate input model. For the single supply devices with ECL inputs the VCC and the VEE on the typical ECL input gate of Figure 1 should be tied to +5V and ground respectively. For the H643 the ECL input supplies should be ground and $-5.2V$ for VCC and VEE respectively. All input pins should have both a package model and ESD protection circuitry connected to them. The package model of Figure 9 is self explanatory, the parasitic values provided are worst case numbers. The package capacitance combines with the parasitic transistor capacitance of the input device and the ESD circuitry to comprise the load capacitance of the input. The various input buffer ESD circuits are outlined in Figure 9, notice that the ECL inputs utilize a different structure than the TTL inputs and outputs. The typical ECL input schematic represents a single ended ECL input, the VBB reference should be tied to $VCC - 1.3V$ and the VCS bias should be tied to $VEE + 1.3V$. To simulate a differential ECL input one simply connects the complimentary input to the "VBB" side of the input gate along with an associated ESD and package model. The differential input does not use the VBB switching reference.

For all of the input and output buffer schematics the resistors should NOT be simulated as simple SPICE resistors. Because these resistors are realized by a diffusion step in wafer processing there are parasitic capacitances associated with each. The subcircuit schematic is shown for the resistors in Figure 9. The value of each subcircuit resistor is one half the value given on the top level schematic and the parasitic capacitance is modelled by a diode back biased to VCC. Also

note that the resistor temperature coefficient (TC) values for both the resistor subcircuit and the resistors in the device subcircuits are provided. For modelling at nominal temperatures only these TC's can be omitted. If however modelling will be performed at the temperature extremes the TC information should be included.

The following table is provided to summarize the various internal voltage swings and bias levels required to run the appropriate SPICE simulations.

Table 2. Input and Bias Levels

Schematic	Input	Levels
ECL Input	V _{BB} V _{CS}	V _{CC} - 1.3V V _{EE} + 1.3V
H641 Output	IN/INB	V _{CC} - 0.85V to V _{CC} - 1.85V
H643 Output	IN/INB CBIAS BIAS3 V _{CS}	-1.4V to -1.7V 1.1V 3.8V V _{EE} + 1.3V
H644 Output	IN/INB BIAS1 BIAS2	V _{CC} to V _{CC} - 1.6V 4.0V 3.2V

Handling Power Supplies

Clock distribution chips by definition are simultaneous switching circuits, therefore it is imperative to properly apply the power supply voltages to accurately model these circuits. This section will explain the power supply terminology used on the I/O buffer schematics and how to properly apply these supplies with the appropriate package model.

Table 3. Power Pin Descriptions

Power Supply	Description
EVCC	EVCC is the most positive supply for the ECL input gate (+5V for the H640, 1, 2, 4 and ground for the H643.)
VEE	V _{EE} is the most negative supply for an ECL gate. For the H640, 1, 2, 4 it is equal to ground for the H643 it is equal to -5.2 or -4.5V.
TVCCI	Internal V _{CC} for TTL circuitry.
TVCCO	Output V _{CC} for TTL circuitry.
GNDI	Internal Ground for TTL circuitry.
GNDO	Output Ground for TTL circuitry.

Table 3 lists the voltage supplies referenced on the I/O schematics along with a description of each. The key to properly simulating these power supplies is in the application of the package model. Because the output buffers, to a varying degree, share VCC and ground pins, adjustments need to be

made to get a more accurate model if all of the outputs are not simulated at the same time. If for example a single output is to be simulated the package model for the VCCO and GNDO supplies should be scaled based on the number of outputs which normally share the supplies. If the simulated output normally shares its supplies with two other outputs the package inductance would be tripled to simulate the same inductive glitch seen on the power pin in an actual application. The capacitive value for the package model is not as critical and thus can be left alone. This method will allow users to more accurately model an output behavior without resorting to more complicated and lengthy simulations. The internal power and ground pins are all powered through a single pin and are basically static, as a result no adjustments are needed for the package models on these supplies. Table 4 outlines the internal power distribution for the H64x clock drivers, this information can be used to determine the scaling factors for the package inductance for the output buffers. The outputs are grouped as they are in the physical layout of the device. To use the table simply identify the output in question and divide the number of outputs in the group by the number of power pins for that group, this will give the multiplication factor for the inductance.

Table 4. Power Pins versus Outputs

Part Type	Outputs	#VCCO	#GNDO
H640	Q0, Q1, Q2, Q3	4	4
	Q0B, Q1B	1	1
	Q4, Q5	1	1
H641, H645	Q0, Q1, Q2	2	2
	Q3, Q4, Q5	2	2
	Q6, Q7, Q8	2	2
H642	Q0, Q1	2	2
	Q2, Q3	2	2
	Q4, Q5	1	1
	Q6, Q7	1	1
H643	Q0, Q1, Q2, Q3	1	2
	Q4, Q5, Q6, Q7	1	2
H644	Q0, Q1, Q2B	1	2
	Q3B, Q4, Q5	1	2

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk. However with today's advanced design tools it will probably be a simpler task to enter the schematics in a good schematic capture package than it will be to manipulate the generic netlists. If, however the netlists are desired or questions arise about the contents of this document the user can contact an ECL applications engineer for assistance.

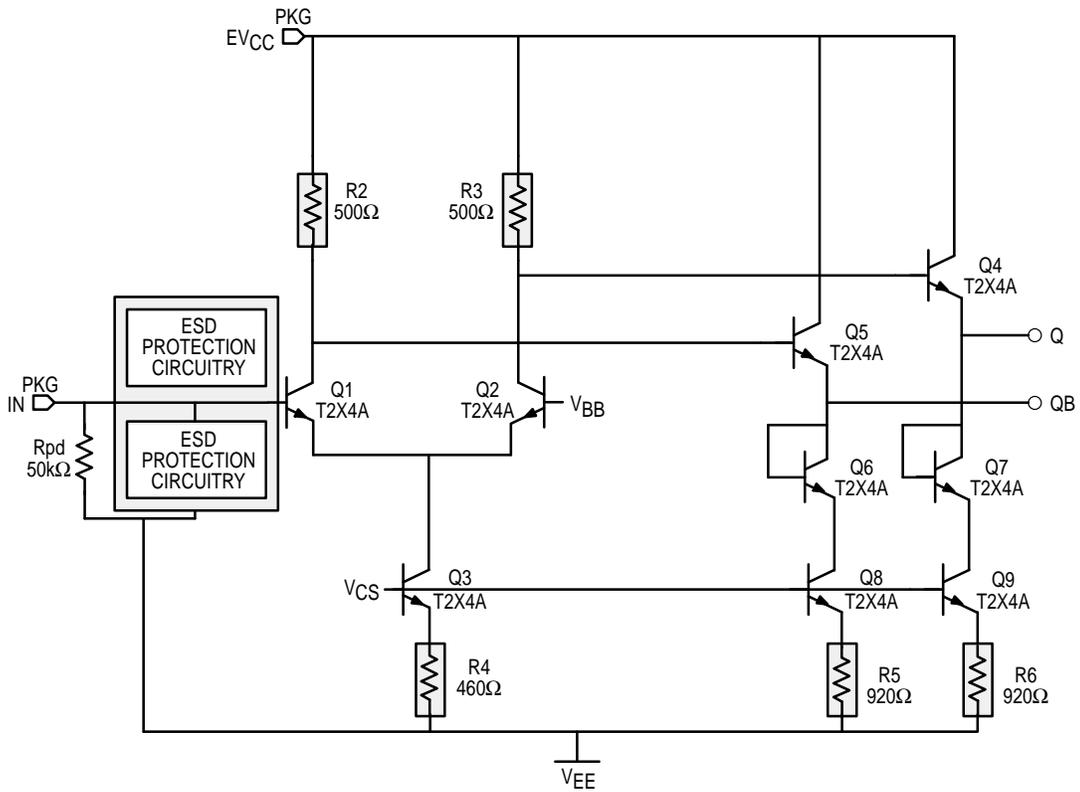


Figure 1. Typical ECL Input Gate

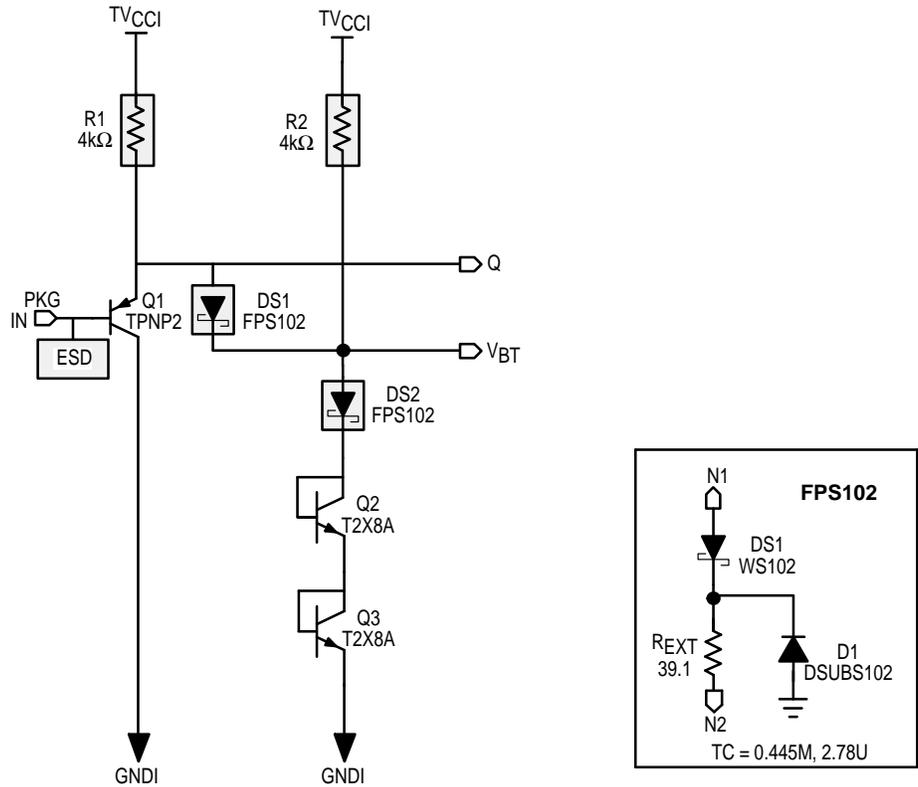


Figure 2. Typical TTL Input Gate

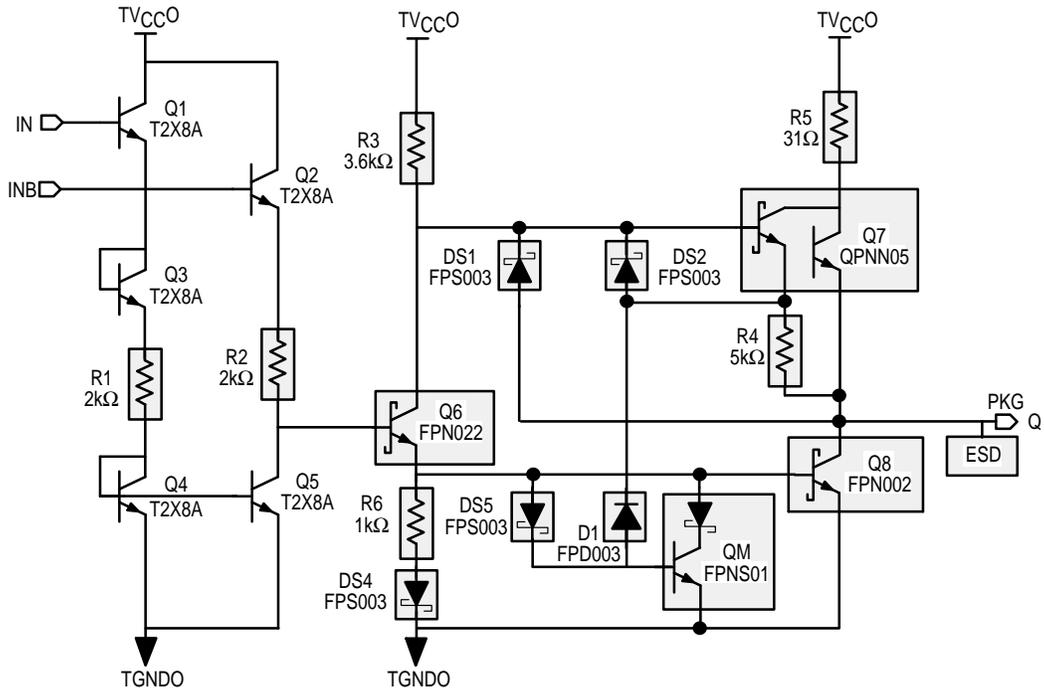


Figure 3. H640, H641, H642, H645 Output Gate

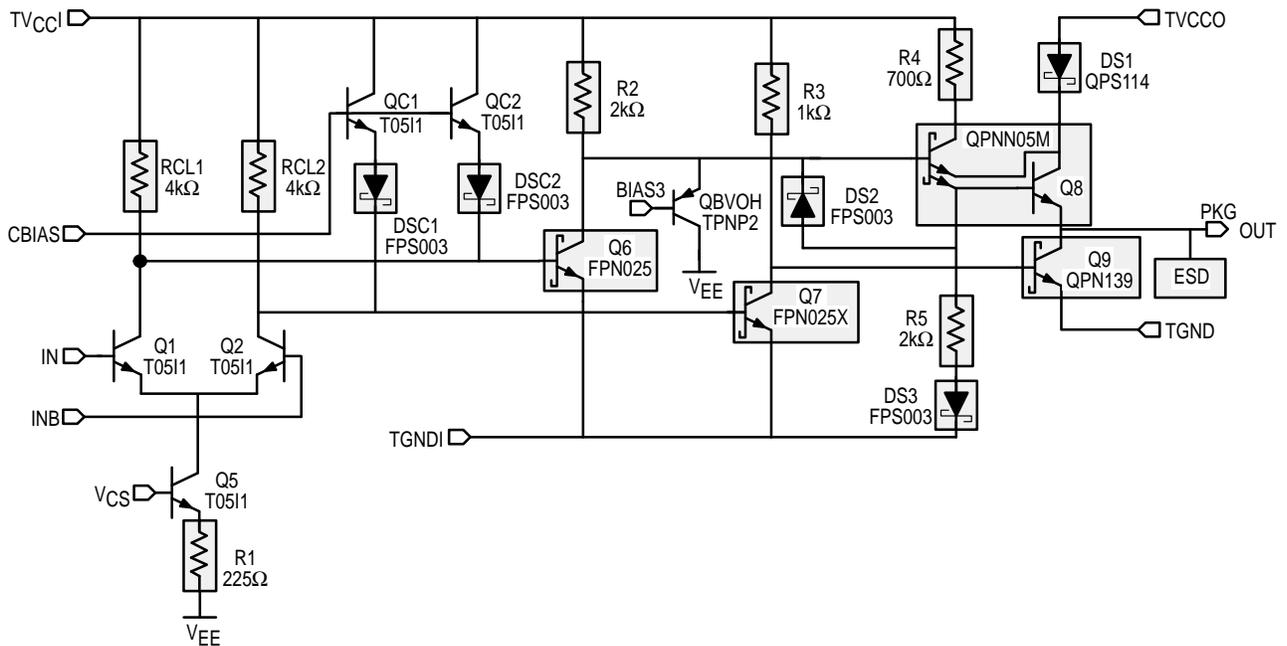
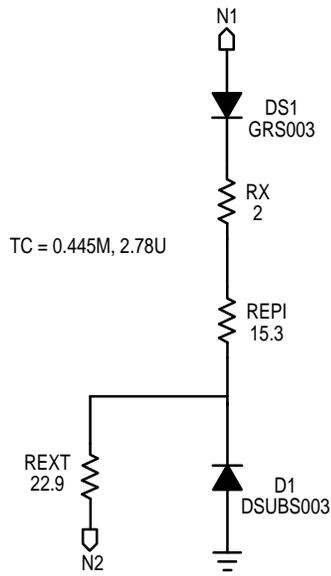
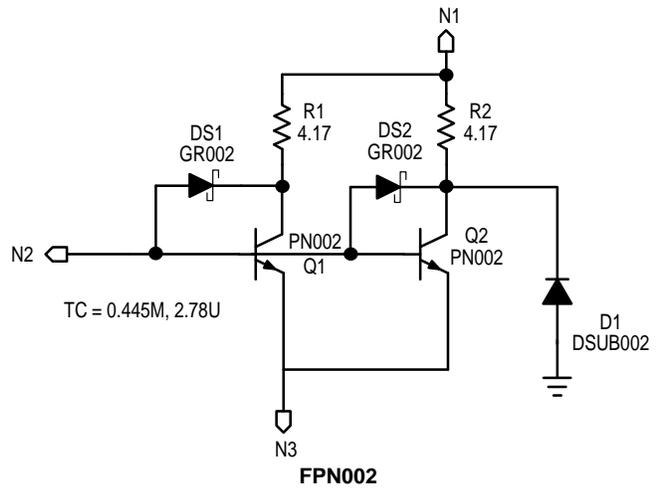


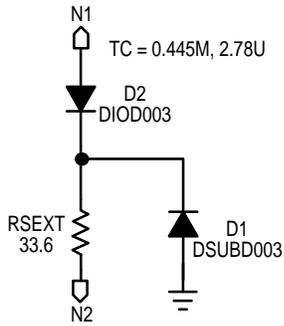
Figure 4. H643 Output Gate



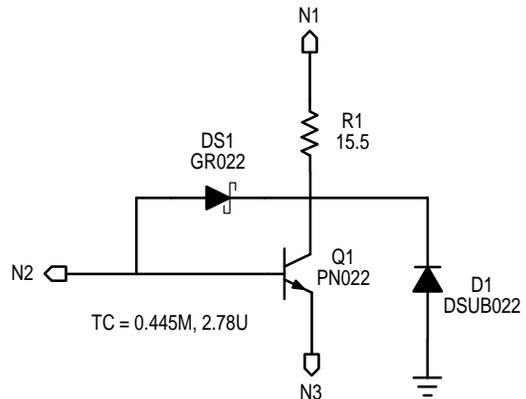
FPS003



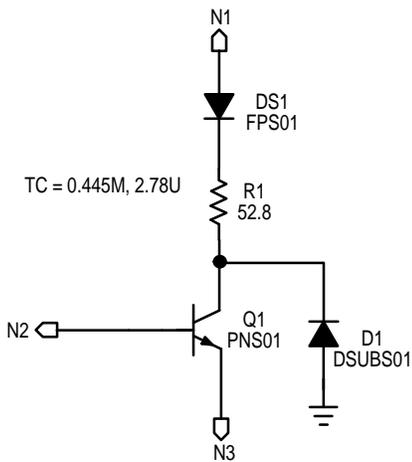
FPN002



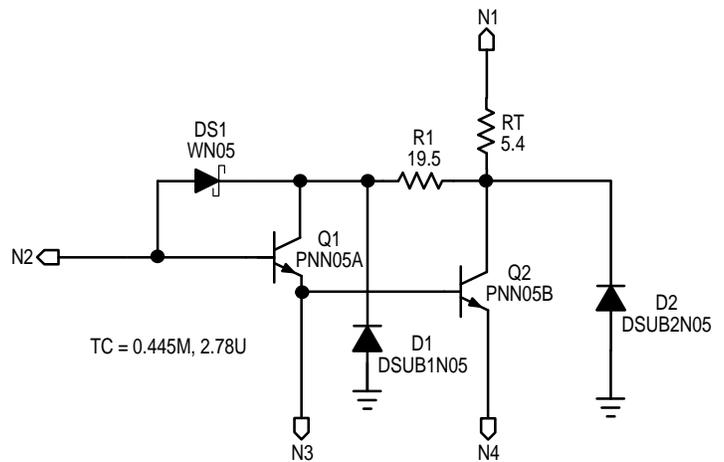
FPD003



FPN022

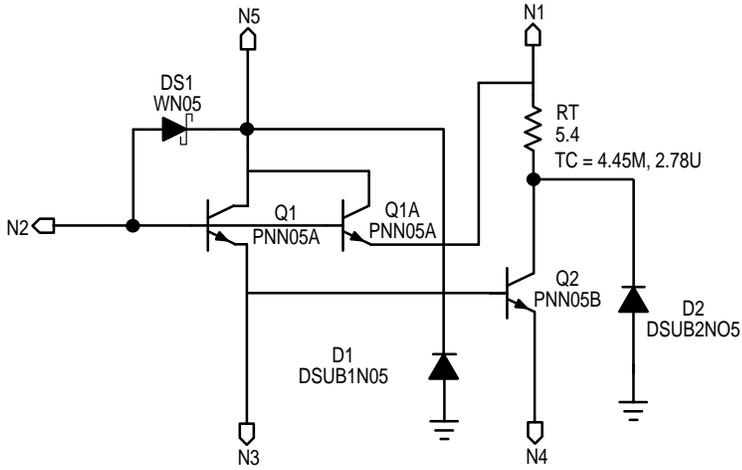


FPNS01

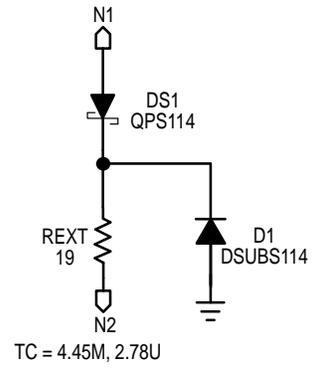


QPNN05

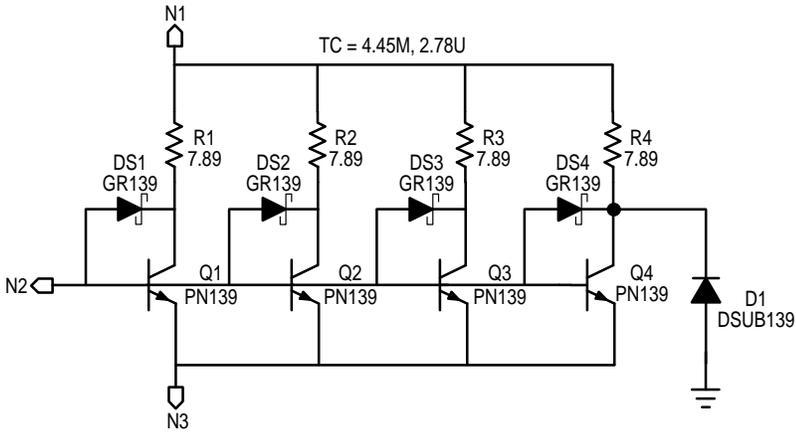
Figure 5. H640, H641, H642, H645 Output Subcircuits



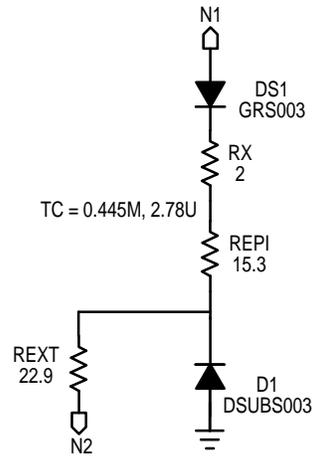
QPNN05M



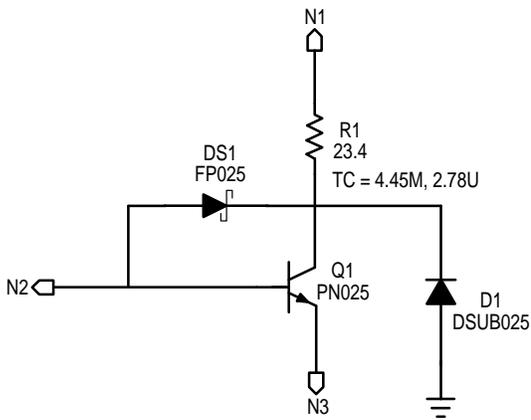
QPS114



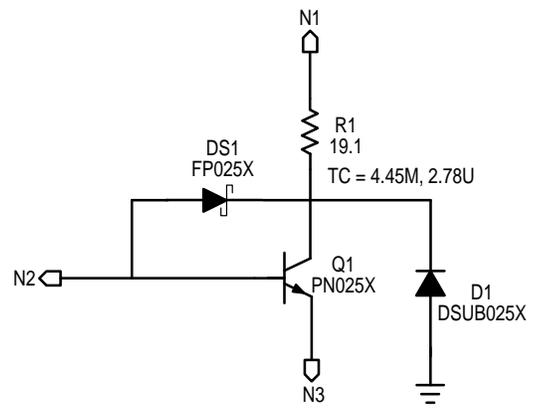
QPN139



FPS003



FPN025



FPN025X

Figure 6. H643 Output Subcircuits

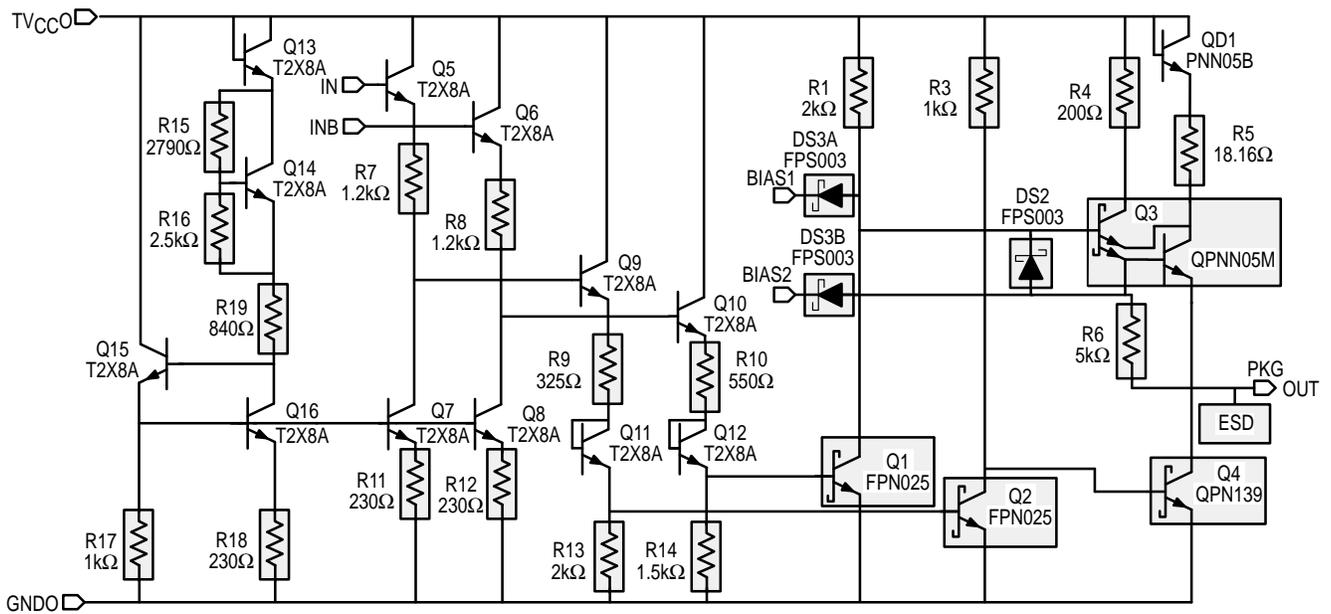


Figure 7. H644 Output Gate

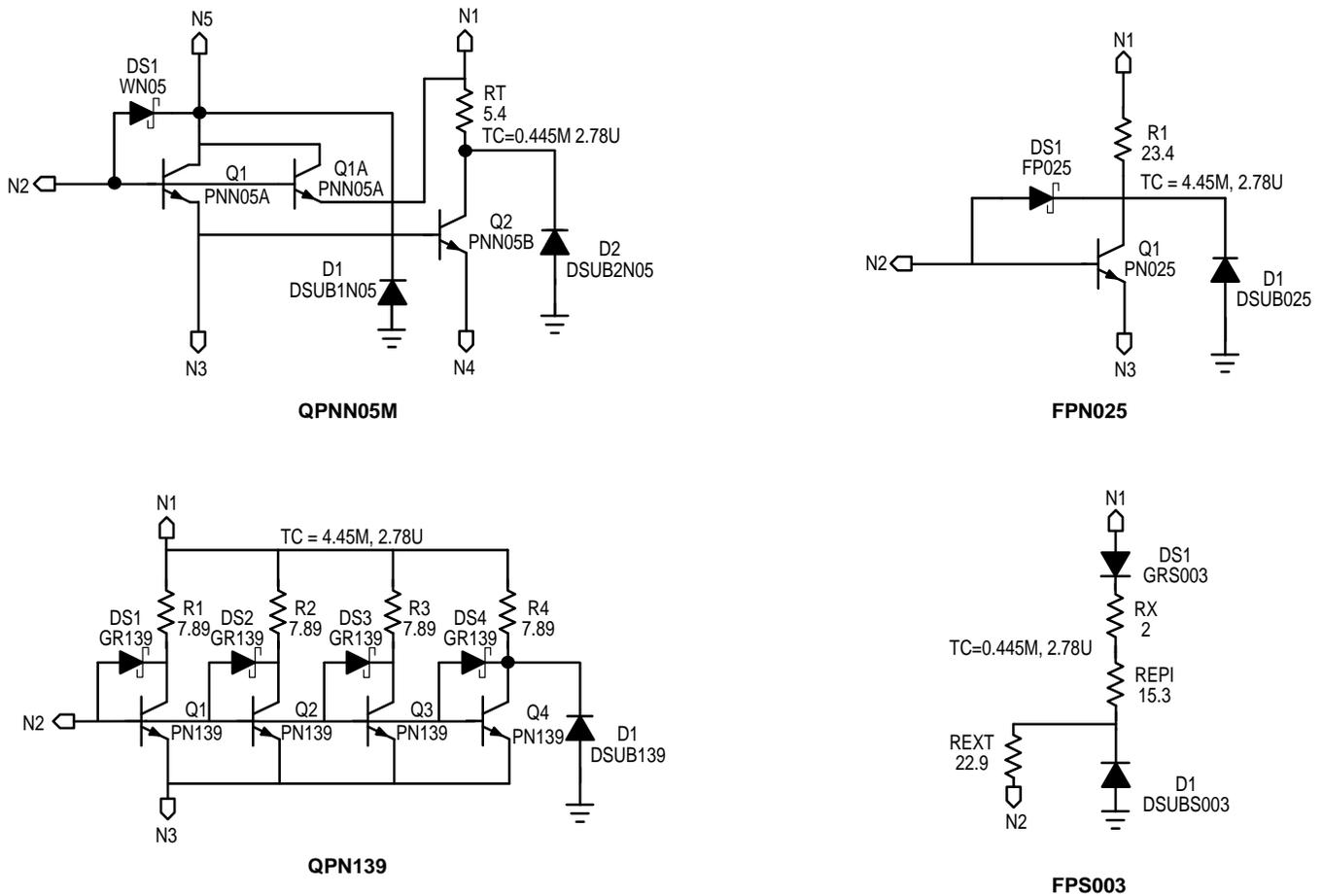
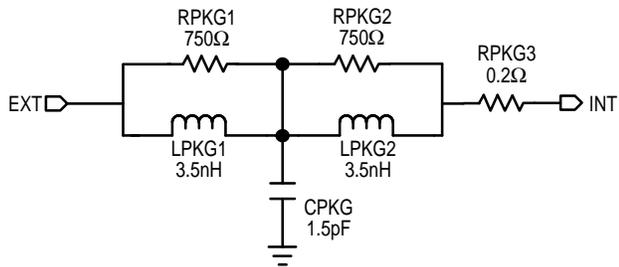
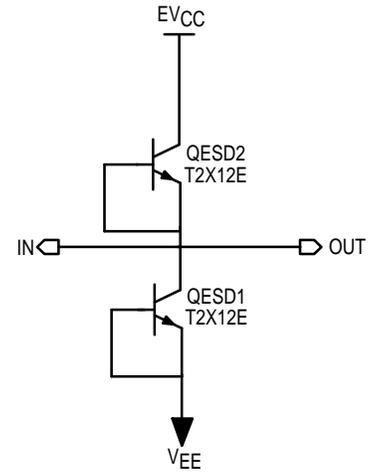


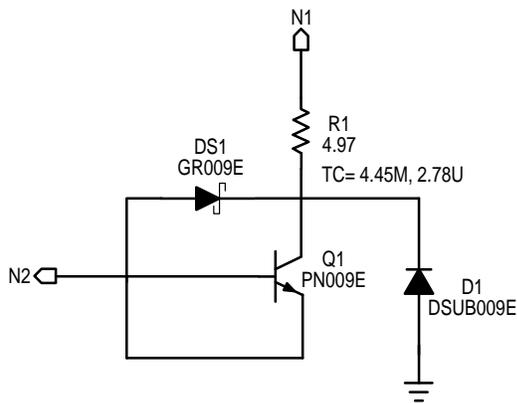
Figure 8. H644 Output Subcircuits



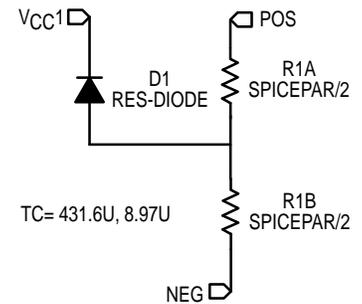
28-lead PLCC Package Model



ECL ESD Structure



FPS009EX
TTL ESD Structure



Resistor Model

Figure 9. Miscellaneous Subcircuits

SPICE Parameter List

TTL Transistor Parameters

```
.MODEL DSUB1N05 D (CJO=203FF VJ=.51 M=.24)
.MODEL DSUB2N05 D (CJO=388FF VJ=.51 M=.24)
.MODEL PNN05A NPN (IS=1.662E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+ ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+ IKR=.7125MA ISC=1.803E-16 NC=1 RB=656.7 RBM=218
+ RE=0 RC=91.62
+ CJE=86.47FF VJE=.9 MJE=.4
+ CJC=58.32FF VJC=.53 MJC=.37
+ TF=40P XTF=0 VTF=100 ITF=3.89MA PTF=0
+ TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
```

TTL Transistor Parameters (continued)

```
.MODEL PNN05B NPN      (IS=1.583E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=6.78MA ISC=1.717E-15 NC=1 RB=77.29 RBM=31.25
+                      RE=0 RC=9.61
+                      CJE=751.6FF VJE=.9 MJE=.4
+                      CJC=445.2FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=37.1MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL WN05 D          (IS=1.0578E-12 RS=37.6 N=1.044 TT=10PS
+                      CJO=141.75FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB022 D      (CJO=214FF VJ=.51 M=.24)
.MODEL PN022 NPN      (IS=2.1E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=.9MA ISC=2.28E-16 NC=1 RB=541 RBM=193
+                      RE=0 RC=72.5
+                      CJE=107FF VJE=.9 MJE=.4
+                      CJC=93.5FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=4.9MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR022 D        (IS=8.87E-14 RS=52 N=1.044 TT=10PS
+                      CJO=112FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB002 D      (CJO=1.53PF VJ=.51 M=.24)
.MODEL PN002 NPN      (IS=3.15E-16 BF=70 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=13MA ISC=3.73E-16 NC=1 RB=125 RBM=32
+                      RE=0 RC=2.98
+                      CJE=1.19PF VJE=.9 MJE=.4
+                      CJC=400FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=148MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR002 D        (IS=1.04E-13 RS=7.2 N=1.044 TT=10PS
+                      CJO=131FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS01 D      (CJO=164FF VJ=.51 M=.24)
.MODEL PNS01 NPN      (IS=2.1E-17 BF=70 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=.9MA ISC=2.28E-16 NC=1 RB=573 RBM=225
+                      RE=0 RC=72.5
+                      CJE=107FF VJE=.9 MJE=.4
+                      CJC=67.5FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=4.9MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FPS01 D        (IS=1.80E-13 RS=0 N=1.044 TT=10PS
+                      CJO=151FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DIOD003 D      (IS=5.82E-17 RS=2.92 N=1 TT=500PS
+                      CJO=202FF VJ=.51 M=.24
+                      EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUBD003 D     (IS=1E-16 RS=0 N=1 TT=500PS
+                      CJO=326FF VJ=.51 M=.24
+                      EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUBS114 D     (IS=1E-16 RS=0 N=1 TT=500PS
+                      CJO=2.75PF VJ=.51 M=.24
+                      EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL QPS114 D       (IS=2.52E-12 RS=1.35 N=1.044 TT=10PS
+                      CJO=2.1PF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
```

TTL Transistor Parameters (continued)

```
.MODEL DSUB025X D      (CJO=284FF VJ=.51 M=.24)
.MODEL PN025X NPN      (IS=4.32E-17 BF=113 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=1.85MA ISC=4.68E-16 NC=1 RB=175 RBM=65
+                      RE=0 RC=35.2
+                      CJE=193FF VJE=.9 MJE=.4
+                      CJC=158FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025X D        (IS=1.08E-13 RS=48.3 N=1.044 TT=10PS
+                      CJO=90FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB025 D      (CJO=284FF VJ=.51 M=.24)
.MODEL PN025 NPN      (IS=2.45E-17 BF=113 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=1MA ISC=2.66E-16 NC=1 RB=193 RBM=89
+                      RE=0 RC=62
+                      CJE=123FF VJE=.9 MJE=.4
+                      CJC=108FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=5.7MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL FP025          (IS=1.4E-13 RS=52 N=1.044 TT=10PS
+                      CJO=117FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUB139 D      (CJO=2.12PF VJ=.51 M=.24)
.MODEL PN139 NPN      (IS=1.03E-16 BF=113 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=4.4MA ISC=1.22E-16 NC=1 RB=117 RBM=47
+                      RE=0 RC=8.41
+                      CJE=493FF VJE=.9 MJE=.4
+                      CJC=244FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=96.7MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR139 D        (IS=7E-14 RS=10 N=1.044 TT=10PS
+                      CJO=88FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL GRS003 D       (IS=4.27E-14 RS=53 N=1.044 TT=10PS
+                      CJO=54FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
.MODEL DSUBS003 D     (IS=1E-16 RS=0 N=1 TT=500PS
+                      CJO=127FF VJ=.51 M=.24
+                      EG=1.115 XTI=3 FC=.5 BV=35)
.MODEL DSUB009E D     (CJO=106FF VJ=.51 M=.24)
.MODEL PN009E NPN     (IS=3.92E-16 BF=113 NF=1.008 VAF=30 IKF=10A
+                      ISE=0 NE=1 BR=5 NR=1 XCJC=.1 VAR=100
+                      IKR=.3MA ISC=4.25E-15 NC=1 RB=185 RBM=39
+                      RE=0 RC=3.9
+                      CJE=1.37PF VJE=.9 MJE=.4
+                      CJC=609FF VJC=.53 MJC=.37
+                      TF=40P XTF=0 VTF=100 ITF=1.64MA PTF=0
+                      TR=200P XTB=1.51 EG=1.115 XTI=5 FC=0.5 )
.MODEL GR009E        (IS=5.4E-13 RS=9.57 N=1.044 TT=10PS
+                      CJO=683FF VJ=.4 M=.33
+                      EG=.69 XTI=3 FC=.5 BV=30)
```

ECL Transistor Model

.MODEL T0511 NPN

+ IS=21.18E-18 BF=112 BR=5.108 RE=1.533 IKF=.0213 VAF=41.8
+ ISE=250E-18 RB=52.7 RBM=0 IRB=0 IKR=53E-5 VAR=3.766
+ ISC=95.62E-18 EG=1.11 RC=26.33 NC=1.141 NR=.997
+ CJE=67.7E-15 VJE=1.037 MJE=.5718 NF=1.000 XTI=4.7
+ CJC=99.5E-15 VJC=.603 MJC=.266 NE=2.000 XTB=1.15
+ CJS=152E-15 VJS=.5052 MJS=.3465 TR=9.92E-9 PTF=20
+ TF=35E-12 XTF=2.25 VTF=1.67 ITF=.00808 XCJC=.069 FC=.8

.MODEL TPNP2 PNP

+ IS=7.69E-17 BF=5 BR=1 RB=164 RC=56 CJE=.086E-12
+ CJC=1.4E-12

.MODEL T2X4A NPN

+ IS=12.88E-18 BF=112.3 BR=.9806 RE=2 IKF=.0143 VAF=46
+ ISE=239.4E-18 RB=400 RBM=200 IRB=850E-6 IKR=.364 VAR=3.581
+ ISC=64.04E-18 EG=1.11 RC=35.4 NC=1.045 NR=.9972
+ CJE=44.5E-15 VJE=1.037 MJE=.572 NF=1.000 XTI=4.7
+ CJC=61E-15 VJC=.75 MJC=.266 NE=2.000 XTB=1.15
+ CJS=109.4E-15 VJS=.5815 MJS=.5273 TR=9.92E-9 PTF=30
+ TF=32E-12 XTF=2.25 VTF=1.67 ITF=.00808 XCJC=.059 FC=.8

.MODEL T2X8A NPN

+ IS=25.32E-18 BF=113 BR=1.383 RE=1.50 IKF=.0273 VAF=46
+ ISE=478E-18 RB=222 RBM=111 IRB=1.7E-3 IKR=.3655 VAR=3.581
+ ISC=80E-18 EG=1.11 RC=22.67 NC=1.045 NR=.9972
+ CJE=79.6E-15 VJE=1.037 MJE=.572 NF=1.000 XTI=4.7
+ CJC=88.7E-15 VJC=.75 MJC=.266 NE=2.000 XTB=1.15
+ CJS=130.9E-15 VJS=.5815 MJS=.5273 TR=8.515E-9 PTF=50
+ TF=34.62E-12 XTF=2.599 VTF=1.578 ITF=.016 XCJC=.085 FC=.8

.MODEL T2X12E NPN

+ IS=37.37E-18 BF=113 BR=1.383 RE=1.30 IKF=.0411 VAF=464
+ ISE=726E-18 RB=154 RBM=76.9 IRB=2.55E-3 IKR=.3655 VAR=3.681
+ ISC=100E-18 EG=1.11 RC=17 NC=1.045 NR=.9972
+ CJE=114E-15 VJE=1.037 MJE=.572 NF=1.000 XTI=4.7
+ CJC=114E-15 VJC=.75 MJC=.266 NE=2.000 XTB=1.15
+ CJS=152.3E-15 VJS=.5815 MJS=.5273 TR=8.515E-9 PTF=80
+ TF=34.62E-12 XTF=2.599 VTF=1.475 ITF=.024 XCJC=.099 FC=.8

Resistor Diode Model

.MODEL RES-DIODE D (IS=1E-16 TT=1NS VJ=.759V M=.333 CJO=50FF)

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