TFP401, TFP401A Design Notes

Digital Visual Interface

ABSTRACT

The Texas Instruments TFP401 is one device in a family of TI PanelBus™ flat panel display products that simplifies digital display systems design by offering value added flexibility and reliability to the system designer. The TFP401 is a DVI compliant flat panel digital receiver that supports display resolutions ranging from VGA to UXGA in 24-bit, true-color pixel format. The TFP401 offers design flexibility in that it can be configured to drive one or two pixels per clock and supports TFT or DSTN panels.

The TFP401 combines PanelBus™ circuit innovation with TI's advanced 0.18-µm EPIC-5™ CMOS process technology along with TI PowerPAD™ package technology to achieve a reliable, low-powered, low noise, high-speed digital solution to digital visual interfacing.

Fundamental Operation

The TFP401 is a DVI (Digital Visual Interface) compliant digital receiver that is used in digital flat panel display systems to receive and decode T.M.D.S. encoded RGB pixel data streams. In a digital display system a host, usually a PC or workstation, contains a DVI compliant transmitter that receives 24-bit pixel data along with appropriate control signals and encodes them into a high-speed low-voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI compliant receiver like the TI TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. The TFP401 supports resolutions up to UXGA.

Routing High-Speed Differential Signal Traces

(RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+)

Trace impedance should be controlled for optimal performance. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2x to 4x Height. A differential trace separation of 4x Height yields about 6% cross-talk(6% effect on impedance).

We recommend that differential trace routing should be side-by-side, though it is not important that the differential traces be tightly coupled together because tight coupling is not achievable on PCB traces. Typical ratios on PCB's are only 20-50%, 99.9% is the value of a well balanced twisted-pair cable.

Each differential trace should be as short as possible (< 2" preferably) with no 90° angles. These high-speed transmission traces should be on layer 1 (top layer).

RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+ signals all route directly from the DVI connector pins to the device, no external components are needed.

DVI Connector Routing

Clear-out holes for connector pins should leave space between pins to allow continuous ground through the pin field. Allow enough spacing in ground plane around signal pin vias however, keep enough copper between vias to allow for ground current to flow between the vias. Avoid creating a large ground-plane slot around the entire connector, minimizing the via capacitance is the goal.

Data and Control Signal Output Routing

The trace length of data and control signals out of the receiver should be kept as close to equal as possible. Trace separation should be ~5x Height. As a general rule, traces also should be less than 2.8," if possible (longer traces can be acceptable).

Calculation

*Delay = 85 * SQRT Er*

Er = 4.35 ; relative permitivity of 50% resin FR-4 @ 1GHz

Delay = 177 ps/inch

Length of rising edge = Tr(picoseconds)/Delay ;Tr = 3 ns

= 3000 ps/177 ps per inch

= 16.9 inches

Length of rising edge / 6 = Max length of trace for lumped circuit

16.9 / 6 = ***2.8 inches****.*

Power Supply De-Coupling

Use solid ground planes, tie ground planes together with as many vias as is practical. This will provide a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus receiver power and ground pins and all by-pass caps to appropriate power or ground plane with via. Vias should be as fat and short as practical, the goal is to minimize the inductance.

DVDD

Place one 0.01-µF capacitor as close as possible between each DVDD device pin (Pins 6, 38, 67) and ground.

A 22-µF tantalum capacitor should be placed between the supply and 0.01-µF capacitors.

A ferrite bead should be used between the source and the 22-µF capacitor.

OVDD

Place one 0.01-µF capacitor as close as possible between each OVDD device pin (Pins 18, 29, 43, 57, 78) and ground.

A 22-µF tantalum capacitor should be placed between the supply and 0.01-µF capacitors.

A ferrite bead should be used between the source and the 22-µF capacitor.

AVDD

Place one 0.01-µF capacitor as close as possible between each AVDD device pin (Pins 82, 84, 88, 95) and ground.

A 22-µF tantalum capacitor should be placed between the supply and 0.01-µF capacitors.

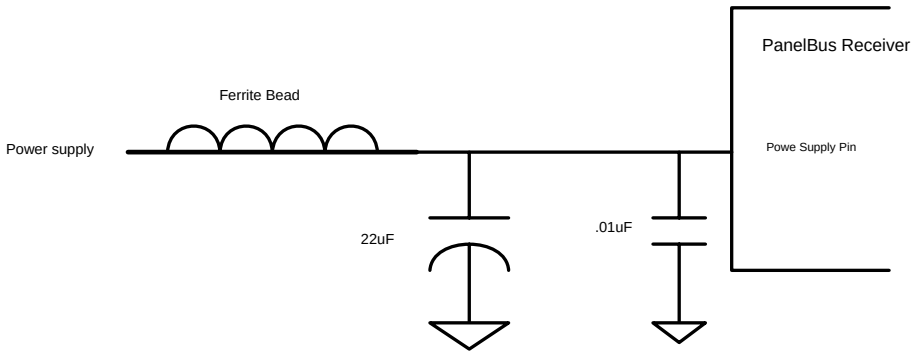
A ferrite bead should be used between the source and the 22-µF capacitor.

PVCC

Place three 0.01-µF capacitors in parallel as close as possible between the PVDD device pin (Pin 97) and ground.

A 22-µF tantalum capacitor should be placed between the supply and 0.01-µF capacitors.

A ferrite bead should be used between the source and the 22-µF capacitor.



PowerPad™ Connection

Designing boards for PowerPad™ connection is optional, there are benefits with the use of TI's PowerPad™ Technology.

Ground plane dimension for TI's 100-Pin PZP package are 12 × 12 mm.

Maximum land area = 12 mm

Reference the following website for detailed PowerPad™ information:

http://www-s.ti.com/sc/techlit/slma002

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